# Cerebro 2 1T1R RRAM ASIC Datasheet

Version 0.7

September 18, 2020


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## Revision History

| Version | Date | Comments | Approved |
|---|---|---|---|
| 0.1 | July 8, 2019 | Initial version | |
| 0.5 | May 10, 2020 | Updates post tapeout | |
| 0.6 | May 18, 2020 | Added sections on ADC and Gate DAC | |

## Terminology & Naming Convention

| Names | | Meaning |
|---|---|---|
| **Chip Blocks** | | |
| tile_mxn | | Bitcell array of mxn synapses and closely associated supporting circuits |
| Array | | 1T1R RRAM bitcell array(s) |
| 1R array | | 1R RRAM array |
| row | | Bitcell row along DRL direction |
| column | | Bitcell column along BL direction |
| Gmin | | Minimum RRAM conductance (fully off) |
| Gmax | | Maximum RRAM conductance (fully on) |
| G0 | | RRAM lowest weight conductance |
| G15 | | RRAM 15$^{th}$ level of weight conductance |
| | | |
| | | |
| **Supplies** | | |
| gnd | | Use whatever is in TPSCo PDK |
| gdd | | Low voltage supply for low voltage devices |
| Vdd x.yV | | High voltage supply for high voltage devices |
| vdd io | | Voltage supply for IO |
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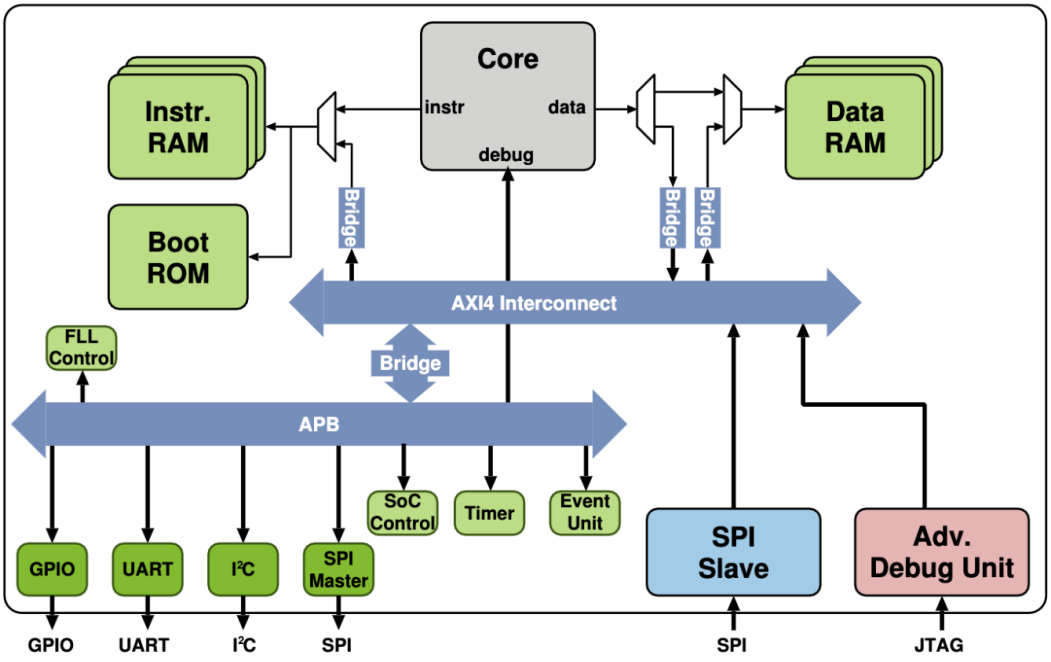
# RISC-V

## PULPino



# AXI Interconnect Modifications

This datasheet only applies to AXI bus in Pulpino, and mainly focuses on interfacing RRAM Blocks in AMAT Project.

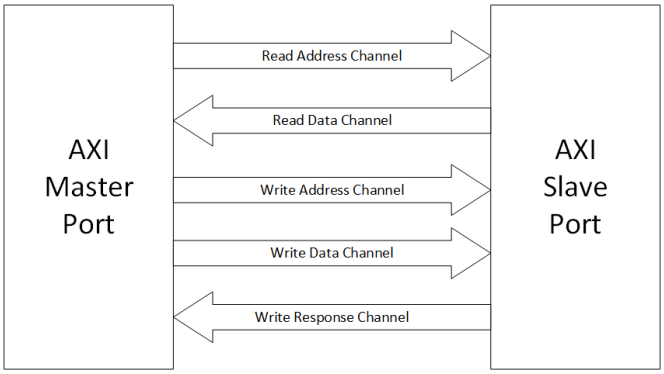
## Blocks and High-Level Overview

AXI is the 3rd generation of ARM's AMBA(Advanced Microcontroller Bus Architecture), and it's full name is Advanced Extensible Interface. It has many versions, including Stream Interface and Memory-Mapped Interface, and under Memory-Mapped Interface there are Full version and Lite version. The one used in Pulpino is Memory-Mapped AXI4 Full.
Here's main features:

- Point to Point Interconnect
- Separate Channels of Signals
- Hand-shaking Confirmation
- Continuous Transfer through Burst (probably won't be used in this project)
- Memory Mapped in Address Space

## Single Master-Slave Pair Interconnect

AXI Master is the module initiates transactions(read or write), and AXI Slave is the module responses to transactions from Master. What connects AXI Master and AXI Slave is **5-channel** AXI Interconnect, which is shown in the figure below and will be illustrated soon. One 5-channel Interconnect only connects one Master to one Slave, and this gives AXI the feature **Point to Point Interconnect,** which is the main difference from many shared bus architecture.




5-channel Interconnect includes:

- Read Address Channel
- Read Data Channel
- Write Address Channel
- Write Data Channel
- Write Response Channel

Arrows in the figure show the directions of main information sent. It's good to know that each channel has a **hand-shaking pair**(valid & ready) that communicates bidirectionally. This will be illustrated soon.

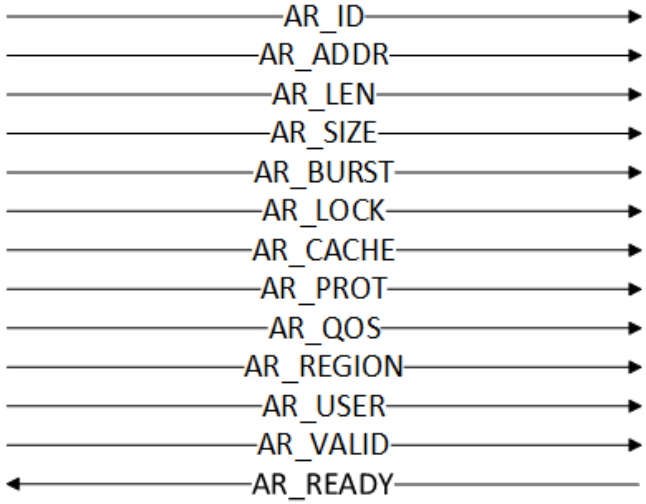
In general, the port sends out Read Address, Write Address and Write Data and receives Read Data and Write Response is the **Master Port**; and the port receives Read Address, Write Address and Write Data and sends out Read Data and Write Response is the **Slave Port**. In this simple case, the port on Master Module is the Master Port and the port on Slave Module is the Slave Port. But when things get complicated and one module can be both AXI Master and AXI Slave and has multiple Interconnect Ports, the only way to tell if a port is Master Port or Slave Port is finding out the directions of information sent.

**Details on 5 Channels**

**In this project, we only care about signals in bold.**
Direction convention in all figures is left as Master Port side and right as Slave Port side.
* ? means width depends on implementation

Read Address Channel (AR)

- **AR_ID [?:0]**
- **AR_ADDR [31:0]**
- **AR_LEN [7:0]**
- **AR_SIZE [2:0]**
- **AR_BURST [1:0]**
- AR_LOCK
- AR_CACHE [3:0]
- AR_PORT [2:0]
- AR_QOS [3:0]
- AR_REGION [3:0]
- AR_USER [?:]
- **AR_VALID**
- **AR_READY**




AR_ID: Read transaction ID
AR_ADDR: Read address (32 bits in this project)
AR_LEN: Read burst length
Support burst length 0-256 in INCR mode and 0-16 in all other modes
Burst length = AR_LEN + 1;
(RRAM Block doesn't need burst, so this is always 8'b0.)
AR_SIZE: Read word size
3'b000: 1 byte
3'b001: 2 bytes
3'b010: 4 bytes
3'b011: 8 bytes
3'b100: 16 bytes
3'b101: 32 bytes

3’b110: 64 bytes
3’b111: 128 bytes
(This project can only afford 1,2,4 bytes because of 32-bit bus.)

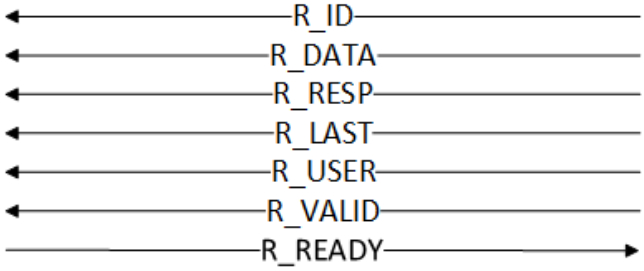
AR_BURST: Read burst mode
2’b00: FIXED - same address
2’b01: INCR - incremental addresses
2’b10: WRAP - incremental addresses, wrap around if reaches the highest
2’b11: Reserved
(RRAM Block doesn’t need burst, so this is always 2’b00.)

AR_VALID & AR_READY: Read address hand-shaking pair

---

Read Data Channel (R)

- **R_ID** **[?:0]**
- **R_DATA** **[31:0]**
- **R_RESP** **[1:0]**
- **R_LAST**
- R_USER [?:0]
- **R_VALID**
- **R_READY**




R_ID: Read transaction ID (same as AR_ID, opposite direction)

R_DATA: Read data (32 bits in this project)

R_RESP: Read Response
2’b00: OKAY - Normal access success
2’b01: EXOKAY - Exclusive access success
2’b10: SLVERR - Slave error
2’b11: DECERR - Decode error
(RRAM Block only supports 2’b00(OKAY).)

R_LAST: Read Last
Assert high with the last word in a read burst

R_VALID & R_READY: Read data hand-shaking pair

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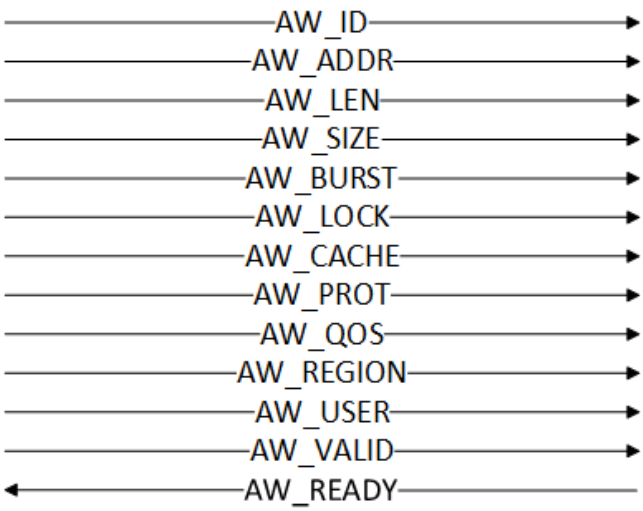
Write Address Channel (AW)

- **AW_ID** **[?:0]**
- **AW_ADDR** **[31:0]**
- **AW_LEN** **[7:0]**
- **AW_SIZE** **[2:0]**
- **AW_BURST** **[1:0]**
- AW_LOCK
- AW_CACHE [3:0]
- AW_PORT [2:0]



- AW_QOS [3:0]
- AW_REGION [3:0]
- AW_USER [?:]
- **AW_VALID**
- **AW_READY**

AW_ID: Write transaction ID
AW_ADDR: Write address (32 bits in this project)
AW_LEN: Write burst length
(Same scheme as AR_LEN)
AW_SIZE: Write word size
(Same scheme as AR_SIZE)
AW_BURST: Write burst mode
(Same scheme as AR_BURST)
AW_VALID & AW_READY: Write address hand-shaking pair

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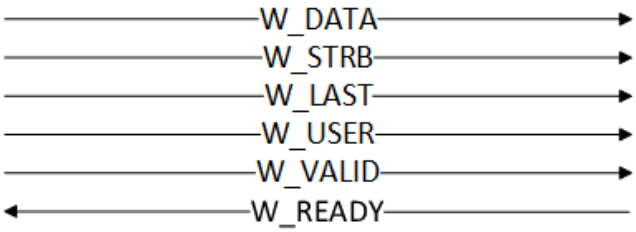
Write Data Channel (W)




- **W_DATA [31:0]**
- **W_STRB [4:0]**
- **W_LAST**
- W_USER [?:0]
- **W_VALID**
- **W_READY**

W_DATA: Write data (32 bits in this project)
W_STRB: Write strobe (4 bits in this project)
Write byte valid, active high
W_LAST: Write last
Assert high with the last word in a write burst
W_VALID & W_READY: Write data hand-shaking pair

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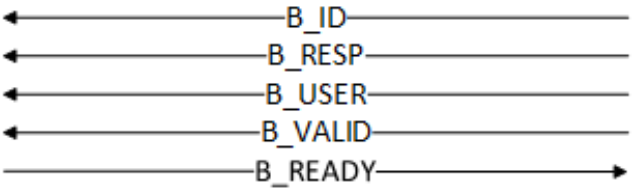
Write Response Channel (B)



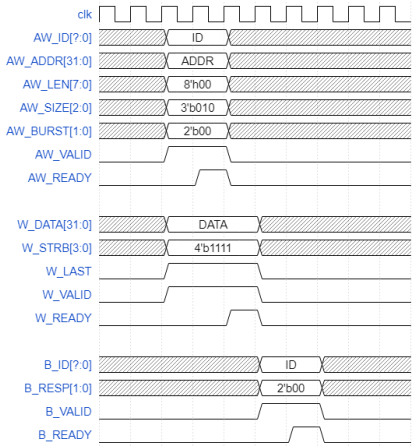

- **B_ID [?:0]**
- **B_RESP [1:0]**
- B_USER [?:0]
- **B_VALID**
- **B_READY**

B_ID: Write transaction ID (same as AW_ID, opposite direction)
B_RESP: Write response
(Same scheme as R_RESP)
B_VALID & B_READY: Write response hand-shaking pair

## Transactions and Timing Diagram

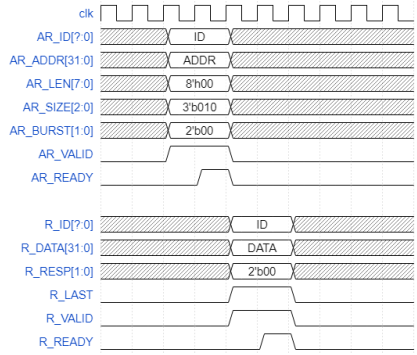
**Single write transaction**

This is the timing diagram of writing a single 32-bit word to a specific address. First, address and transaction information is confirmed through hand-shaking. Address and all transaction information, including AW_LEN, AW_SIZE and AW_BURST have to be held until AW_VALID and AW_READY are both high. Then data is written to the address when W_VALID and W_READY are both high. So, data has to be held until this happens. After data written, Slave Module sends back write response.



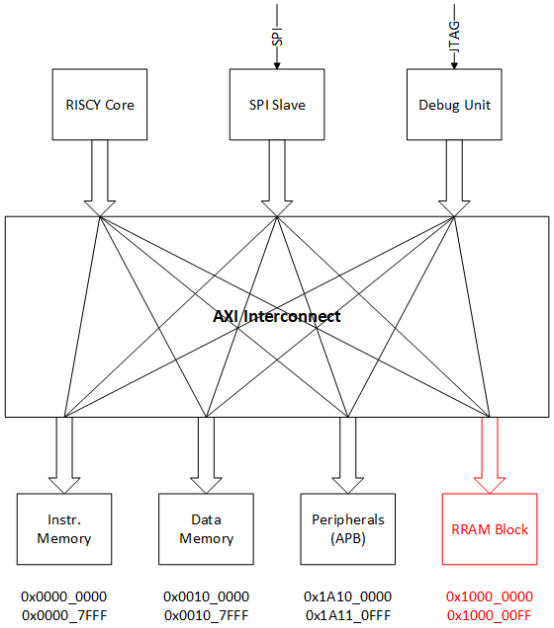

**Single read transaction**

This is the timing diagram of reading a single 32-bit word from a specific address. First, address and transaction information is confirmed through hand-shaking. Address and all transaction information, including AR_LEN, AR_SIZE and AR_BURST have to be held until AR_VALID and AR_READY are both high. Then, Slave Module sends back data and read response.




## Multiple Masters and Slaves Interconnect

Single master-slave pair is rare in real design, since it's not very extensible. Most design using AXI bus has multiple Masters and multiple Slaves and requires every Master has access to every Slave. So, an AXI Interconnect Block is needed for routing between all Masters and Slaves, like the one shown below.




This figure shows the AXI Architecture in Pulpino. Here it has three AXI Master (RISCY Core, SPI and JTAG) and four Slave Blocks (Instruction Memory, Data Memory, Peripheral Bus and RRAM Block, which can be more). The AXI Interconnect Block connects all three Masters and all four Slaves. So, as you can see, the AXI Interconnect Block has three Slave Ports (Arrow towards inside) and four Master Ports (Arrow towards outside). Inside the Interconnect Block are address decoders, multiplexers and buffers that direct transactions from

Master to Slave and responses back from Slave to Master. The way achieves this is **Memory Mapping**. Each Slave is mapped to a specific range of address (as shown in the figure), and Master can access specific Slave through that range of address. For example, address 0x0000_000C accesses something inside Instruction Memory, and address 0x0010_0010 accesses something inside Data Memory. What is actually accessed depends on the design of the Slave Module. In this system, 0x0000_000C accesses the fourth word (32 bits) in Instruction Memory, and 0x0010_0010 accesses the fifth word (32 bits) in Data Memory. This is the **Memory Mapping** feature of AXI.

# AXI Tile Interface Memory Map

| Address Name | Width | | Address |
|---|---|---|---|
| R_SM_WRITE_CYCLES | [31:0] | | 0x1000_0000 |
| R_DL_ADDRESS | [31:0] | | 0x1000_0004 |
| R_DL_CONTROL | [31:0] | | 0x1000_0008 |
| R_WL_DAC_DATA | [31:0] | | 0x1000_000C |
| R_WL_ADDRESS | [31:0] | | 0x1000_0010 |
| R_WL_CONTROL | [31:0] | | 0x1000_0014 |
| R_BL_ADDRESS | [31:0] | | 0x1000_0018 |
| R_BL_CONTROL | [31:0] | | 0x1000_001C |
| R_ANALOG_CONFIG | [31:0] | | 0x1000_0020 |
| R_WRITE_CONFIG | [31:0] | | 0x1000_0024 |
| D_SM_START_READ | pulse | wo | 0x1000_0060 |
| D_SM_START_WRITE | pulse | wo | 0x1000_0064 |
| D_SM_WRITE_DONE | [0:0] | ro | 0x1000_0068 |
| D_SM_EOC | [0:0] | ro | 0x1000_006C |
| READ_BURST_LENGTH | [5:0] | | 0x1000_0070 |
| READ_BURST_ADDR | [31:0] | | 0x1000_0074 |
| READ_BURST_OFFSET | [5:0] | | 0x1000_0078 |
| READ_BURST_START | pulse | wo | 0x1000_007C |
| WRITE_BURST_LENGTH | [2:0] | | 0x1000_0080 |
| WRITE_BURST_ADDR | [31:0] | | 0x1000_0084 |
| WRITE_BURST_OFFSET | [2:0] | | 0x1000_0088 |
| WRITE_BURST_START | pulse | wo | 0x1000_008C |
| COMPUTE_AUTOMATION | [0:0] | | 0x1000_0090 |
| READ_DAC_RESET | pulse | wo | 0x1000_0094 |
| READ_BURST_DONE | [0:0] | ro | 0x1000_0098 |
| WRITE_BURST_DONE | [0:0] | ro | 0x1000_009C |
| ADC_DATA[7:0] | [31:0] | ro | 0x1000_00C0 - 0x1000_00DC |
| READ_DAC_INPUT[64] | [31:0] | | 0x1000_0100 - 0x1000_01FC |
| | | | |
| | | TILE 1 | 0x1000_0200 - 0x1000_03FC |
| | | TILE 2 | 0x1000_0400 - 0x1000_05FC |
| | | TILE 3 | 0x1000_0600 - 0x1000_07FC |

# Burst Control Operating Manual

## READ BURST CONTROL

Read burst means burst transfer of data from data memory to DAC input registers

### Registers Specification

**READ_BURST_LENGTH**:

The actual burst length is READ_BURST_LENGTH + 1, this complies with the specification of AXI protocol. The valid range of READ_BURST_LENGTH is 0 to 63, corresponding to bursting 1 word to 64 words. It is the programmers' responsibility to keep the value in the valid range to avoid any side effects.

**READ_BURST_ADDR**:

READ_BURST_ADDR specifies the start address in data memory being read from.

**READ_BURST_OFFSET**:

READ_BURST_OFFSET dictates the starting point of writing READ_DAC_INPUT registers array. READ_BURST_OFFSET is reseted to 0, meaning the access always starts from the beginning of the array. Any other value would shift the starting point towards the end of the array by that amount. The valid range of READ_BURST_OFFSET is 0 to 63. If a burst exceeds the physical boundary of the registers array (which is 64), access rolls back to the beginning of the array. It is the programmer's responsibility to keep the value in the valid range and clearly aware of the effect of rolling back in burst transaction, since it is not a usual scenario and usually caused by programming bugs.

**READ_BURST_START**:

READ_BURST_START is the start trigger address of the read burst. Any stores toward this address, regardless of the value being stored, can start a read burst transfer.

**READ_BURST_DONE**:

Done signal is set to 1 after each read burst transfer finishes. It will automatically reset to 0 by the next read burst start signal (READ_BURST_START).

### Pseudo-codes

```
        store <burst length>   READ_BURST_LENGTH
        store <start address>   READ_BURST_ADDR
        store <offset>   READ_BURST_OFFSET
        store <any value>   READ_BURST_START
check:  load READ_BURST_DONE   R1
        branch R1 == 0 check
        <subsequent instructions>
```

## WRITE BURST CONTROL

Write burst means burst transfer of data from ADC output registers to data memory

### Registers Specification

**WRITE_BURST_LENGTH**:

The actual burst length is WRITE_BURST_LENGTH + 1, this complies with the specification of AXI protocol. The valid range of WRITE_BURST_LENGTH is 0 to 7, corresponding to bursting 1 word to 8 words. It is the programmer's responsibility to keep the value in the valid range to avoid any side effects.

**WRITE_BURST_ADDR**:

WRITE_BURST_ADDR specifies the start address in data memory being written to.

**WRITE_BURST_OFFSET**:

WRITE_BURST_OFFSET dictates the starting point of reading ADC_DATA registers array. WRITE_BURST_OFFSET is reseted to 0, meaning the access always starts from the beginning of the array. Any other value would shift the starting point towards the end of the array by that amount. The valid range of WRITE_BURST_OFFSET is 0 to 7. If a burst exceeds the physical boundary of the registers array (which is 8), access rolls back to the beginning of the array.
It is the programmer's responsibility to keep the value in the valid range and clearly aware of the effect of rolling back in burst transaction, since it is not a usual scenario and usually caused by programming bugs.

**WRITE_BURST_START**:

WRITE_BURST_START is the start trigger address of the write burst. Any stores toward this address, regardless of the value being stored, can start a write burst transfer.

**WRITE_BURST_DONE**:

Done signal is set to 1 after each write burst transfer finishes. It will automatically reset to 0 by the next write burst start signal (WRITE_BURST_START).

### Pseudo-codes

```
        store <burst length>   WRITE_BURST_LENGTH
        store <start address>   WRITE_BURST_ADDR
        store <offset>   WRITE_BURST_OFFSET
        store <any value>   WRITE_BURST_START
check:  load WRITE_BURST_DONE   R1
        branch R1 == 0 check
        <subsequent instructions>
```

## MAC OPERATION EXAMPLE

(The following sequence of instructions is not optimized to achieve best performance. Reordering some instructions can hide latency.)

### Pseudo-codes

```
        store <read burst length>   READ_BURST_LENGTH       #Configure read burst
        store <read start address>   READ_BURST_ADDR
        store <read offset>   READ_BURST_OFFSET
        store <any value>   READ_BURST_START                #Start read burst
chk_r:  load READ_BURST_DONE   R1
        branch R1 == 0 chk_r                                #Read burst finishes
        store <any value>   D_SM_START_READ                 #Start conversion
chk_c:  load D_SM_EOC   R1
        branch R1 == 0 chk_c                                #Conversion finishes
        store <write burst length>   WRITE_BURST_LENGTH     #Configure write burst
        store <write start address>   WRITE_BURST_ADDR
        store <write offset>   WRITE_BURST_OFFSET
        store <any value>   WRITE_BURST_START               #Start write burst
chk_w:load WRITE_BURST_DONE   R1
        branch R1 == 0 chk_w                                #Write burst finishes
        <subsequent instructions>
```

## OPERATION AUTOMATION

There is an automation function in the burst control that can start the conversion right after the preceding read burst finishes and start the write burst right after the preceding conversion

finishes. In the automation mode, tile doesn't have to communicate with the host core until the whole operation (ex. MAC) finishes.

### Registers Specification

**COMPUTE_AUTOMATION**:

Default value of COMPUTE_AUTOMATION is 0, meaning the automation function is off. To turn on the automation mode, set COMPUTE_AUTOMATION to 1.

### Pseudo-codes

```
        store 1   COMPUTE_AUTOMATION
        store <read burst length>   READ_BURST_LENGTH       #Configure read burst
        store <read start address>   READ_BURST_ADDR
        store <read offset>   READ_BURST_OFFSET
        store <write burst length>   WRITE_BURST_LENGTH     #Configure write burst
        store <write start address>   WRITE_BURST_ADDR
        store <write offset>   WRITE_BURST_OFFSET
        store <any value>   READ_BURST_START                #Start read burst
check:  load WRITE_BURST_DONE   R1
        branch R1 == 0 check                                #Operation finishes
        <subsequent instructions>
```

# SPI datasheet

This datasheet applies to SPI Slave in Pulpino

## Input & Output Ports

| | | |
|---|---|---|
| input | spi_clk_i | - SPI clock |
| input | spi_cs_i | - chip select (active low) |
| input | spi_sdi0_i | - serial data input (a.k.a MOSI) |
| input | spi_sdi1_i | - serial data input used in QSPI |
| input | spi_sdi2_i | - serial data input used in QSPI |
| input | spi_sdi3_i | - serial data input used in QSPI |
| output | spi_sdo0_i | - serial data output (a.k.a MISO) |
| output | spi_sdo1_i | - serial data output used in QSPI |
| output | spi_sdo2_i | - serial data output used in QSPI |
| output | spi_sdo3_i | - serial data output used in QSPI |
| output [1:0] | spi_mode_o | - SPI mode |

## SPI Mode (Status)

Output port spi_mode_o indicates the status of data transfer.
2'b00: standard transmitting
2'b01: standard receiving
2'b10: QSPI transmitting
2'b11: QSPI receiving

## Configurable Registers

reg0 [7:0]: bit 0 enables QSPI (active high)
- reset to 0

reg1 [7:0]: number of dummy cycles between MOSI and MISO
- reset to 32

reg2 [7:0]: wrap length (lower 8 bits)
- reset to 0

reg3 [7:0]: wrap length (higher 8 bits)
- reset to 0

## SPI Commands

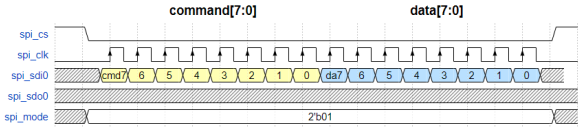
All SPI commands in this design are 8 bits.
8'h01: write reg0
8'h02: write memory and memory mapped peripherals

8’h05: read reg0
8’h07: read reg1
8’h0B: read memory and memory mapped peripherals
8’h11: write reg1
8’h20: write reg2
8’h21: read reg2
8’h30: write reg3
8’h31: read reg3

## Standard SPI Transactions

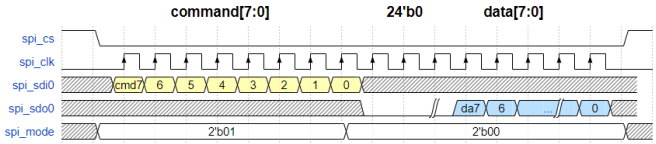
**Write configurable registers**:

Stream in command and data in sequence (MSB first) after assert spi_cs. This type of transaction only accepts 8-bit command and 8-bit data, since the registers are all 8-bit.



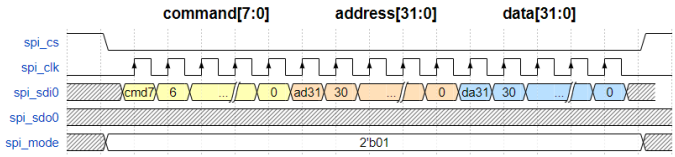

**Read configurable registers**:

Stream in command (MSB first) after assert spi_cs. This type of transaction only accepts 8-bit command. After the last bit of command is received, 32-bit data streams out on spi_sdo0(MISO). Since each register has only 8 bits, the first 24 bits of data are all 0’s. There is no dummy cycles between command and data.

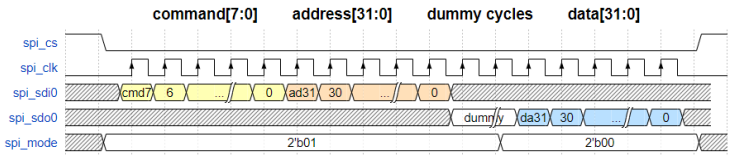



**Write memory and memory mapped peripherals**:

Stream in command(8’h02), address and data in sequence (MSB first) after assert spi_cs. This type of transaction only accepts 8-bit command, 32-bit address and 32-bit data.



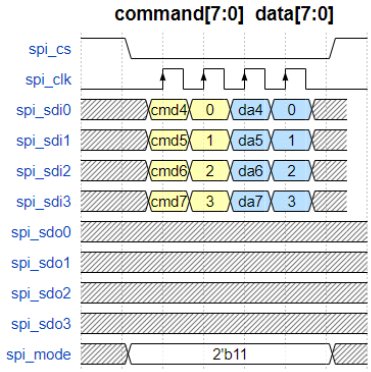
**Read memory and memory mapped peripherals**:
Stream in command(8'h0B), address in sequence (MSB first) after assert spi_cs. This type of transaction only accepts 8-bit command and 32-bit address. After the last bit of address is received, several dummy cycles occur on spi_sdo0(MISO) before 32-bit data streams out. spi_mode also tells when data is valid. Notice that the number of dummy cycles is the number stored in reg1 plus 1.



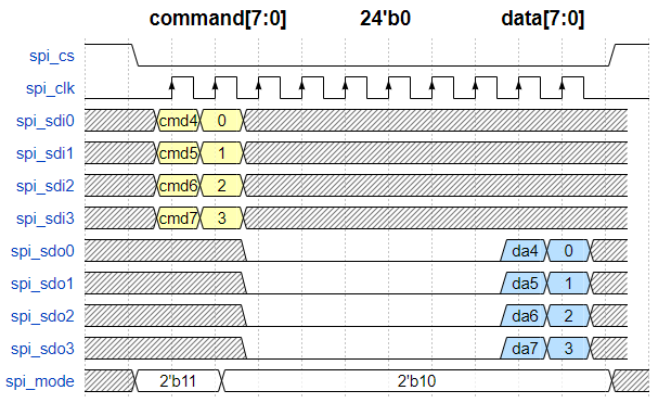

## QSPI Transactions

The only difference between standard SPI transaction and QSPI transaction is that with QSPI 4 bits are streamed in or out every cycle.

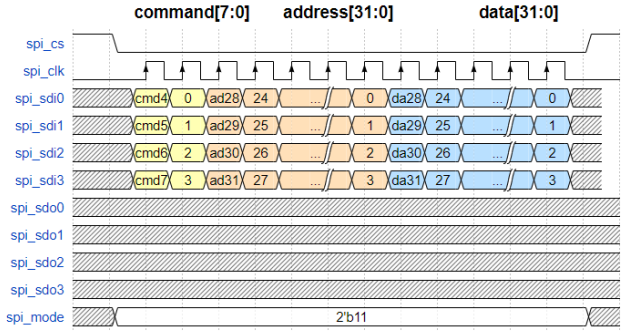
**Write configurable registers**:



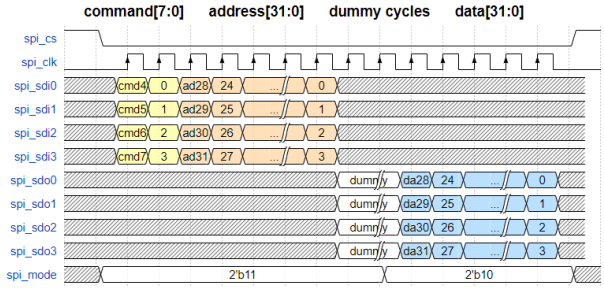

**Read configurable registers**:




**Write memory and memory mapped peripherals**:




**Read memory and memory mapped peripherals**:



# 16K 1T1R RRAM CIM Module

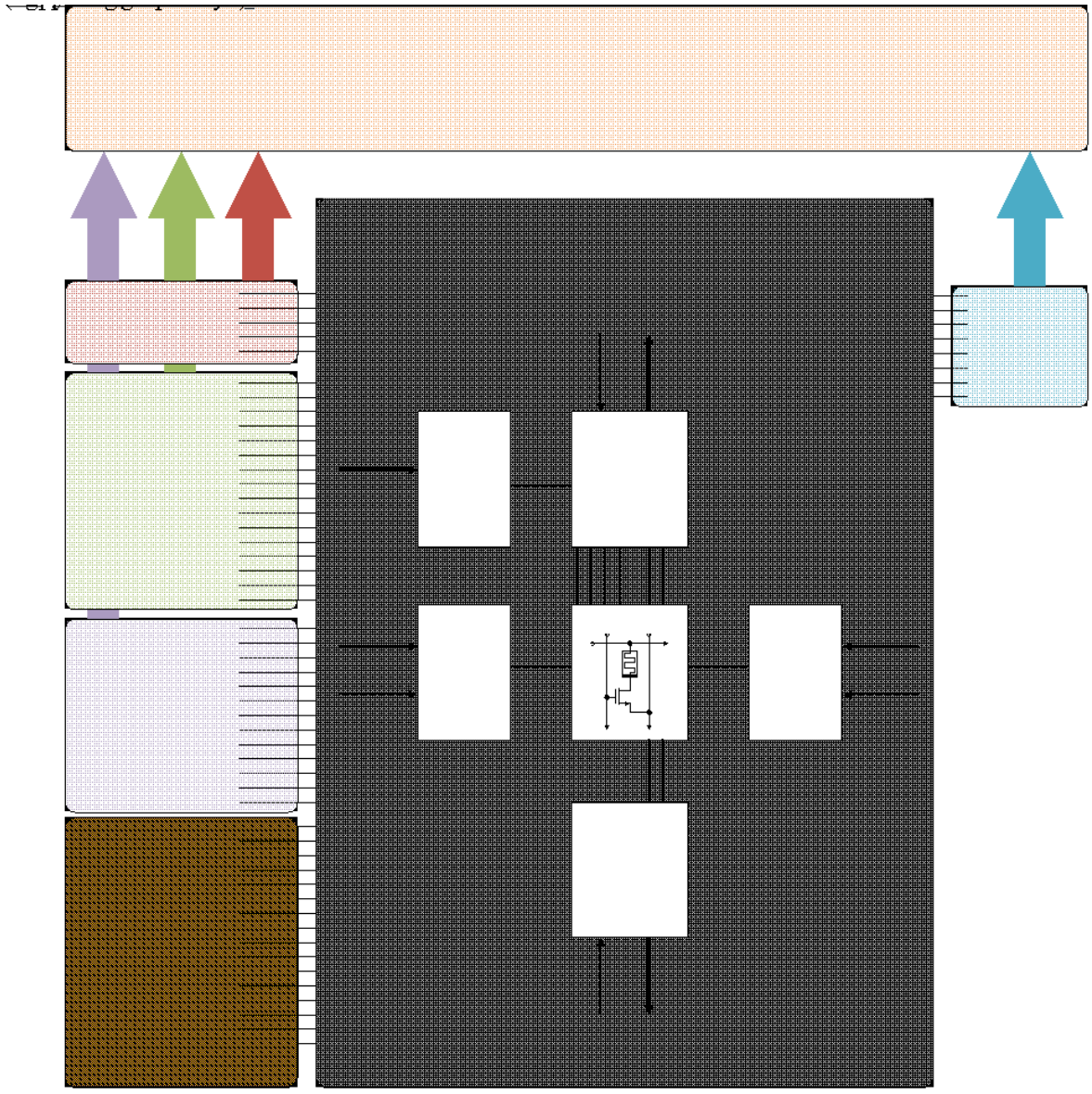


*Figure 1. Mixed-signal tile peripheral.*

The 16K 1T1R RRAM CIM module is designed to operate as a peripheral of the RISCV Pulpino. The module consists of two parts, namely the “mixed-signal tile” and the “mixed-signal digital interface”. The mixed-signal tile consists of DACs, ADCs, and analog multiplexors that interface to the crossbar. The mixed-signal digital interface consists of memory mapped registers to configure the tile and read and write state machines to provide timing to drive the tile operations. This section details the design and operation of the CIM module.

## Mixed-Signal Tile

The mixed-signal tile consists of a 256 x 64 1T1R RRAM crossbar array and the circuits that interface to the array. The circuits are described in the following sections: Drive Line, Bit Line, and Word Line.

## Drive Line

The drive line circuitry interfaces to the rows of the crossbar array. Each row of the array is physically connected to the top electrode of each RRAM bitcell in that row. The drive line consists of 256 slices and a global write voltage select block shown in the figure below. Each slice consists of a 1b pulse DAC and read, write, and ground switches. The global write voltage select block consists of 3 one-hot switches to select the appropriate write voltage.

The drive line supports 3 modes of operation: read, write, and idle. The modes are determined by the switches enabled by signals “a”, “b” and “c” shown below. The read enable switch is a 3V I/O NMOS transistor that connects the DAC to the crossbar during read and protects the DAC during write when the drive line voltage may exceed VDDL = 1.2V. All read enable switches activate at once under control of a global level shifter. During read, switch “a” is selected and switches “b” and “c” are off or disabled. The write enable switch connects the global write voltage select block to the crossbar during read through a 3V I/O transmission gate. The level shifter is local to each slice. The actual write voltage is further selected by the 3 one-hot switches (“f”, “g”, “h”) in the write voltage select block. During write, switch “b” is selected and switches “a” and “c” are disabled. The idle state of the drive line is 0V or GND. To enable idle mode, switch “c” is on and switches “a” and “b” are off or disabled. The DAC logic switches are detailed in the next section.

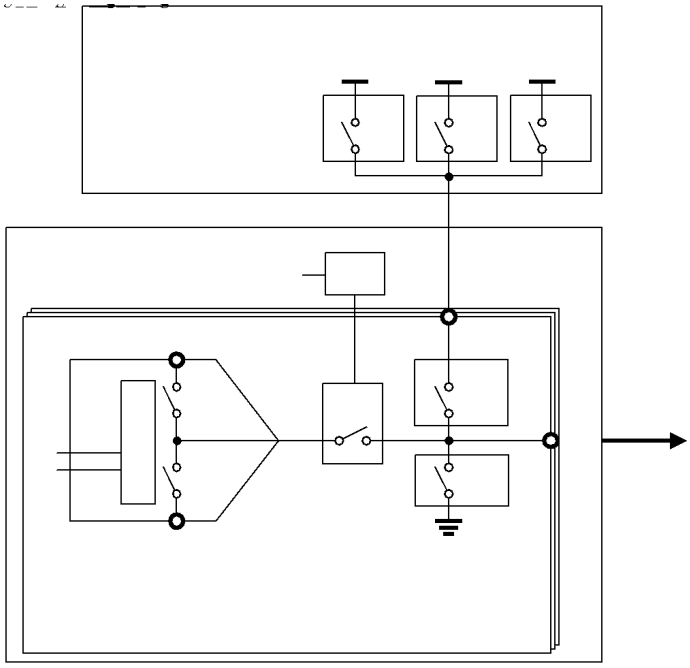


*Figure 2. Drive line conceptual diagram.*

## Drive Line 1bit Pulse DAC

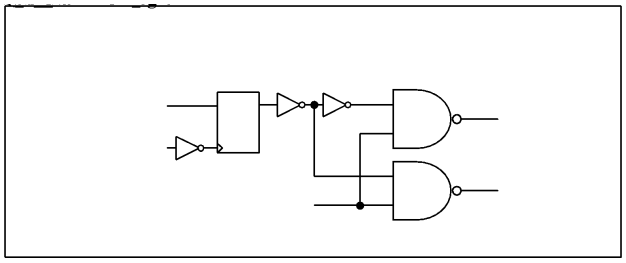


*Figure 3. Drive line pulse DAC schematic.*

The logic of the drive line 1b pulse DAC drives two 1.2V PMOS switches between VCM and VREAD. Since the source of the 1T1R bitcell is connected to VCM during read mode, the 1b pulse DAC toggles the row with the appropriate read voltage amplitude (VREAD-VCM). The pulse DAC input, D_DL_DSTREAM, is a 1b serialized bit stream generated in the mixed-signal digital interface block from an 8-bit input word. The DFF with negative clk latches the serialized bit stream into the tile clock domain with a ¼ clock cycle delay.

During read mode, the read enable switch connects all 256 1b pulse DACs to the crossbar rows as mentioned above. During single read mode, the signal D_DL_DSTREAM_EN is used to enable the selected pulse DAC while tri-stating all unused DACs. This feature was added to mitigate extraneous leakage currents that could arise due to differences in VCM between the rows and “VCM” presented by the column virtual ground regulator.

## Drive Line Control Register

| Drive Line Control Register | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| One-hot Write Voltage Select | | | Global Read | DSTREAM Address Decoder | | | Write Switch Address Decoder | | | Ground Switch Address Decoder | | |
| [12] | [11] | [10] | [9] | [8] | [7] | [6] | [5] | [4] | [3] | [2] | [1] | [0] |
| VFORM Select | VSET Select | VRESET Select | Read Enable | DSTREAM Enabl | DSTREAM SEL[1] | DSTREAM SEL[0] | Write Enable | Write SEL[1] | Write SEL[0] | Ground Enable | Ground SEL[1] | Ground SEL[0] |

*Table 1. Drive line control register*

The control of the switches of the drive line is provided by an 8b row address register and the drive line control register. The control register consists of four one-hot select bits (bits 12-9) and the control bits for three address decoders (bits 8-0). The address decoders are explained in detail in the mixed-signal digital interface section.

## Bit Line

The bit line circuitry interfaces to the columns of the crossbar array. Each column of the array is physical connected to the source of each transistor in the bitcells of that column. The columns of the array are multiplexed by two, meaning two columns share one TIA and ADC. The bit line circuitry is split among the top and bottom of the array in two sections where each section consists of 16 slices for a total of 32 slices (64/2). The top slices include the word line circuitry and will be discussed in the next section. The bit line slice consists of a pseudo-neuron (TIA + ADC), and read, write and idle switches.

The bit line supports 3 modes of operation: read, write, and idle. The modes are determined by the switches enabled by signals “a” – “f” shown below. Further due to the multiplexed nature, the bit line is operated in an even/odd fashion. The following describes the operations from the “even” perspective but is easily extended to the “odd” case.

The read enable switch is a 3V I/O NMOS with local level shifter that connects the pseudo-neuron (TIA + ADC) to the crossbar rows during read and protects the pseudo-neuron during write when the bit line voltage may exceed VDDL = 1.2V. During read (even), switch “e” is enabled and all other switches are off or disabled. The write enable switch is a 3V I/O transmission gate with local level-shifter and connects the crossbar column to the reset voltage V_RESET during the reset write operation. During write (even), switch “a” is enabled and all other switches are disabled. The idle state of the bit line is 0V or GND. To enable idle mode, switch “c” is enabled and all other switches are disabled.

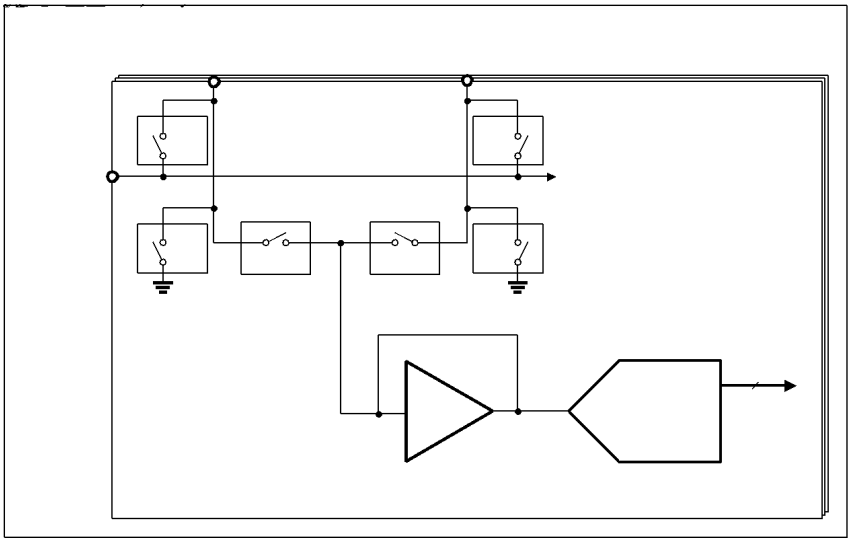


*Figure 4. Bit line (bottom) conceptual diagram.*

## Bit Line Control Register

| Bit Line Control Register | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| **Write Switch Address Decoder** | | | **Ground Switch Address Decoder** | | | **Even/Odd ADC Switch Address Decoder** | | | |
| [9] | [8] | [7] | [6] | [5] | [4] | [3] | [2] | [1] | [0] |
| Write Enable | Write SEL[1] | Write SEL[0] | Ground Enable | Ground SEL[1] | Ground SEL[0] | Even Enable | Odd Enable | Even/Odd SEL[1] | Even/Odd SEL[0] |

*Table 2. Bit line control register*

The control of the switches of the bit line is provided by an 6b row address register and the bit line control register. The control register consists the control bits for three address decoders (bits 9-0). The address decoders are explained in detail in the mixed-signal digital interface section.

## Trans-Impedance Amplifier (TIA)

TIA senses column current and converts it to voltage. The maximum allowable current is 3 μA and 45 μA for single and MAC operation, respectively. Negative feedback with a pass transistor reduces input resistance so that input pole seen from column becomes large and settling time remains short. The virtual ground from the feedback loop is strongly tied to common-mode voltage. To maintain stability in TIA, bleeding current is required, which is 10 μA. Sensed column current with bleeding current pass through the pass transistor. The total current is multiplied by resistor and becomes voltage information. Since the next stage, ADC, has a finite sampling capacitor value, the output resistance has to be as much as small. However, if the resistance is small, output voltage becomes small as well. To improve settling time and reduce a RC time constant at the output, amplified current from the pass transistor is necessary so that the output resistance becomes small. In order to achieve better settling time, a replicated pass transistor is implemented. For the single read and MAC read mode, the output resistor is 20 kΩ

and 5 kΩ. When the TIA is not used, it can be turned off using TIA_EN signal. All bias signals are off, and no current flows through TIA. The RC time constant of the settling time at the output for single read is 20k*CLOAD. On the other hand, the RC time constant of that for MAC read is 5k*CLOAD. Since the RC time constant of single read is larger than that of MAC read, the clock speed for single read is needed to be slow.

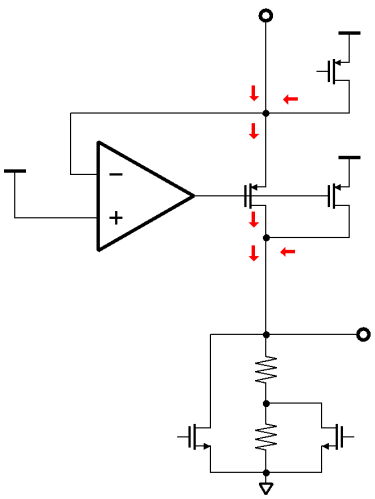


*Figure 5. Trans-impedance amplifier schematic.*

| | Single Read | | | MAC Read | | |
|---|---|---|---|---|---|---|
| **Load** | 20K | | | 5K | | |
| **Offset** | 400mV | | | 100mV | | |
| | **Input Current** | **Output Votlage** | **Total Current** | **Input Current** | **Output Votlage** | **Total Current** |
| **MAX** | 3uA | 520mV | 26uA | 45uA | 550mV | 110uA |
| **MIN** | 0.3uA | 412mV | 20.6uA | 0uA | 100mV | 20uA |

*Table 3. Trans-impedance amplifier specification.*

## Bit-Serial ADC

### *Input/Output Ports*

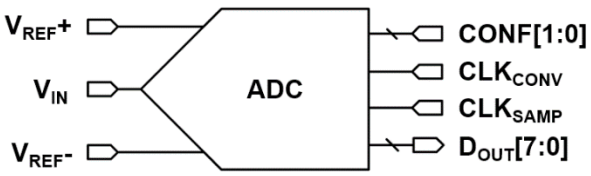



*Figure 6. Bit-serial ADC symbol.*

$V_{IN}$ is the analog input and $D_{OUT}$ is the 8-bit digital output. $CLK_{SAMP}$ and $CLK_{CONV}$ are the sampling clock and conversion clock respectively. $V_{REF}$+- are the positive and negative voltage reference for quantization. And $C_{ONF}$[1:0] is a 2-bit configuration input for timing calibration.

## *Functionality Overview*

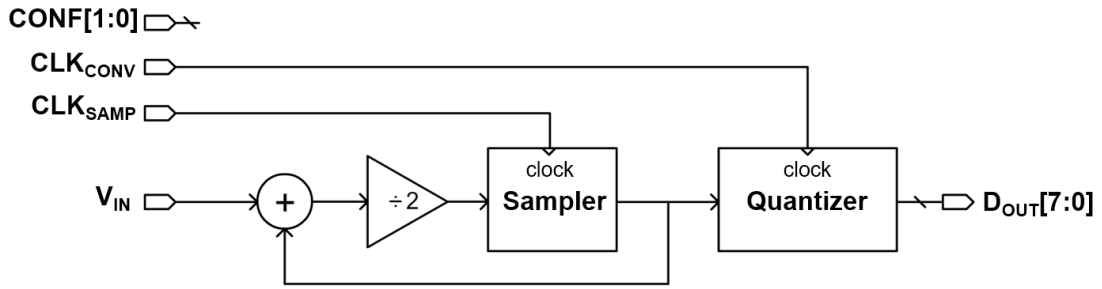



*Figure 7. Bit-serial ADC operation.*

The binary-weighted multi-cycle sampling ADC is a specialized Analog to Digital Convertor (ADC). It accepts two clock input: $CLK_{CONV}$ and $CLK_{SAMP}$. At every pos-edge of $CLK_{SAMP}$, the ADC samples $V_{IN}$ and add it to the previous sampled value, and then halves the sampled value. At every pos-edge of $CLK_{CONV}$, the ADC quantizes the current sampled value and output a corresponding digital code. The $CLK_{SAMP}$ can occur continuously many times before $CLK_{CONV}$ occurs, such that a serials of $V_{IN}$ are sampled and summed up with binary weighting. The overall behavior of the ADC can be descripted by the following expression:

$$D_{OUT} = \left\lfloor \frac{2^{-1}A_{IN}[n]+2^{-2}A_{IN}[n-1]+2^{-3}A_{IN}[n-2]+\ldots+2^{-n}A_{IN}[1]}{V_{REF}^{+}-V_{VREF}^{-}} \times 256 \right\rfloor$$

## *Circuit Schematic*

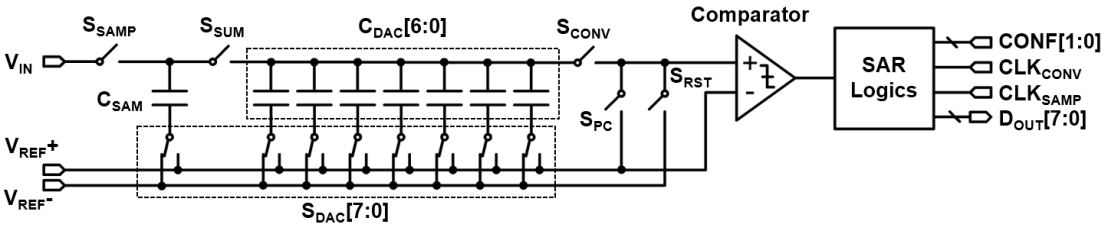



*Figure 8. Bit-serial ADC circuit schematic.*

| $C_{SAM}$ | $C_{DAC}[6]$ | $C_{DAC}[5]$ | $C_{DAC}[4]$ | $C_{DAC}[3]$ | $C_{DAC}[2]$ | $C_{DAC}[1]$ | $C_{DAC}[0]$ |
|---|---|---|---|---|---|---|---|
| 128x 1.4fF | 64x 1.4fF | 32x 1.4fF | 16x 1.4fF | 8x 1.4fF | 4x 1.4fF | 2x 1.4fF | 1x 1.4fF |

*Table 4. Bit-serial ADC C-DAC.*

The actual ADC is implemented in a modified SAR architecture. The sampler in Fig. 1 is implemented by $S_{SAMP}$ and $C_{SAM}$. And the quantizer is implemented by a C-DAC (consist of $C_{SAM}$ and $C_{DAC}[6:0]$), a comparator and the SAR logics. The SAR logics accept two clock signals ($CLK_{CONV}$ and $CLK_{SAMP}$), control $S_{DAC}[7:0]$, use successive approximation to quantize the signal on $C_{DAC}[6:0]$ and generate $D_{OUT}[7:0]$. The adder and divider in Fig. 1 are implemented by the charge-sharing between $C_{SAM}$ and $C_{DAC}[6:0]$. Fig. 4 shows the operation timing.

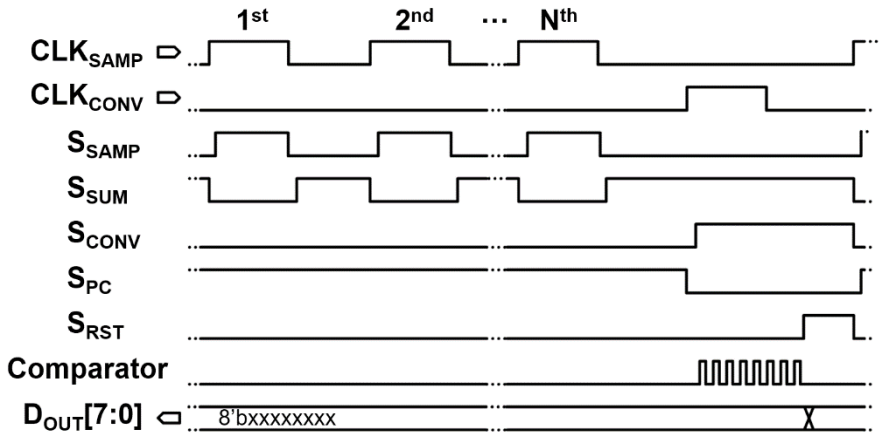



*Figure 9. Bit-serial ADC timing diagram.*

## *Tuning and Calibration*

The SAR logics use R-C delayer based asynchronous logic design. Therefore, its timing is sensitive to PVT variation. CONF[1:0] is the configuration inputs to tune the delayers and ensure correct timing. The functional description of CONF is as follow:

| CONF[1:0] | Delayer's Latency | Recommend Case |
|---|---|---|
| 00 | Long | FF corner / High Voltage |
| 01 | Moderate | TT corner & Normal Voltage |
| 1x | Short | SS corner / Low Voltage |

*Table 5. Bit-serial ADC turning and calibration settings.*

The reference voltages ($V_{REF}$+-) are also tunable. Generally, $V_{REF}$- should be shorted to ground and the voltage difference between $V_{REF}$+ and $V_{REF}$- define the maximum input voltage corresponding to the maximum code (8b'11111111). Therefore, the ADC's conversion gain can be change by tuning $V_{REF}$. More specifically, reduce $V_{REF}$+ can increase the gain of ADC, vice versa. But avoid make $V_{REF}$+ < 500mV which may significant degrade ADC's performance.

## *Specifications*

| Specification | Value (Simulated) |
|---|---|
| **Supply** | 1.2V |
| **Sampling Rate** | >40MHz (with 5Kohm $R_S$) |
| **Conversion Delay** | 20 nS |
| **Power** | 7.8 pJ/conversion (8 sampling + 1 conversion)<br>or 35uW @ 40MHz |
| **Area** | 7.68um x 210um |
| **Resolution** | 8 bits |
| **Input Range** | 0 ~ ($V_{REF}$+ - $V_{REF}$-) |
| **Effective Number of Bit** | 7.5 bit (w/ noise, w/o mismatch) |

*Table 6. Bit-wise ADC specification.*

## Word Line

The word line circuitry interfaces to the gates of the 3V I/O transistors in the 1T1R bitcells of the crossbar array. The “selector” transistor is turned fully on during read and provides current compliance during write. The word line consists of 16 slices, a global word line multiplexor, and a global 9b resistor-based segmented DAC. Each slice has 4 channel enable switches and is located at the top of the array in the bit line slices. The DAC provides fine grained potentiation steps to program the RRAM bit cells.

The word line supports 3 modes of operation: read, write, and idle. The modes are determined by the switches enabled by signals “h” – “j” shown below and by switches “a” and “b” in the word line mux. The word line mux connects the channel enable switches (1T gates) to either the 9b gate DAC or to a 3.3V reference switches “a” and “b”, a 3V I/O transmission gate and 3V I/O PMOS transistor. In each channel, a 3V I/O transmission gate connects the channel to the word line mux or a 3V I/O NMOS transistor connects the channel to ground. The switches operate in complementary, i.e. while one is on the other is off. This ensures that the gates of the bitcells are never floating. For read mode, in the word line mux, switch “b” is enabled and switch “a” is disabled. Similarly, for write mode, in the word line mux, switch “a” is enabled and switch “b” is disabled. The corresponding channels are enabled through the word line control register. The channels are inherently placed in idle mode when not selected.

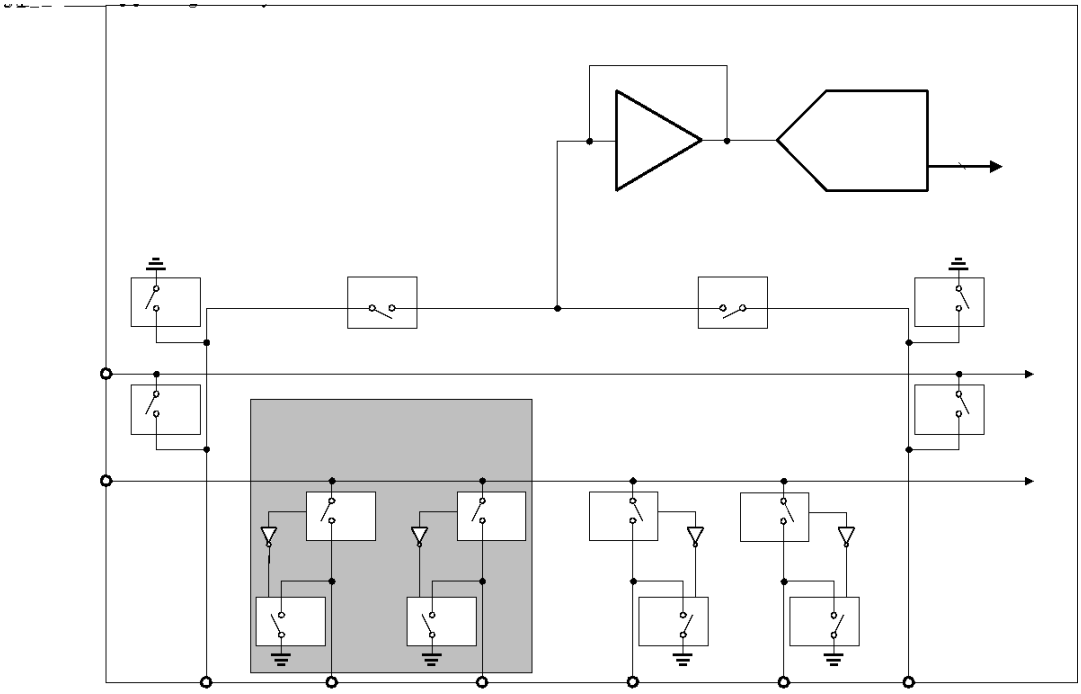


*Figure 10. Bit line (top) conceptual diagram with word line switches.*

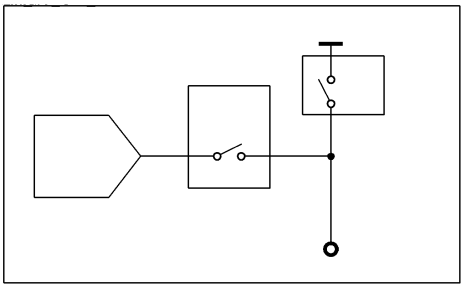


*Figure 11. Word line mux.*

## Word Line Control Register

| Word Line Control Register | | | | | |
|---|---|---|---|---|---|
| One-hot DAC | One-hot VDD | DAC/VDD Switch Address Decoder | | | |
| [5] | [4] | [3] | [2] | [1] | [0] |
| WL DAC Enable | WL VDD Enable | Even Enable | Odd Enable | Even/Odd SEL[1] | Even/Odd SEL[0] |

*Table 7. Word line control register.*

The control of the switches of the word line is provided by an 6b row address register and the bit line control register. The control register consists of two one-hot controls (bits 5,4) and the control bits for one address decoder (bits 3-0). The address decoder is explained in detail in the mixed-signal digital interface section.

## Word Line 9b Gate DAC

Gate DAC consists of a resistor-based segmented DAC and output buffer. The resistor DAC has a 4-b thermometer DAC for MSB and 5-b R-2R binary DAC for LSB. R-2R binary DAC may have a linearity issue when the worst case happens. For this reason, the LSB part is implemented with a R-2R DAC, and the MSB part is designed with a thermometer DAC. To have a thermometer operation for the MSB part, it has a thermometer-to-binary decoder. The output voltage from the resistor DAC is buffered by the output buffer to transmit the voltage to the word line. The output buffer is composed of a class-AB amplifier with a unity-gain configuration. For moderate operation in the output buffer, this requires 10 μA bias current. Operating voltage of the 9-b Gate DAC is from 0.5V to 2.9V. 1 LSB value is 4.687 mV. Since the DAC is used only in write mode, GATE DAC can be turned off to save power consumption.

## Mixed-Signal Digital Interface

The mixed signal digital interface describes “glue logic” that drives the mixed-signal tile by way of memory mapped registers to the RISCV core. The timing of the mixed signal tile is provided by separate read and write state machines. Control and address decoding are provided by memory mapped registers. The configuration of the mixed-signal tile is set by the programmer by manipulating the memory mapped registers. The table below shows the memory map for a mixed-signal tile.

| Address Name | Width | | Address |
|---|---|---|---|
| R_SM_WRITE_CYCLES | [31:0] | | 0x1000_0000 |
| R_DL_ADDRESS | [31:0] | | 0x1000_0004 |
| R_DL_CONTROL | [31:0] | | 0x1000_0008 |
| R_WL_DAC_DATA | [31:0] | | 0x1000_000C |
| R_WL_ADDRESS | [31:0] | | 0x1000_0010 |
| R_WL_CONTROL | [31:0] | | 0x1000_0014 |
| R_BL_ADDRESS | [31:0] | | 0x1000_0018 |
| R_BL_CONTROL | [31:0] | | 0x1000_001C |
| R_ANALOG_CONFIG | [31:0] | | 0x1000_0020 |
| R_WRITE_CONFIG | [31:0] | | 0x1000_0024 |
| D_SM_START_READ | pulse | wo | 0x1000_0060 |
| D_SM_START_WRITE | pulse | wo | 0x1000_0064 |
| D_SM_WRITE_DONE | [0:0] | ro | 0x1000_0068 |
| D_SM_EOC | [0:0] | ro | 0x1000_006C |
| ADC_DATA[7:0] | [31:0] | ro | 0x1000_00C0 - 0x1000_00DC |
| READ_DAC_INPUT[64] | [31:0] | | 0x1000_0100 - 0x1000_01FC |

### 4-Function Address Decoder

The 4-funciton decoder drives the switches that make the desired crossbar connections. The 4 functions are as follows: “all outputs low”, “all outputs high”, “active high decode”, and “active low decode”. In “active high decode” mode, the selected output corresponds to the decoder address and is a logical “1”. All unselected outputs are at logical “0”. In “active low decode” mode, the selected output corresponds to the decoder address and is a logical “0”. All unselected outputs are at logical “1”. The table below shows the truth table of the 4-function decoder. It contains a typical one-hot decoder but with an added inverted path and a mux to select between the two paths.

Further control is provided adding AND gates and an ENABLE signal to the output of the decoder. In this way, the activation for the decoder output can be applied from the programmer through the memory mapped registers or from the state machine through the enable signal. Both modes are setup in the write config register. Also, an extra ENABLE signal is added to the column decoders to activate even and odd modes. For example, to enable even mode, the column decoder is set to “01” and “Even Enable” bit is set to “1”. This will activate all of the even outputs of the column address decoder.

| Function Select | Decoder Output |
|---|---|
| 00 | All “0” |
| 01 | All “1” |
| 10 | Active high decode (ex. 0000010) |
| 11 | Active low decode (ex. 1111101) |

*Table 8. Truth table for 4-function address decoder.*

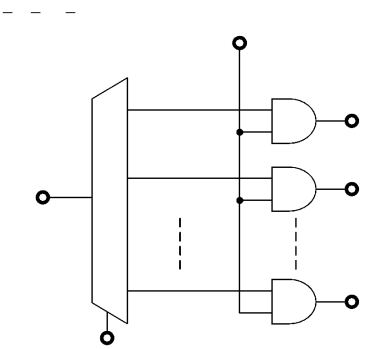


*Figure 12. Row decoder.*

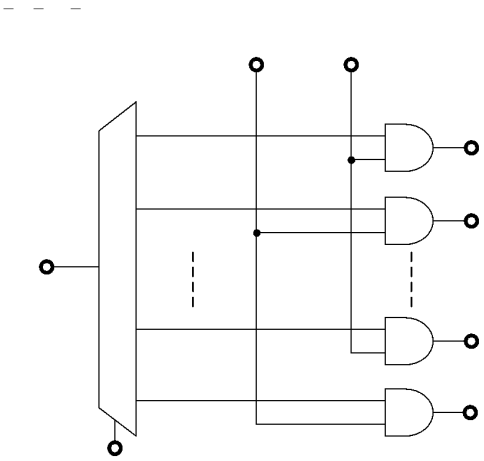


*Figure 13. Column decoder.*

## Write State Machine

TODO

## Read State Machine

TODO

## Write Configuration Register

The write configuration register is used to override the register settings during RESET, FORM and SET. Specifically, the write configuration register routes the write state machine timing signal to either the word line (RESET) or the drive line (FORM, SET). Address decoding is still required to select the desired bitcell.

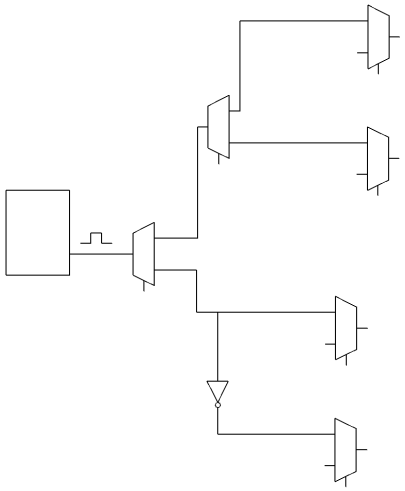


*Figure 14. Write config register signal routing.*

| Write Config Register | | | | |
|---|---|---|---|---|
| [4] | [3] | [2] | [1] | [0] |
| WL/DL Select | DL Reg/Pulse Select | WL Even/Odd | Even Reg / Pulse Select | Odd Reg / Pulse Select |

*Table 9. Write configuration register.*

## Analog Configuration Register

The analog configuration register is used to configure different settings in the TIAs, ADCs, and gate DAC. The ADC timing configuration is set by ADC_CONF[1:0], more details are found in the ADC section. The TIA is enabled by setting bit 2. Bit 3 changes the gain setting for the TIA. Details of the TIA settings can be found in the TIA section. The output buffer of the gate DAC is enables by setting bit 4. Free run mode is not implemented on this version of ASIC.

| Analog Config Register | | | | | |
|---|---|---|---|---|---|
| [5] | [4] | [3] | [2] | [1] | [0] |
| Free Run Mode | DAC Amplifier Enable | MAC Enable | TIA Enable | ADC CONF[1] | ADC CONF[0] |

*Table 10. Analog configuration register.*

# Array Operations

## Write Operations

FORM
SET
RESET

## Read Operations

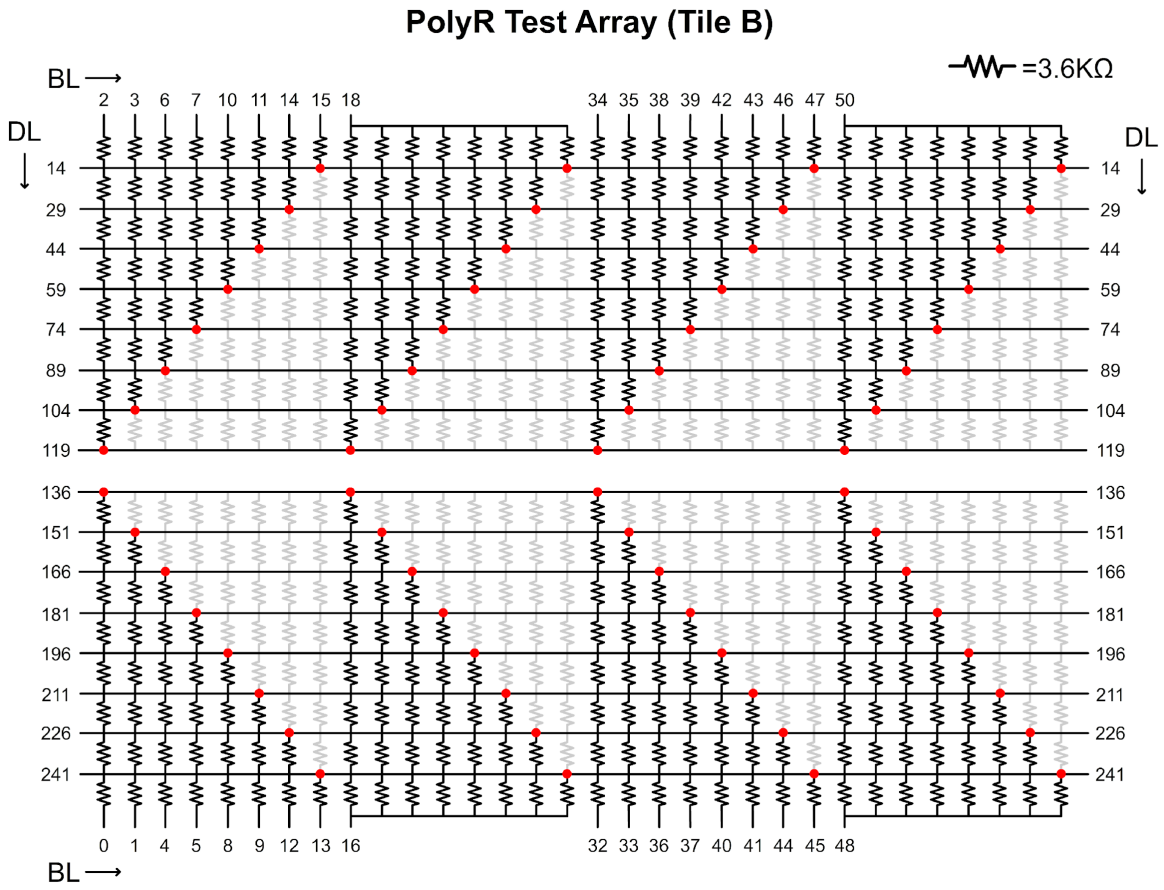
SINGLE READ
MAC READ

# Test Chip – Chip2

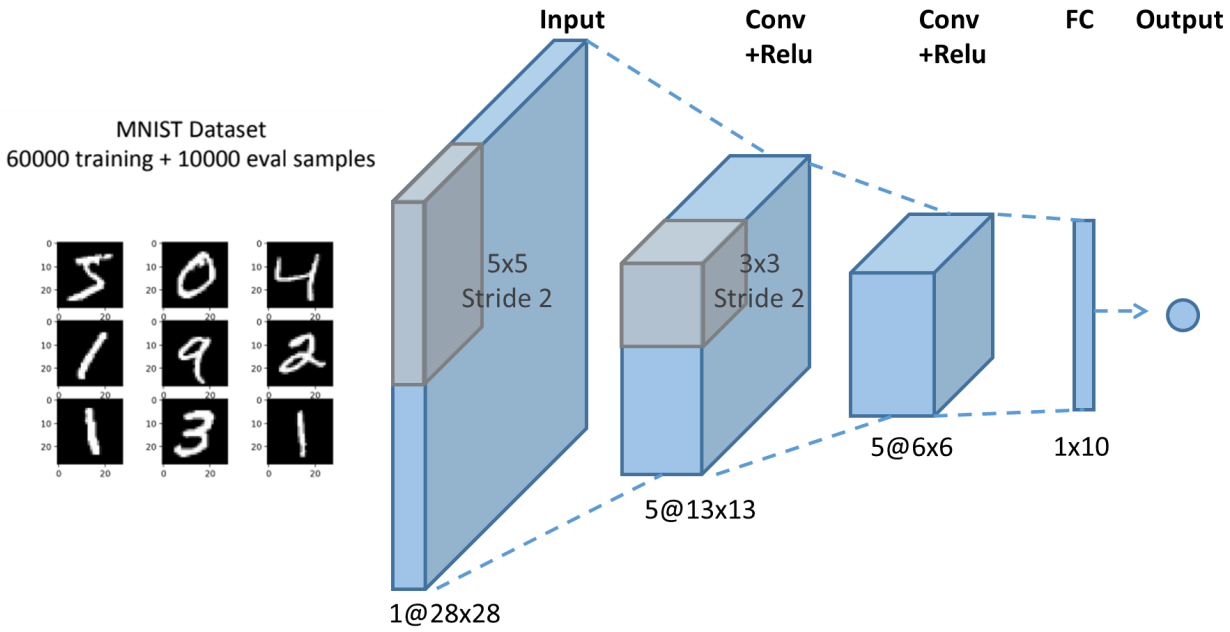
## Modifications

Tile V2A

Tile V2B



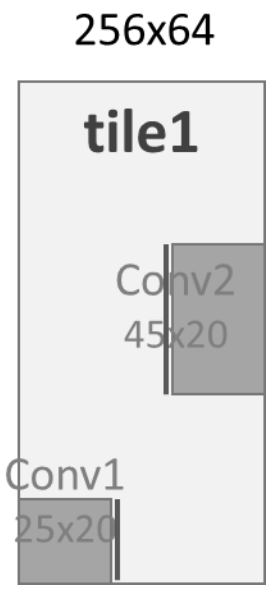

Tile V2C




| Layer | Input HxWxC | Weight K@SxRxC [stride] | Output H'xW'xK | # param |
|---|---|---|---|---|
| **CONV1** | 28x28x1 | 5@5x5x1 [2] | 13x13x5 | 125 |
| ReLU | | | | |
| **Conv2** | 13x13x5 | 5@3x3x5 [2] | 7x7x5 | 225 |
| ReLu | | | | |
| **FC** | 7x7x5 | 10@7x7x5 | 1x10 | 2,450 |
| Classifier (argmax) | | | | |
| | | | | Total 2.81K |

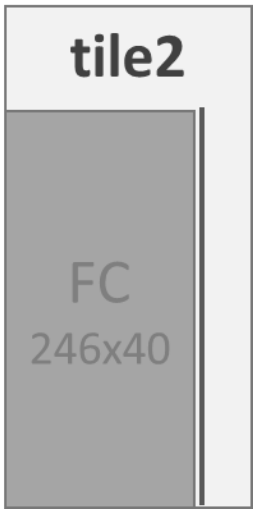
| Layer | Input HxWxC | Weight K@SxRxC [stride] | HW mapping (8b weight → 8/2 = 4 columns) |
|---|---|---|---|
| **CONV1** | 28x28x1 | 5@5x5x1 [2] | 5x5 = 25rows,<br>5x4 = 20cols @tile1 |
| ReLU | | | Digital |
| **Conv2** | 13x13x5 | 5@3x3x5 [2] | 3x3x5 = 45rows,<br>5x4 = 20cols @tile1 |
| ReLu | | | Digital |
| **FC** | 7x7x5 | 10@7x7x5<br>(+10 bias) | 7x7x5 +1=246rows,<br>10x4 = 40cols @tile2 |
| Classifier (argmax) | | | Digital |

Total 2.81K




Tile V2D

256x64

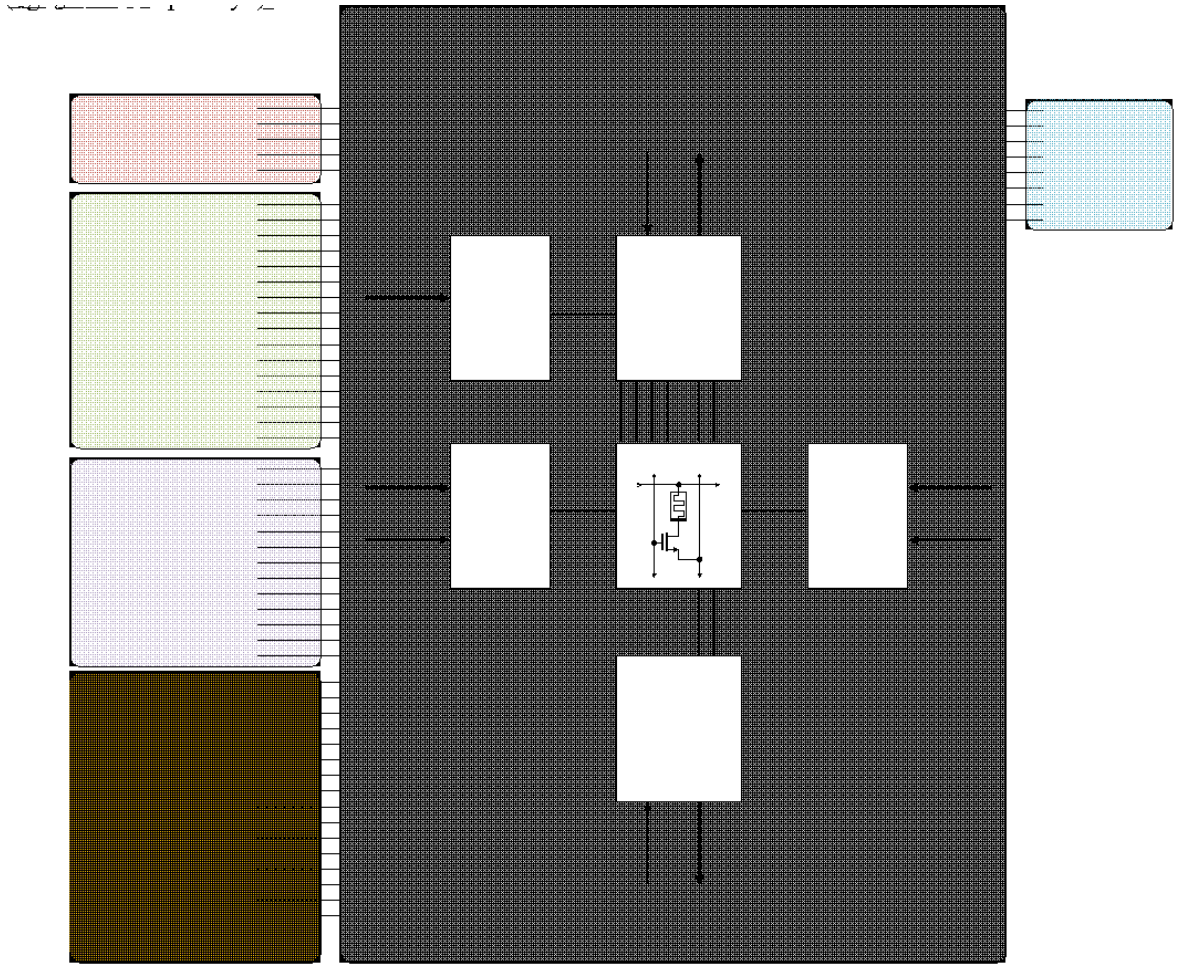


# Table of Figures

# Table of Tables

# Appendix

## Mixed-signal Tile I/O Specification



### Tile I/O List

| DL_LEFT | | | | | | |
|---|---|---|---|---|---|---|
| **Net Name** | **Description** | **Type** | **Min** | **Typ** | **Max** | **Units** |
| D_DL_SYS_CLK_L | System clock DL_LEFT | Digital Input | | 1.2 | | V |
| D_DL_nRESET_L | System reset DL_LEFT | Digital Input | | 1.2 | | V |
| R_DL_VFORM_SELECT_L | One-hot VFORM write voltage select DL_LEFT | Register | | 1.2 | | V |
| R_DL_VSET_SELECT_L | One-hot VSET write voltage select DL_LEFT | Register | | 1.2 | | V |
| R_DL_VRESET_SELECT_L | One-hot VRESET write voltage select DL_LEFT | Register | | 1.2 | | V |

| | | | | | | |
|---|---|---|---|---|---|---|
| R_DL_READ_EN_L | One-hot global read voltage enable, connects read DAC to crossbar | Register | | 1.2 | | V |
| D_DL_WR_EN<254:0:2> | Drive line write enable switch control from decoder | Digital | | 1.2 | | V |
| D_DL_GND_EN<254:0:2> | Drive line ground enable switch control from decoder | Digital Input | | 1.2 | | V |
| D_DL_DSTREAM<254:0:2> | 1b read DAC data input from serializer | Digital Input | | 1.2 | | V |
| D_DL_DSTREAM_EN<254:0:2> | 1b read DAC tri-state for single read from decoder | Digital Input | | 1.2 | | V |
| V_FORM | FORM voltage | Off-chip reference | | 3 | | V |
| V_SET | SET voltage | Off-chip reference | | 3 | 5 | V |
| V_RESET | RESET voltage | Off-chip reference | | 3 | | V |
| V_READ | READ voltage top setting | Off-chip reference | | 1.2 | | V |
| VDDH | Level-shifter VDD | Off-chip reference | | 3.3 | | V |
| VDDL | Analog VDD | Off-chip reference | | 1.2 | | V |
| VCM | READ voltage bottom setting | Off-chip reference | | 0.9 | | V |
| VSS | System ground | Off-chip reference | | 0 | | V |
| DL<254:0:2> | Drive line output to crossbar | Analog | | | | V |

| **DL_RIGHT** | | | | | | |
|---|---|---|---|---|---|---|
| **Net Name** | **Description** | **Type** | **Min** | **Typ** | **Max** | **Units** |
| D_DL_SYS_CLK_R | System clock DL_RIGHT | Digital Input | | 1.2 | | V |
| D_DL_nRESET_R | System reset DL_RIGHT | Digital Input | | 1.2 | | V |
| R_DL_VFORM_SELECT_R | One-hot VFORM write voltage select DL_RIGHT | Register | | 1.2 | | V |
| R_DL_VSET_SELECT_R | One-hot VSET write voltage select DL_RIGHT | Register | | 1.2 | | V |
| R_DL_VRESET_SELECT_R | One-hot VRESET write voltage select DL_RIGHT | Register | | 1.2 | | V |
| R_DL_READ_EN_R | One-hot global read voltage enable, connects read DAC to crossbar | Register | | 1.2 | | V |
| D_DL_WR_EN<255:1:2> | Drive line write enable switch control from decoder | Digital Input | | 1.2 | | V |
| D_DL_GND_EN<255:1:2> | Drive line ground enable switch control from decoder | Digital Input | | 1.2 | | V |
| D_DL_DSTREAM<255:1:2> | 1b read DAC data input from serializer | Digital Input | | 1.2 | | V |
| D_DL_DSTREAM_EN<255:1:2> | 1b read DAC tri-state for single read from decoder | Digital Input | | 1.2 | | V |
| V_FORM | FORM voltage | Off-chip reference | | 3 | | V |
| V_SET | SET voltage | Off-chip reference | | 3 | 5 | V |
| V_RESET | RESET voltage | Off-chip reference | | 3 | | V |

| | | | | | | |
|---|---|---|---|---|---|---|
| V_READ | READ voltage top setting | Off-chip reference | | 3 | | V |
| VDDH | Level-shifter VDD | Off-chip reference | | 3.3 | | V |
| VDDL | Analog VDD | Off-chip reference | | 1.2 | | V |
| VCM | READ voltage bottom setting, virtual ground setting | Off-chip reference | | 0.9 | | V |
| VSS | System ground | Off-chip reference | | 0 | | V |
| DL<255:1:2> | Drive line output to crossbar | Analog | | | | V |

| **BL_TOP** | | | | | | |
|---|---|---|---|---|---|---|
| **Net Name** | **Description** | **Type** | **Min** | **Typ** | **Max** | **Units** |
| D_WL_CH_EN<60:0:4> | Word line channel enable switch control from decoder | Digital Input | | 1.2 | | V |
| D_WL_CH_EN<61:1:4> | Word line channel enable switch control from decoder | Digital Input | | 1.2 | | V |
| D_WL_CH_EN<62:2:4> | Word line channel enable switch control from decoder | Digital Input | | 1.2 | | V |
| D_WL_CH_EN<63:3:4> | Word line channel enable switch control from decoder | Digital Input | | 1.2 | | V |
| D_BL_WR_EN<62:2:4> | Bit line write enable switch control from decoder | Digital Input | | 1.2 | | V |
| D_BL_WR_EN<63:3:4> | Bit line write enable switch control from decoder | Digital Input | | 1.2 | | V |
| D_BL_GND_EN<62:2:4> | Bit line ground enable switch control from decoder | Digital Input | | 1.2 | | V |
| D_BL_GND_EN<63:3:4> | Bit line ground enable switch control from decoder | Digital Input | | 1.2 | | V |
| D_BL_READ_EN<62:2:4> | Bit line read enable switch control from decoder | Digital Input | | 1.2 | | V |
| D_BL_READ_EN<63:3:4> | Bit line read enable switch control from decoder | Digital Input | | 1.2 | | V |
| R_BL_MAC_EN_T | MAC enable | Register | | 1.2 | | V |
| R_BL_TIA_EN_T | TIA enable | Register | | 1.2 | | V |
| D_BL_ADC_EN_T | ADC enable from timing generator, for clock gating | Digital Input | | 1.2 | | V |
| D_BL_ADC_CLK_T | Free running sys_clk/2 | Digital Input | | 1.2 | | V |
| D_BL_ADC_CONV_T | ADC conversion signal from timing generator, for clock gating | Digital Input | | 1.2 | | V |
| D_BL_ADC_CONF_T<1:0> | ADC configuration bits | Digital Input | | 1.2 | | V |
| D_BL_ADC7<31:1:2> | ADC output to AXI bus | Digital Output | | 1.2 | | V |
| D_BL_ADC6<31:1:2> | ADC output to AXI bus | Digital Output | | 1.2 | | V |
| D_BL_ADC5<31:1:2> | ADC output to AXI bus | Digital Output | | 1.2 | | V |
| D_BL_ADC4<31:1:2> | ADC output to AXI bus | Digital Output | | 1.2 | | V |
| D_BL_ADC3<31:1:2> | ADC output to AXI bus | Digital Output | | 1.2 | | V |
| D_BL_ADC2<31:1:2> | ADC output to AXI bus | Digital Output | | 1.2 | | V |
| D_BL_ADC1<31:1:2> | ADC output to AXI bus | Digital Output | | 1.2 | | V |
| D_BL_ADC0<31:1:2> | ADC output to AXI bus | Digital Output | | 1.2 | | V |

| | | | | | | |
|---|---|---|---|---|---|---|
| WL_IN | Word line voltage input from global WL mux to channel mux | Analog | | | | V |
| I_BL_TIA_10U | TIA current reference | Off-chip reference | | 10u | | A |
| V_BL_ADC_TOP | ADC top voltage reference | Off-chip reference | | 0.7 | | V |
| V_BL_ADC_BOT | ADC bottom voltage reference | Off-chip reference | | 0 | | V |
| V_RESET | RESET voltage | Off-chip reference | | 3 | | V |
| VDDWL | Word line VDD | Off-chip reference | | 3.3 | | V |
| VDDH | Level-shifter VDD | Off-chip reference | | 3.3 | | V |
| VDDL | Analog VDD | Off-chip reference | | 1.2 | | V |
| VCM | READ voltage bottom setting, virtual ground setting | Off-chip reference | | 0.9 | | V |
| VSS | Analog GND | Off-chip reference | | 0 | | V |
| WL<60:0:4> | Word line output to crossbar | Digital Output | | | | V |
| WL<61:1:4> | Word line output to crossbar | Digital Output | | | | V |
| WL<62:2:4> | Word line output to crossbar | Digital Output | | | | V |
| WL<63:3:4> | Word line output to crossbar | Digital Output | | | | V |
| BL<62:2:4> | Bit line input from crossbar | Digital Output | | 0.9 | | V |
| BL<63:3:4> | Bit line input from crossbar | Digital Output | | 0.9 | | V |

| **WL_GLOBAL** | | | | | | |
|---|---|---|---|---|---|---|
| **Net Name** | **Description** | **Type** | **Min** | **Typ** | **Max** | **Units** |
| R_WL_VDD_SELECT | One-hot WL MUX VDD select | Register | | 1.2 | | V |
| R_WL_DAC_SELECT | One-hot WL MUX DAC select | Register | | 1.2 | | V |
| R_WL_DAC_DIN<8:0> | Word line Gate DAC digital input word | Register | | 1.2 | | V |
| R_WL_DAC_AMP_EN | Word line Gate DAC output buffer amplifier enable | Register | | 1.2 | | V |
| I_WL_DAC_10U | Word line Gate DAC output buffer current reference | Off-chip reference | | 10u | | A |
| V_WL_DAC_TOP | Word line Gate DAC top voltage reference | Off-chip reference | | 2.9 | | V |
| V_WL_DAC_BOT | Word line Gate DAC bottom voltage reference | Off-chip reference | | 0.5 | | V |
| VDDWL | Word line VDD | Off-chip reference | | 3.3 | | V |
| VDDH | Level-shifter VDD | Off-chip reference | | 3.3 | | V |
| VDDL | Analog VDD | Off-chip reference | | 1.2 | | V |
| VSS | Analog GND | Off-chip reference | | 0 | | V |
| **BL_BOT** | | | | | | |
| **Net Name** | **Description** | **Type** | **Min** | **Typ** | **Max** | **Units** |
| D_BL_WR_EN<60:0:4> | Bit line write enable switch control from decoder | Digital | | 1.2 | | V |

| | | | | | | |
|---|---|---|---|---|---|---|
| D_BL_WR_EN<61:1:4> | Bit line write enable switch control from decoder | Digital | | 1.2 | | V |
| D_BL_GND_EN<60:0:4> | Bit line ground enable switch control from decoder | Digital | | 1.2 | | V |
| D_BL_GND_EN<61:1:4> | Bit line ground enable switch control from decoder | Digital | | 1.2 | | V |
| D_BL_READ_EN<60:0:4> | Bit line read enable switch control from decoder | Digital | | 1.2 | | V |
| D_BL_READ_EN<61:1:4> | Bit line read enable switch control from decoder | Digital | | 1.2 | | V |
| R_BL_MAC_EN_B | MAC enable | Register | | 1.2 | | V |
| R_BL_TIA_EN_B | TIA enable | Register | | 1.2 | | V |
| D_BL_ADC_EN_B | ADC enable from timing generator, for clock gating | Digital | | 1.2 | | V |
| D_BL_ADC_CLK_B | Free running sys_clk/2 | Digital | | 1.2 | | V |
| D_BL_ADC_CONV_B | ADC conversion signal from timing generator, for clock gating | Digital | | 1.2 | | V |
| D_BL_ADC_CONF_B<1:0> | ADC configuration bits | Digital | | 1.2 | | V |
| D_BL_ADC7<30:0:2> | ADC output to AXI bus | Digital | | 1.2 | | V |
| D_BL_ADC6<30:0:2> | ADC output to AXI bus | Digital | | 1.2 | | V |
| D_BL_ADC5<30:0:2> | ADC output to AXI bus | Digital | | 1.2 | | V |
| D_BL_ADC4<30:0:2> | ADC output to AXI bus | Digital | | 1.2 | | V |
| D_BL_ADC3<30:0:2> | ADC output to AXI bus | Digital | | 1.2 | | V |
| D_BL_ADC2<30:0:2> | ADC output to AXI bus | Digital | | 1.2 | | V |
| D_BL_ADC1<30:0:2> | ADC output to AXI bus | Digital | | 1.2 | | V |
| D_BL_ADC0<30:0:2> | ADC output to AXI bus | Digital | | 1.2 | | V |
| I_BL_TIA_BOT_10U | TIA current reference | Off-chip reference | | 10u | | A |
| V_BL_ADC_TOP | ADC top voltage reference | Off-chip reference | | 0.7 | | V |
| V_BL_ADC_BOT | ADC bottom voltage reference | Off-chip reference | | 0+ | | V |
| V_RESET | RESET voltage | Off-chip reference | | 3 | | V |
| VDDH | Level-shifter VDD | Off-chip reference | | 3.3 | | V |
| VDDL | Analog VDD | Off-chip reference | | 1.2 | | V |
| VCM | READ voltage bottom setting, virtual ground setting | Off-chip reference | | 0.9 | | V |
| VSS | Analog GND | Off-chip reference | | 0 | | V |
| BL<60:0:4> | Bit line input from crossbar | Digital | | 0.9 | | V |
| BL<61:1:4> | Bit line input from crossbar | Digital | | 0.9 | | V |

## DRIVE LINE I/O List

| **DL_GLOBAL** | | | | | | |
|---|---|---|---|---|---|---|
| **Net Name** | **Description** | **Type** | **Min** | **Typ** | **Max** | **Units** |

| | | | | | | |
|---|---|---|---|---|---|---|
| D_SYS_CLK | System clock | Digital Input | | 1.2 | | V |
| D_nRESET | System reset | Digital Input | | 1.2 | | V |
| R_DL_VFORM_SELECT | One-hot V_FORM select, global write voltage select | Register | | 1.2 | | V |
| R_DL_VSET_SELECT | One-hot V_SET select, global write voltage select | Register | | 1.2 | | V |
| R_DL_VRESET_SELECT | One-hot V_RESET select, global write voltage select | Register | | 1.2 | | V |
| R_DL_READ_EN | One-hot select global read enable | Register | | 1.2 | | V |
| V_FORM | Form voltage from off-chip | Off-chip reference | | 3 | | V |
| V_SET | Set voltage from off-chip | Off-chip reference | | 3 | 5 | V |
| V_RESET | Reset voltage from off-chip | Off-chip reference | | 3 | | V |
| VDDH | Level-shifter VDD | Off-chip reference | | 3.3 | | V |
| VDDL | Analog VDD | Off-chip reference | | 1.2 | | V |
| VSS | Analog GND | GND | | 0 | | V |
| SYS_CLKB_BUF | Buffered system clock | Digital Output | | 1.2 | | V |
| nRESET_BUF | Buffered reset | Digital Output | | 1.2 | | V |
| DL_READ_EN | One-hot select global read enable, level-shifted | Digital Output | | 3.3 | | V |
| V_WRITE | Write voltage output to DL slices | Reference | | | | V |

| **DL_SLICE** | | | | | | |
|---|---|---|---|---|---|---|
| **Net Name** | **Description** | **Type** | **Min** | **Typ** | **Max** | **Units** |
| SYS_CLKB_BUF | System clock (inverted for mixed-signal 1/4 clk delay) | Digital Input | | 1.2 | | V |
| nRESET_BUF | System reset | Digital Input | | 1.2 | | V |
| DL_READ_EN | Global pulse DAC enable, tri-states 1.2V DACs during write, global level shifter | Digital Input | | 1.2 | | V |
| D_DL_WR_EN | Row slice write enable, connected selected row to write voltage | Digital Input | | 1.2 | | V |
| D_DL_GND_EN | Row slice ground enable, grounds selected row | Digital Input | | 1.2 | | V |
| D_DL_DSTREAM | Row slice input data stream, data input to 1b DAC | Digital Input | | 1.2 | | V |
| D_DL_DSTREAM_EN | Row slice data stream enable, tri-states unselected DACs during single read | Digital Input | | 1.2 | | V |
| V_WRITE | Write voltage from global write voltage select | Reference | | | | V |
| V_READ | 1b DAC reference high | Off-chip reference | | 1.2 | | V |
| VDDH | Level-shifter VDD | Off-chip reference | | 3.3 | | V |
| VDDL | Analog VDD | Off-chip reference | | 1.2 | | V |
| VCM | 1b DAC reference low | Off-chip reference | | 0.9 | | V |
| VSS | Analog GND | GND | | 0 | | V |
| DL | Drive line crossbar connection | Analog | | | | V |

## BIT LINE Top I/O List

| BL_GLOBAL | | | | | | |
|---|---|---|---|---|---|---|
| **Net Name** | **Description** | **Type** | **Min** | **Typ** | **Max** | **Units** |
| R_BL_TIA_EN | TIA enable | Digital Input | | 1.2 | | V |
| I_BL_TIA_10U | TIA current reference | Analog | | 10u | | A |
| D_BL_ADC_EN | ADC enable from timing generator, for clock gating | Digital Input | | 1.2 | | V |
| D_BL_ADC_CLK | Free running sys_clk/2 | Digital Input | | 1.2 | | V |
| D_BL_ADC_CONV | ADC conversion signal from timing generator, for clock gating | Digital Input | | 1.2 | | V |
| R_BL_ADC_CONF<1:0> | ADC configuration bits | Digital Input | | 1.2 | | V |
| VDDL | Analog VDD | Off-chip reference | | 1.2 | | V |
| VSS | Analog GND | Off-chip reference | | 0 | | V |
| TIA_EN | TIA enable | Digital Output | | 1.2 | | V |
| TIA_ENB | TIA enable bar | Digital Output | | 1.2 | | V |
| TIA_VBP | TIA + voltage reference from current reference | Analog | | | | V |
| TIA_VBN | TIA - voltage reference from current reference | Analog | | | | V |
| ADC_SAMP | ADC sample clock, 8 clocks @ MS clock rate (sys_clk/2) | Digital Output | | 1.2 | | V |
| ADC_CONV | ADC conversion signal, 1 clock @ MS clock rate(sys_clk/2) | Digital Output | | 1.2 | | V |
| ADC_CONF<1:0> | ADC configuration bits | Digital Output | | 1.2 | | V |

| BL_WL_SLICE | | | | | | |
|---|---|---|---|---|---|---|
| **Net Name** | **Description** | **Type** | **Min** | **Typ** | **Max** | **Units** |
| BL_EVEN | Bit line input from crossbar, even columns | Analog | | | | V |
| BL_ODD | Bit line input from crossbar, odd columns | Analog | | | | V |
| D_BL_WR_EN_EVEN | Bit line write enable switch control from decoder | Digital Input | | 1.2 | | V |
| D_BL_WR_EN_ODD | Bit line write enable switch control from decoder | Digital Input | | 1.2 | | V |
| D_BL_GND_EN_EVEN | Bit line ground enable switch control from decoder | Digital Input | | 1.2 | | V |
| D_BL_GND_EN_ODD | Bit line ground enable switch control from decoder | Digital Input | | 1.2 | | V |
| D_BL_READ_EN_EVEN | Bit line read enable switch control from decoder | Digital Input | | 1.2 | | V |
| D_BL_READ_EN_EVEN | Bit line read enable switch control from decoder | Digital Input | | 1.2 | | V |
| R_BL_MAC_EN | MAC enable | Digital Input | | 1.2 | | V |
| TIA_EN | TIA enable | Digital Input | | 1.2 | | V |

| | | | | | | |
|---|---|---|---|---|---|---|
| TIA_ENB | TIA enable bar | Digital Input | | 1.2 | | V |
| TIA_VBP | TIA + voltage reference from current reference | Analog | | | | V |
| TIA_VBN | TIA - voltage reference from current reference | Analog | | | | V |
| ADC_SAMP | ADC sample clock, 8 clocks @ MS clock rate (sys_clk/2) | Digital Input | | 1.2 | | V |
| ADC_CONV | ADC conversion signal, 1 clock @ MS clock rate(sys_clk/2) | Digital Input | | 1.2 | | V |
| ADC_CONF<1:0> | ADC configuration bits | Digital Input | | 1.2 | | V |
| V_BL_ADC_TOP | ADC top voltage reference | Off-chip reference | | 0.7 | | V |
| V_BL_ADC_BOT | ADC bottom votlage reference | Off-chip reference | | 0+ | | V |
| V_RESET | | Analog | | 3 | | V |
| VDDH | Level-shifter VDD | Off-chip reference | | 3.3 | | V |
| VDDL | Analog VDD | Off-chip reference | | 1.2 | | V |
| VCM | READ voltage bottom setting, virtual ground setting | Off-chip reference | | 0.9 | | V |
| VSS | Analog GND | Off-chip reference | | 0 | | V |
| WL_IN | Word line voltage input from global WL mux to channel mux | Analog | | | | V |
| WL_EVEN1 | Word line output to crossbar | Analog | | | | V |
| WL_ODD1 | Word line output to crossbar | Analog | | | | V |
| WL_EVEN2 | Word line output to crossbar | Analog | | | | V |
| WL_ODD2 | Word line output to crossbar | Analog | | | | V |
| D_WL_CH_EN_EVEN1 | Word line channel enable switch control from decoder | Digital Input | | 1.2 | | V |
| D_WL_CH_EN_ODD1 | Word line channel enable switch control from decoder | Digital Input | | 1.2 | | V |
| D_WL_CH_EN_EVEN2 | Word line channel enable switch control from decoder | Digital Input | | 1.2 | | V |
| D_WL_CH_EN_ODD2 | Word line channel enable switch control from decoder | Digital Input | | 1.2 | | V |
| VDDWL | Word line VDD | Off-chip reference | | 3.3 | | V |
| VDDL | Analog VDD | Off-chip reference | | 1.2 | | V |
| VSS | Analog GND | Off-chip reference | | 0 | | V |
| D7 | ADC output bit 7 | Digital Output | | 1.2 | | V |
| D6 | ADC output bit 6 | Digital Output | | 1.2 | | V |
| D5 | ADC output bit 5 | Digital Output | | 1.2 | | V |
| D4 | ADC output bit 4 | Digital Output | | 1.2 | | V |
| D3 | ADC outptu bit 3 | Digital Output | | 1.2 | | V |
| D2 | ADC output bit 2 | Digital Output | | 1.2 | | V |
| D1 | ADC output bit 1 | Digital Output | | 1.2 | | V |
| D0 | ADC output bit 0 | Digital Output | | 1.2 | | V |

## BIT LINE Bottom I/O List

| BL_GLOBAL | | | | | | |
|---|---|---|---|---|---|---|
| **Net Name** | **Description** | **Type** | **Min** | **Typ** | **Max** | **Units** |
| R_BL_TIA_EN | TIA enable | Digital Input | | 1.2 | | V |
| I_BL_TIA_10U | TIA current reference | Analog | | 10u | | A |
| D_BL_ADC_EN | ADC enable from timing generator, for clock gating | Digital Input | | 1.2 | | V |
| D_BL_ADC_CLK | Free running sys_clk/2 | Digital Input | | 1.2 | | V |
| D_BL_ADC_CONV | ADC conversion signal from timing generator, for clock gating | Digital Input | | 1.2 | | V |
| R_BL_ADC_CONF<1:0> | ADC configuration bits | Digital Input | | 1.2 | | V |
| VDDL | Analog VDD | Off-chip reference | | 1.2 | | V |
| VSS | Analog GND | Off-chip reference | | 0 | | V |
| TIA_EN | TIA enable | Digital Output | | 1.2 | | V |
| TIA_ENB | TIA enable bar | Digital Output | | 1.2 | | V |
| TIA_VBP | TIA + voltage reference from current reference | Analog | | | | V |
| TIA_VBN | TIA - voltage reference from current reference | Analog | | | | V |
| ADC_SAMP | ADC sample clock, 8 clocks @ MS clock rate (sys_clk/2) | Digital Output | | 1.2 | | V |
| ADC_CONV | ADC conversion signal, 1 clock @ MS clock rate(sys_clk/2) | Digital Output | | 1.2 | | V |
| ADC_CONF<1:0> | ADC configuration bits | Digital Output | | 1.2 | | V |

| BL_WL_SLICE | | | | | | |
|---|---|---|---|---|---|---|
| **Net Name** | **Description** | **Type** | **Min** | **Typ** | **Max** | **Units** |
| BL_EVEN | Bit line input from crossbar, even columns | Analog | | | | V |
| BL_ODD | Bit line input from crossbar, odd columns | Analog | | | | V |
| D_BL_WR_EN_EVEN | Bit line write enable switch control from decoder | Digital Input | | 1.2 | | V |
| D_BL_WR_EN_ODD | Bit line write enable switch control from decoder | Digital Input | | 1.2 | | V |
| D_BL_GND_EN_EVEN | Bit line ground enable switch control from decoder | Digital Input | | 1.2 | | V |
| D_BL_GND_EN_ODD | Bit line ground enable switch control from decoder | Digital Input | | 1.2 | | V |
| D_BL_READ_EN_EVEN | Bit line read enable switch control from decoder | Digital Input | | 1.2 | | V |
| D_BL_READ_EN_EVEN | Bit line read enable switch control from decoder | Digital Input | | 1.2 | | V |
| R_BL_MAC_EN | MAC enable | Digital Input | | 1.2 | | V |
| TIA_EN | TIA enable | Digital Input | | 1.2 | | V |
| TIA_ENB | TIA enable bar | Digital Input | | 1.2 | | V |
| TIA_VBP | TIA + voltage reference from current reference | Analog | | | | V |
| TIA_VBN | TIA - voltage reference from current reference | Analog | | | | V |

| | | | | | | |
|---|---|---|---|---|---|---|
| ADC_SAMP | ADC sample clock, 8 clocks @ MS clock rate (sys_clk/2) | Digital Input | | 1.2 | | V |
| ADC_CONV | ADC conversion signal, 1 clock @ MS clock rate(sys_clk/2) | Digital Input | | 1.2 | | V |
| ADC_CONF<1:0> | ADC configuration bits | Digital Input | | 1.2 | | V |
| V_BL_ADC_TOP | ADC top voltage reference | Off-chip reference | | 0.7 | | V |
| V_BL_ADC_BOT | ADC bottom votlage reference | Off-chip reference | | 0+ | | V |
| V_RESET | | Analog | | | | V |
| VDDH | Level-shifter VDD | Off-chip reference | | 3.3 | | V |
| VDDL | Analog VDD | Off-chip reference | | 1.2 | | V |
| VCM | READ voltage bottom setting, virtual ground setting | Off-chip reference | | 0.9 | | V |
| VSS | Analog GND | Off-chip reference | | 0 | | V |
| D7 | ADC output bit 7 | Digital Output | | 1.2 | | V |
| D6 | ADC output bit 6 | Digital Output | | 1.2 | | V |
| D5 | ADC output bit 5 | Digital Output | | 1.2 | | V |
| D4 | ADC output bit 4 | Digital Output | | 1.2 | | V |
| D3 | ADC outptu bit 3 | Digital Output | | 1.2 | | V |
| D2 | ADC output bit 2 | Digital Output | | 1.2 | | V |
| D1 | ADC output bit 1 | Digital Output | | 1.2 | | V |
| D0 | ADC output bit 0 | Digital Output | | 1.2 | | V |

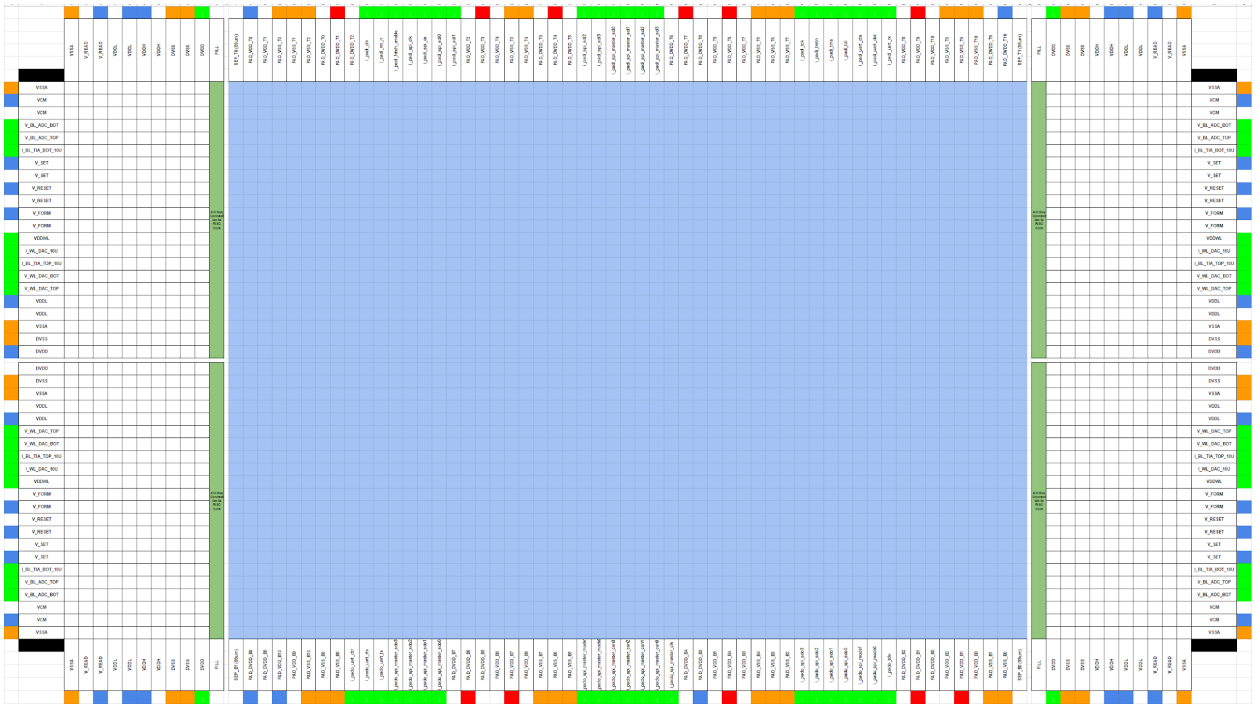
## WORD LINE DAC and Mux I/O List

| **WL_DAC** | | | | | | |
|---|---|---|---|---|---|---|
| **Net Name** | **Description** | **Type** | **Min** | **Typ** | **Max** | **Units** |
| R_WL_DAC_DIN<8:0> | Word line gate DAC input word | Digital Input | | 1.2 | | V |
| R_WL_DAC_AMP_EN | Word line gate DAC output buffer amplifer enable | Digital Input | | 1.2 | | V |
| I_WL_DAC_10U | Word line gate DAC output buffer current reference | Analog | | 10u | | A |
| V_WL_DAC_TOP | Word line gate DAC top voltage reference | Off-chip reference | | 2.9 | | V |
| V_WL_DAC_BOT | Word line gate DAC bottom voltage reference | Off-chip reference | | 0.5 | | V |
| VDDH | Level-shifter VDD | Off-chip reference | | 3.3 | | V |
| VDDL | Analog VDD | Off-chip reference | | 1.2 | | V |
| VSS | Analog VSS | Off-chip reference | | 0 | | V |
| WL_DAC | Word line DAC voltage output | Analog | | | | V |

| **WL_MUX** | | | | | | |
|---|---|---|---|---|---|---|
| **Net Name** | **Description** | **Type** | **Min** | **Typ** | **Max** | **Units** |

| | | | | | | |
|---|---|---|---|---|---|---|
| R_WL_VDD_SELECT | One-hot word line VDD select to channel switches | Digital Input | | 1.2 | | V |
| R_WL_DAC_SELECT | One-hot word line gate DAC select to channel switches | Digital Input | | 1.2 | | V |
| WL_DAC | Word line gate DAC input to global mux | Analog | | | | V |
| VDDWL | Word line VDD | Off-chip reference | | 3.3 | | V |
| VDDL | Analog VDD | Off-chip reference | | 1.2 | | V |
| VSS | Analog GND | Off-chip reference | | 0 | | V |
| WL_IN | Word line mux output to channel switches | Analog | | | | V |

# ASIC Pin Map



# ASIC I/O

| Pad Number | Domain | Sub-Domain | Net Name | I/O | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|---|
| 1 | Analog Tile | Analog Reference | VSSA | GND | | 0 | | V |
| 2 | Analog Tile | 1T1R Read Reference | V_READ | REF | | 1.2 | | V |
| 3 | Analog Tile | 1T1R Read Reference | V_READ | REF | | 1.2 | | V |
| 4 | Analog Tile | Analog LV Reference | VDDL | REF | | 1.2 | | V |
| 5 | Analog Tile | Analog LV Reference | VDDL | REF | | 1.2 | | V |
| 6 | Analog Tile | Analog HV Reference | VDDH | REF | | 3.3 | | V |
| 7 | Analog Tile | Analog HV Reference | VDDH | REF | | 3.3 | | V |
| 8 | N/A | | FILL | | | | | |
| 9 | Digital | Digital Reference | DVSS | GND | | 0 | | V |
| 10 | Digital | Digital Reference | DVSS | GND | | 0 | | V |
| 11 | Digital | Digital Reference | DVDD | REF | | 1.2 | | V |
| 12 | N/A | | SEP_B1 (88um) | | | | | |
| 13 | Digital | | PAD_DVDD_B9 | REF | | 3.3 | | V |
| 14 | Digital | | PAD_DVDD_B8 | REF | | 3.3 | | V |
| 15 | Digital | | PAD_VDD_B10 | REF | | 1.2 | | V |
| 16 | Digital | | PAD_VDD_B9 | REF | | 1.2 | | V |
| 17 | Digital | Digital Reference | PAD_VSS_B10 | GND | | 0 | | V |
| 18 | Digital | Digital Reference | PAD_VSS_B9 | GND | | 0 | | V |
| 19 | Digital | Digital Reference | PAD_VSS_B8 | GND | | 0 | | V |
| 20 | Digital | UART | i_pado_uart_dtr | Output | | 1.2 | | V |
| 21 | Digital | UART | i_pado_uart_rts | Output | | 1.2 | | V |
| 22 | Digital | UART | i_pado_uart_tx | Output | | 1.2 | | V |
| 23 | Digital | SPI Master | i_pado_spi_master_sdo3 | Output | | 1.2 | | V |
| 24 | Digital | SPI Master | i_pado_spi_master_sdo2 | Output | | 1.2 | | V |
| 25 | Digital | SPI Master | i_pado_spi_master_sdo1 | Output | | 1.2 | | V |
| 26 | Digital | SPI Master | i_pado_spi_master_sdo0 | Output | | 1.2 | | V |
| 27 | Digital | | PAD_DVDD_B7 | REF | | 3.3 | | V |
| 28 | Digital | | PAD_DVDD_B6 | REF | | 3.3 | | V |
| 29 | Digital | | PAD_DVDD_B5 | REF | | 3.3 | | V |
| 30 | Digital | | PAD_VDD_B8 | REF | | 1.2 | | V |
| 31 | Digital | | PAD_VDD_B7 | REF | | 1.2 | | V |
| 32 | Digital | | PAD_VDD_B6 | REF | | 1.2 | | V |
| 33 | Digital | Digital Reference | PAD_VSS_B7 | GND | | 0 | | V |
| 34 | Digital | Digital Reference | PAD_VSS_B6 | GND | | 0 | | V |
| 35 | Digital | Digital Reference | PAD_VSS_B5 | GND | | 0 | | V |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| 36 | Digital | SPI Master | i_pado_spi_master_mode1 | Output | | 1.2 | | V |
| 37 | Digital | SPI Master | i_pado_spi_master_mode0 | Output | | 1.2 | | V |
| 38 | Digital | SPI Master | i_pado_spi_master_csn3 | Output | | 1.2 | | V |
| 39 | Digital | SPI Master | i_pado_spi_master_csn2 | Output | | 1.2 | | V |
| 40 | Digital | SPI Master | i_pado_spi_master_csn1 | Output | | 1.2 | | V |
| 41 | Digital | SPI Master | i_pado_spi_master_csn0 | Output | | 1.2 | | V |
| 42 | Digital | SPI Master | i_pado_spi_master_clk | Output | | 1.2 | | V |
| 43 | Digital | | PAD_DVDD_B4 | REF | | 3.3 | | V |
| 44 | Digital | | PAD_DVDD_B3 | REF | | 3.3 | | V |
| 45 | Digital | | PAD_VDD_B5 | REF | | 1.2 | | V |
| 46 | Digital | | PAD_VDD_B4 | REF | | 1.2 | | V |
| 47 | Digital | | PAD_VDD_B3 | REF | | 1.2 | | V |
| 48 | Digital | Digital Reference | PAD_VSS_B4 | GND | | 0 | | V |
| 49 | Digital | Digital Reference | PAD_VSS_B3 | GND | | 0 | | V |
| 50 | Digital | Digital Reference | PAD_VSS_B2 | GND | | 0 | | V |
| 51 | Digital | Quad SPI | i_pado_spi_sdo3 | Output | | 1.2 | | V |
| 52 | Digital | Quad SPI | i_pado_spi_sdo2 | Output | | 1.2 | | V |
| 53 | Digital | Quad SPI | i_pado_spi_sdo1 | Output | | 1.2 | | V |
| 54 | Digital | Quad SPI | i_pado_spi_sdo0 | Output | | 1.2 | | V |
| 55 | Digital | Quad SPI | i_pado_spi_mode1 | Output | | 1.2 | | V |
| 56 | Digital | Quad SPI | i_pado_spi_mode0 | Output | | 1.2 | | V |
| 57 | Digital | JTAG | i_pado_tdo | Output | | 1.2 | | V |
| 58 | Digital | | PAD_DVDD_B2 | REF | | 3.3 | | V |
| 59 | Digital | | PAD_DVDD_B1 | REF | | 3.3 | | V |
| 60 | Digital | | PAD_DVDD_B0 | REF | | 3.3 | | V |
| 61 | Digital | | PAD_VDD_B2 | REF | | 1.2 | | V |
| 62 | Digital | | PAD_VDD_B1 | REF | | 1.2 | | V |
| 63 | Digital | | PAD_VDD_B0 | REF | | 1.2 | | V |
| 64 | Digital | Digital Reference | PAD_VSS_B1 | GND | | 0 | | V |
| 65 | Digital | Digital Reference | PAD_VSS_B0 | GND | | 0 | | V |
| 66 | N/A | | SEP_B0 (88um) | | | | | |
| 67 | Digital | Digital Reference | DVDD | REF | | 1.2 | | V |
| 68 | Digital | Digital Reference | DVSS | GND | | 0 | | V |
| 69 | Digital | Digital Reference | DVSS | GND | | 0 | | V |
| 70 | N/A | | FILL | | | | | |
| 71 | Analog Tile | Analog HV Reference | VDDH | REF | | 3.3 | | V |
| 72 | Analog Tile | Analog HV Reference | VDDH | REF | | 3.3 | | V |
| 73 | Analog Tile | Analog LV Reference | VDDL | REF | | 1.2 | | V |
| 74 | Analog Tile | Analog LV Reference | VDDL | REF | | 1.2 | | V |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| 75 | Analog Tile | 1T1R Read Reference | V_READ | REF | | 1.2 | | V |
| 76 | Analog Tile | 1T1R Read Reference | V_READ | REF | | 1.2 | | V |
| 77 | Analog Tile | Analog Reference | VSSA | GND | | 0 | | V |
| 78 | Analog Tile | Analog Reference | VSSA | GND | | 0 | | V |
| 79 | Analog Tile | 1T1R Read Reference | VCM | REF | | 0.9 | | V |
| 80 | Analog Tile | 1T1R Read Reference | VCM | REF | | 0.9 | | V |
| 81 | Analog Tile | ADC Reference | V_BL_ADC_BOT | REF | | 0 | | V |
| 82 | Analog Tile | ADC Reference | V_BL_ADC_TOP | REF | | 0.7 | | V |
| 83 | Analog Tile | TIA Reference | I_BL_TIA_BOT_10U | REF | | 10u | | A |
| 84 | Analog Tile | 1T1R Write Reference | V_SET | REF | | 3 | 5 | V |
| 85 | Analog Tile | 1T1R Write Reference | V_SET | REF | | 3 | 5 | V |
| 86 | Analog Tile | 1T1R Write Reference | V_RESET | REF | | 3 | | V |
| 87 | Analog Tile | 1T1R Write Reference | V_RESET | REF | | 3 | | V |
| 88 | Analog Tile | 1T1R Write Reference | V_FORM | REF | | 3 | | V |
| 89 | Analog Tile | 1T1R Write Reference | V_FORM | REF | | 3 | | V |
| 90 | Analog Tile | 1T1R Gate Reference | VDDWL | REF | | 3.3 | | V |
| 91 | Analog Tile | Gate DAC Reference | I_WL_DAC_10U | REF | | 10u | | A |
| 92 | Analog Tile | TIA Reference | I_BL_TIA_TOP_10U | REF | | 10u | | A |
| 93 | Analog Tile | Gate DAC Reference | V_WL_DAC_BOT | REF | | 0.5 | | V |
| 94 | Analog Tile | Gate DAC Reference | V_WL_DAC_TOP | REF | | 2.9 | | V |
| 95 | Analog Tile | Analog LV Reference | VDDL | REF | | 1.2 | | V |
| 96 | Analog Tile | Analog LV Reference | VDDL | REF | | 1.2 | | V |
| 97 | N/A | | FILL | | | | | |
| 98 | Digital | Digital Reference | VSSA | GND | | 0 | | V |
| 99 | Digital | Digital Reference | VSSA | GND | | 0 | | V |
| 100 | Digital | Digital Reference | DVDD | REF | | 1.2 | | V |
| 101 | Digital | Digital Reference | DVDD | REF | | 1.2 | | V |
| 102 | Digital | Digital Reference | VSSA | GND | | 0 | | V |
| 103 | Digital | Digital Reference | VSSA | GND | | 0 | | V |
| 104 | N/A | | FILL | | | | | |
| 105 | Analog Tile | Analog LV Reference | VDDL | REF | | 1.2 | | V |
| 106 | Analog Tile | Analog LV Reference | VDDL | REF | | 1.2 | | V |
| 107 | Analog Tile | Gate DAC Reference | V_WL_DAC_TOP | REF | | 2.9 | | V |
| 108 | Analog Tile | Gate DAC Reference | V_WL_DAC_BOT | REF | | 0.5 | | V |
| 109 | Analog Tile | TIA Reference | I_BL_TIA_TOP_10U | REF | | 10u | | A |
| 110 | Analog Tile | Gate DAC Reference | I_WL_DAC_10U | REF | | 10u | | A |
| 111 | Analog Tile | 1T1R Gate Reference | VDDWL | REF | | 3.3 | | V |
| 112 | Analog Tile | 1T1R Write Reference | V_FORM | REF | | 3 | | V |
| 113 | Analog Tile | 1T1R Write Reference | V_FORM | REF | | 3 | | V |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| 114 | Analog Tile | 1T1R Write Reference | V_RESET | REF | | 3 | | V |
| 115 | Analog Tile | 1T1R Write Reference | V_RESET | REF | | 3 | | V |
| 116 | Analog Tile | 1T1R Write Reference | V_SET | REF | | 3 | 5 | V |
| 117 | Analog Tile | 1T1R Write Reference | V_SET | REF | | 3 | 5 | V |
| 118 | Analog Tile | TIA Reference | I_BL_TIA_BOT_10U | REF | | 10u | | A |
| 119 | Analog Tile | ADC Reference | V_BL_ADC_TOP | REF | | 0.7 | | V |
| 120 | Analog Tile | ADC Reference | V_BL_ADC_BOT | REF | | 0 | | V |
| 121 | Analog Tile | 1T1R Read Reference | VCM | REF | | 0.9 | | V |
| 122 | Analog Tile | 1T1R Read Reference | VCM | REF | | 0.9 | | V |
| 123 | Analog Tile | Analog Reference | VSSA | GND | | 0 | | V |
| 124 | Analog Tile | Analog Reference | VSSA | GND | | 0 | | V |
| 125 | Analog Tile | 1T1R Read Reference | V_READ | REF | | 1.2 | | V |
| 126 | Analog Tile | 1T1R Read Reference | V_READ | REF | | 1.2 | | V |
| 127 | Analog Tile | Analog LV Reference | VDDL | REF | | 1.2 | | V |
| 128 | Analog Tile | Analog LV Reference | VDDL | REF | | 1.2 | | V |
| 129 | Analog Tile | Analog HV Reference | VDDH | REF | | 3.3 | | V |
| 130 | Analog Tile | Analog HV Reference | VDDH | REF | | 3.3 | | V |
| 131 | N/A | | FILL | | | | | |
| 132 | Digital | Digital Reference | DVSS | GND | | 0 | | V |
| 133 | Digital | Digital Reference | DVSS | GND | | 0 | | V |
| 134 | Digital | Digital Reference | DVDD | REF | | 1.2 | | V |
| 135 | N/A | | SEP_T1 (88um) | | | | | |
| 136 | Digital | | PAD_DVDD_T10 | REF | | 3.3 | | V |
| 137 | Digital | | PAD_DVDD_T9 | REF | | 3.3 | | V |
| 138 | Digital | Digital Reference | PAD_VSS_T10 | GND | | 0 | | V |
| 139 | Digital | Digital Reference | PAD_VSS_T9 | GND | | 0 | | V |
| 140 | Digital | Digital Reference | PAD_VSS_T8 | GND | | 0 | | V |
| 141 | Digital | | PAD_VDD_T10 | REF | | 1.2 | | V |
| 142 | Digital | | PAD_VDD_T9 | REF | | 1.2 | | V |
| 143 | Digital | | PAD_VDD_T8 | REF | | 1.2 | | V |
| 144 | Digital | UART | i_padi_uart_rx | Input | | 1.2 | | V |
| 145 | Digital | UART | i_padi_uart_dsr | Input | | 1.2 | | V |
| 146 | Digital | UART | i_padi_uart_cts | Input | | 1.2 | | V |
| 147 | Digital | JTAG | i_padi_tdi | Input | | 1.2 | | V |
| 148 | Digital | JTAG | i_padi_tms | Input | | 1.2 | | V |
| 149 | Digital | JTAG | i_padi_trstn | Input | | 1.2 | | V |
| 150 | Digital | JTAG | i_padi_tck | Input | | 1.2 | | V |
| 151 | Digital | Digital Reference | PAD_VSS_T7 | GND | | 0 | | V |
| 152 | Digital | Digital Reference | PAD_VSS_T6 | GND | | 0 | | V |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| 153 | Digital | Digital Reference | PAD_VSS_T5 | GND | | 0 | | V |
| 154 | Digital | | PAD_VDD_T7 | REF | | 1.2 | | V |
| 155 | Digital | | PAD_VDD_T6 | REF | | 1.2 | | V |
| 156 | Digital | | PAD_VDD_T5 | REF | | 1.2 | | V |
| 157 | Digital | | PAD_DVDD_T8 | REF | | 3.3 | | V |
| 158 | Digital | | PAD_DVDD_T7 | REF | | 3.3 | | V |
| 159 | Digital | | PAD_DVDD_T6 | REF | | 3.3 | | V |
| 160 | Digital | SPI Master | i_padi_spi_master_sdi3 | Input | | 1.2 | | V |
| 161 | Digital | SPI Master | i_padi_spi_master_sdi2 | Input | | 1.2 | | V |
| 162 | Digital | SPI Master | i_padi_spi_master_sdi1 | Input | | 1.2 | | V |
| 163 | Digital | SPI Master | i_padi_spi_master_sdi0 | Input | | 1.2 | | V |
| 164 | Digital | Quad SPI | i_padi_spi_sdi3 | Input | | 1.2 | | V |
| 165 | Digital | Quad SPI | i_padi_spi_sdi2 | Input | | 1.2 | | V |
| 166 | Digital | | PAD_DVDD_T5 | REF | | 3.3 | | V |
| 167 | Digital | | PAD_DVDD_T4 | REF | | 3.3 | | V |
| 168 | Digital | | PAD_DVDD_T3 | REF | | 3.3 | | V |
| 169 | Digital | Digital Reference | PAD_VSS_T4 | GND | | 0 | | V |
| 170 | Digital | Digital Reference | PAD_VSS_T3 | GND | | 0 | | V |
| 171 | Digital | | PAD_VDD_T4 | REF | | 1.2 | | V |
| 172 | Digital | | PAD_VDD_T3 | REF | | 1.2 | | V |
| 173 | Digital | | PAD_VDD_T2 | REF | | 1.2 | | V |
| 174 | Digital | Quad SPI | i_padi_spi_sdi1 | Input | | 1.2 | | V |
| 175 | Digital | Quad SPI | i_padi_spi_sdi0 | Input | | 1.2 | | V |
| 176 | Digital | Quad SPI | i_padi_spi_cs | Input | | 1.2 | | V |
| 177 | Digital | Quad SPI | i_padi_spi_clk | Input | | 1.2 | | V |
| 178 | Digital | Core | i_padi_fetch_enable | Input | | 1.2 | | V |
| 179 | Digital | Core | i_padi_rst_n | Input | | 1.2 | | V |
| 180 | Digital | Core | i_padi_clk | Input | | 1.2 | | V |
| 181 | Digital | | PAD_DVDD_T2 | REF | | 3.3 | | V |
| 182 | Digital | | PAD_DVDD_T1 | REF | | 3.3 | | V |
| 183 | Digital | | PAD_DVDD_T0 | REF | | 3.3 | | V |
| 184 | Digital | Digital Reference | PAD_VSS_T2 | GND | | 0 | | V |
| 185 | Digital | Digital Reference | PAD_VSS_T1 | GND | | 0 | | V |
| 186 | Digital | Digital Reference | PAD_VSS_T0 | GND | | 0 | | V |
| 187 | Digital | | PAD_VDD_T1 | REF | | 1.2 | | V |
| 188 | Digital | | PAD_VDD_T0 | REF | | 1.2 | | V |
| 189 | N/A | | SEP_T0 (88um) | | | | | |
| 190 | Digital | Digital Reference | DVDD | REF | | 1.2 | | V |
| 191 | Digital | Digital Reference | DVSS | GND | | 0 | | V |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| 192 | Digital | Digital Reference | DVSS | GND | | 0 | | V |
| 193 | N/A | | FILL | | | | | |
| 194 | Analog Tile | Analog HV Reference | VDDH | REF | | 3.3 | | V |
| 195 | Analog Tile | Analog HV Reference | VDDH | REF | | 3.3 | | V |
| 196 | Analog Tile | Analog LV Reference | VDDL | REF | | 1.2 | | V |
| 197 | Analog Tile | Analog LV Reference | VDDL | REF | | 1.2 | | V |
| 198 | Analog Tile | 1T1R Read Reference | V_READ | REF | | 1.2 | | V |
| 199 | Analog Tile | 1T1R Read Reference | V_READ | REF | | 1.2 | | V |
| 200 | Analog Tile | Analog Reference | VSSA | GND | | 0 | | V |
| 201 | Analog Tile | Analog Reference | VSSA | GND | | 0 | | V |
| 202 | Analog Tile | 1T1R Read Reference | VCM | REF | | 0.9 | | V |
| 203 | Analog Tile | 1T1R Read Reference | VCM | REF | | 0.9 | | V |
| 204 | Analog Tile | ADC Reference | V_BL_ADC_BOT | REF | | 0 | | V |
| 205 | Analog Tile | ADC Reference | V_BL_ADC_TOP | REF | | 0.7 | | V |
| 206 | Analog Tile | TIA Reference | I_BL_TIA_BOT_10U | REF | | 10u | | A |
| 207 | Analog Tile | 1T1R Write Reference | V_SET | REF | | 3 | 5 | V |
| 208 | Analog Tile | 1T1R Write Reference | V_SET | REF | | 3 | 5 | V |
| 209 | Analog Tile | 1T1R Write Reference | V_RESET | REF | | 3 | | V |
| 210 | Analog Tile | 1T1R Write Reference | V_RESET | REF | | 3 | | V |
| 211 | Analog Tile | 1T1R Write Reference | V_FORM | REF | | 3 | | V |
| 212 | Analog Tile | 1T1R Write Reference | V_FORM | REF | | 3 | | V |
| 213 | Analog Tile | 1T1R Gate Reference | VDDWL | REF | | 3.3 | | V |
| 214 | Analog Tile | Gate DAC Reference | I_WL_DAC_10U | REF | | 10u | | A |
| 215 | Analog Tile | TIA Reference | I_BL_TIA_TOP_10U | REF | | 10u | | A |
| 216 | Analog Tile | Gate DAC Reference | V_WL_DAC_BOT | REF | | 0.5 | | V |
| 217 | Analog Tile | Gate DAC Reference | V_WL_DAC_TOP | REF | | 2.9 | | V |
| 218 | Analog Tile | Analog LV Reference | VDDL | GND | | 1.2 | | V |
| 219 | Analog Tile | Analog LV Reference | VDDL | GND | | 1.2 | | V |
| 220 | N/A | | FILL | | | | | |
| 221 | Digital | Digital Reference | VSSA | GND | | 0 | | V |
| 222 | Digital | Digital Reference | VSSA | GND | | 0 | | V |
| 223 | Digital | Digital Reference | DVDD | REF | | 1.2 | | V |
| 224 | Digital | Digital Reference | DVDD | REF | | 1.2 | | V |
| 225 | Digital | Digital Reference | VSSA | GND | | 0 | | V |
| 226 | Digital | Digital Reference | VSSA | GND | | 0 | | V |
| 227 | N/A | | FILL | | | | | |
| 228 | Analog Tile | Analog LV Reference | VDDL | REF | | 1.2 | | V |
| 229 | Analog Tile | Analog LV Reference | VDDL | REF | | 1.2 | | V |
| 230 | Analog Tile | Gate DAC Reference | V_WL_DAC_TOP | REF | | 2.9 | | V |

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|---|---|---|---|---|---|---|---|---|
| 231 | Analog Tile | Gate DAC Reference | V_WL_DAC_BOT | REF | | 0.5 | | V |
| 232 | Analog Tile | TIA Reference | I_BL_TIA_TOP_10U | REF | | 10u | | A |
| 233 | Analog Tile | Gate DAC Reference | I_WL_DAC_10U | REF | | 10u | | A |
| 234 | Analog Tile | 1T1R Gate Reference | VDDWL | REF | | 3.3 | | V |
| 235 | Analog Tile | 1T1R Write Reference | V_FORM | REF | | 3 | | V |
| 236 | Analog Tile | 1T1R Write Reference | V_FORM | REF | | 3 | | V |
| 237 | Analog Tile | 1T1R Write Reference | V_RESET | REF | | 3 | | V |
| 238 | Analog Tile | 1T1R Write Reference | V_RESET | REF | | 3 | | V |
| 239 | Analog Tile | 1T1R Write Reference | V_SET | REF | | 3 | 5 | V |
| 240 | Analog Tile | 1T1R Write Reference | V_SET | REF | | 3 | 5 | V |
| 241 | Analog Tile | TIA Reference | I_BL_TIA_BOT_10U | REF | | 10u | | A |
| 242 | Analog Tile | ADC Reference | V_BL_ADC_TOP | REF | | 0.7 | | V |
| 243 | Analog Tile | ADC Reference | V_BL_ADC_BOT | REF | | 0 | | V |
| 244 | Analog Tile | 1T1R Read Reference | VCM | REF | | 0.9 | | V |
| 245 | Analog Tile | 1T1R Read Reference | VCM | REF | | 0.9 | | V |
| 246 | Analog Tile | Analog Reference | VSSA | GND | | 0 | | V |