Space optimised FPGA-based side-microprocessor.

PRCO304 - Project Initiation Document

Ben Lancaster
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Abstract
The Discrete Fourier Transform algorithm is widely used in digital signal processing applications, particularly for converting time domain signals to the frequency domain. The algorithm has $O(n^2)$ complexity resulting in long computation times for large data sets. Introducing parallel concepts to this sequential algorithm, like dividing the input samples over multiple processes, and utilizing GPU hardware with CUDA, can greatly increase the performance. Results show that a performance increase of 5x to 10x can be seen on small to large datasets using both MPI and CUDA solutions.

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1 Introduction

Modern electronics equipment, like function generators, oscilloscopes, and spectrum analysers, use FPGAs to implement their compute intensive logic. These FPGAs are often accompanied by a small, low-cost, microprocessor to supervise and provide interfaces to external peripherals.

The aim of this project is to implement this side-microprocessor into the FPGA to save on BOM costs, PCB space, and power costs, which contribute to higher development and product costs. While savings can be made by the lack of side microprocessor, the product may need a larger FPGA to accommodate the embedded microprocessor. The project will produce a small, soft-core, CPU design and compiler.

2 Business Case

The requirement of a side-microprocessor to control and provide external interfaces to FPGA-based applications carries a significant demand in both development and projects costs.

Firstly, the additional PCB space and design considerations to house the external microprocessor results in additional design planning and manufacturing costs.

Firstly, the inclusion of a external microprocessor in a project design will require

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