Highlight Reports

PRCO304 - FPGA-based RISC microprocessor

Ben Lancaster
February 14, 2018

Revision History

Table 1: Document revisions.

Date	Highlight	Changes
14/02/2018	2	Highlight report 2.
06/02/2018	1	Highlight report 1.

Table of Contents

1 Highlight Reports

1.1 Highlight Report 1

PRCO304: Highlight Report 1
Name: Ben Lancaster
Date: 06/02/2018
Active project stage: Stage 1.1: Research and Requirement Gathering
Review of work undertaken: This week was assigned to work on stage 1.1: Research and requirement gathering. **Research and requirement gathering:** Research into existing soft-core processor designs has been started to identify their features, targets, and advantages and disadvantages. Key existing soft-core processors found are: - Xilinx' MicroBlaze: a 32-bit Xilinx FPGA embeddable core capable of running operating systems, like Linux. Exposes a configurable GUI to customise the build of the processor to suit designers requirements (like number of GPIO, interrupts, timers, etc.). - ARM Cortex-A9: a 32-bit Xilinx and Altera FPGA core. Features out-of-order execution, compatible with existing ARM Thumb2 C compilers, and multi-core processing. I have used this research to aim my soft-core processor's requirements and architecture. To document and finalize my processors design and requirements, I have started a processor specification and reference document. This document outlines the processors features, architecture, compatibility, and instructions. Additional progress: - Version control set up for documentation, highlight reports, and code bases.
Risks and Challenges: Urgent risks: New risks: Existing risks: RC4: Schedule overrun. A gantt time chart has been created to better visualize task durations and requirements.
Plan of work for the next week: Work will begin on Stage 1.2: Core high level design. Finalised specifications and architecture of the soft-core processor will be put into a processor specification and reference document. Architecture, control, pipelines, will be visualised in this document.
Date(s) of supervisory meeting(s) since last Highlight: This is the 1st highlight report. 30/01/18 - An introductory meeting was held to discuss the project initiation document (PID) and gain feedback on the project.
Notes from supervisory meeting(s) held since last Highlight: Ensure risks are carefully explored and project core deliverables are realistic and achievable.

1.2 Highlight Report 2

PRCO304: Highlight Report 2

Name: Ben Lancaster

Date: 15/02/2018

Active project stage: Stage 1.2: Core high level design

Review of work undertaken:
This week was assigned to work on stage 1.2: Core high level design. gathering.

Core high level design:
I have spent this week defining a processor specification and creating a processor specification/reference guide booklet (see attached). This booklet will contain both high-level and technical details regarding the design and implementation of the processor, including: register sets, control and pipelining strategies, the ISA and each instruction, and the compiler and how to use it.

This booklet will be developed over the life cycle of the project. Although the specification has been clearly defined, the booklet will be incrementally updated as processor features/requirements are added to the implementation (such as instructions, modules, and compiler features).

Currently the reference booklet contains: register set definitions, several primitive instructions, and a brief introduction to instruction cycle timing.

Risks and Challenges:
Urgent risks:
New risks:
Existing risks:
~~RC4: Schedule overrun. A gantt time chart has been created to better visualize task durations and requirements.~~
Resolved risks:
RC4: Schedule overrun. A gantt time chart has been created to better visualize task durations and requirements. (See attached time management chart indev.)

Plan of work for the next week:
Work will begin on Stage 2.0: Core dev. Register set implementation.

The register set module will be implemented in Verilog for the processor. Unit tests will be created to verify the timing/behaviour of the module.
The processor specification/reference booklet will be updated to describe how the register set has been implemented in the processor.

Date(s) of supervisory meeting(s) since last Highlight:
08/02/18 15:00 - 15:40

Notes from supervisory meeting(s) held since last Highlight:
Discussion included comparing existing processor's (ARM, x86) features (privileged instructions, interrupts, IO, variable-length ISA) and designs (ISA and pipelining) to this processor.