BEN-1816 - Processor Documentation

PRCO304 - Processor Documentation

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Revision History

Table 1: Document revisions.

Date	Version	Changes
04/02/2018	1.00	Initial revision. Processor introduction. Initial ISA. Initial Register definitions.

Table of Contents

1   BEN-1816 Processor

The BEN-1816 processor is a soft-microprocessor design targeted for general purpose computing and co-processing.

1.1   Features

- Small, embeddable, Verilog core.

- 16-bit RISC instruction set.

- 16-bit register, ALU, and IO, bus widths.

- 12+12 general purpose IO inputs and outputs.

- 9 special IO pins.

    - 4 PWM pins.
    - 2 RS232 pins.
    - 3 SPI pins.

2   BEN-1816 Architecture

2.1   Registers

BEN-1816 has a total of 6 addressable, read and write, registers. These registers are identified by letters A through F.

2.1.1   General Purpose Registers

Registers A through D are designed for general purpose use and are safe to store user values over the run-time of the processor.

Table 2: General purpose registers.

Registers	Bits	Description
A through D	15:0	4 General purpose registers

Instructions that require a destination register, such as CMP, can reference any register (even special registers if that is your requirement). For the CMP instruction as an example, the processor will put the result of the comparison instruction in the destination register, overwriting any value present in that register.

2.1.2   Special Registers

Registers E and F are special registers within the processor. The processor cannot guarantee that a value written or read in these registers will persist over the run-time of the processor. Erroneously writing to these registers may severely affect program and processor behaviour.

Even though all registers can be used at the will of the programmer, it is recommended to isolate a few registers to provide special features, such as RAM stack management, interrupts, and IO multiplexing.

Table 3: Special registers.

Registers	Bits	Description
E	15:0	RAM Stack pointer
F	15:0	RAM Base pointer

2.2   Interrupts and Exceptions

3 BEN-1816 Instruction Set Architecture

This section describes instructions available on the BEN-1816 processor.

3.1 General Instructions

The term, general instruction, is given to instructions that are common to primitive operations such as arithmetic and comparison instructions.

ADD

Description The ADD instruction adds an immediate value to a destination register, Rd.

Assembly ADD Rd, 255

Pseudocode Rd $<=$ Rd + Imm8

Registers altered Rd

15:12	11:9	8:0
0001	Rd	Imm8

SUB

Description The SUB instruction subtracts an immediate value from a destination register, Rd.

Assembly SUB Rd, 255

Pseudocode Rd $<=$ Rd - Imm8

Registers altered Rd

15:12	11:9	8:0
0002	Rd	Imm8

CMP

Description Sets register, Rd, to the value of Ra - Rb.

Assembly CMP Rd, Ra, Rb

Pseudocode Rd $<=$ CMP(Ra, Rb)

Registers altered Rd

15:12	11:9	8:6	5:3	2:0
0003	Rd	Ra	Rb	X

3.2 Special Instructions

4   Compiler

4.1