Highlight Report Document (Rev. 6.00)

PRCO304 - FPGA-based RISC microprocessor

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Revision History

Table 1: Document revisions.

Date	Highlight	Changes
07/03/2018	6	Highlight report 6.
07/03/2018	5	Highlight report 5. Added Highlight Attachments section.
28/02/2018	4	Highlight report 4.
20/02/2018	3	Highlight report 3. Added Risks & Challenges section. Changed header (right) title.
14/02/2018	2	Highlight report 2.
06/02/2018	1	Highlight report 1.

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1 Highlight Reports

1.1 Highlight Report 1

PRCO304: Highlight Report 1

Name: Ben Lancaster

Date: 06/02/2018

Active project stage: Stage 1.1: Research and Requirement Gathering

Review of work undertaken:
This week was assigned to work on stage 1.1: Research and requirement gathering.

Research and requirement gathering:
Research into existing soft-core processor designs has been started to identify their features, targets, and advantages and disadvantages. Key existing soft-core processors found are:
- Xilinx' MicroBlaze: a 32-bit Xilinx FPGA embeddable core capable of running operating systems, like Linux. Exposes a configurable GUI to customise the build of the processor to suit designers requirements (like number of GPIO, interrupts, timers, etc.).
- ARM Cortex-A9: a 32-bit Xilinx and Altera FPGA core. Features out-of-order execution, compatible with existing ARM Thumb2 C compilers, and multi-core processing.

I have used this research to aim my soft-core processor's requirements and architecture. To document and finalize my processors design and requirements, I have started a processor specification and reference document. This document outlines the processors features, architecture, compatibility, and instructions.

Additional progress:
- Version control set up for documentation, highlight reports, and code bases.

Risks and Challenges:
Urgent risks:
New risks:
Existing risks:
RC4: Schedule overrun. A gantt time chart has been created to better visualize task durations and requirements.

Plan of work for the next week:
Work will begin on Stage 1.2: Core high level design.

Finalised specifications and architecture of the soft-core processor will be put into a processor specification and reference document.
Architecture, control, pipelines, will be visualised in this document.

Date(s) of supervisory meeting(s) since last Highlight:
This is the 1st highlight report.
30/01/18 - An introductory meeting was held to discuss the project initiation document (PID) and gain feedback on the project.

Notes from supervisory meeting(s) held since last Highlight:
Ensure risks are carefully explored and project core deliverables are realistic and achievable.

1.2 Highlight Report 2

PRCO304: Highlight Report 2

Name: Ben Lancaster

Date: 15/02/2018

Active project stage: Stage 1.2: Core high level design

Review of work undertaken:
This week was assigned to work on stage 1.2: Core high level design. gathering.

Core high level design:
I have spent this week defining a processor specification and creating a processor specification/reference guide booklet (see attached). This booklet will contain both high-level and technical details regarding the design and implementation of the processor, including: register sets, control and pipelining strategies, the ISA and each instruction, and the compiler and how to use it.

This booklet will be developed over the life cycle of the project. Although the specification has been clearly defined, the booklet will be incrementally updated as processor features/requirements are added to the implementation (such as instructions, modules, and compiler features).

Currently the reference booklet contains: register set definitions, several primitive instructions, and a brief introduction to instruction cycle timing.

Risks and Challenges:
Urgent risks:
New risks:
Existing risks:
~~RC4: Schedule overrun. A gantt time chart has been created to better visualize task durations and requirements.~~
Resolved risks:
RC4: Schedule overrun. A gantt time chart has been created to better visualize task durations and requirements. (See attached time management chart indev.)

Plan of work for the next week:
Work will begin on Stage 2.0: Core dev. Register set implementation.

The register set module will be implemented in Verilog for the processor. Unit tests will be created to verify the timing/behaviour of the module.
The processor specification/reference booklet will be updated to describe how the register set has been implemented in the processor.

Date(s) of supervisory meeting(s) since last Highlight:
08/02/18 15:00 - 15:40

Notes from supervisory meeting(s) held since last Highlight:
Discussion included comparing existing processor's (ARM, x86) features (privileged instructions, interrupts, IO, variable-length ISA) and designs (ISA and pipelining) to this processor.

1.3 Highlight Report 3

PRCO304: Highlight Report 3
Name: Ben Lancaster
Date: 20/02/2018
Active project stage: Stage 2.0: Core Register-set Implementation.
Review of work undertaken: This week was assigned to work on stage 2.0: Core Register-set Implementation. **Core Register-set Implementation:** Good progress has been made implementing the PRCO processor's register set in Verilog. The register set consists of 8 16-bit wide general purpose registers labelled rA through rH in duel-port read and single-port write. Implementation progress is approximately 1 week ahead of schedule. Because of this, work has also been done on the decoder and ALU modules. Consideration of the control/sequencing pipeline has been considered. The pipeline needs to work for time-varying functions (such as memory writes). The current plan is to give each module outputs to signal when it has finished so the following module can safely read in data and operate on it. A handshake between modules currently seems overkill due to the relatively simple structure but may be considered later in the project.
Risks and Challenges: Urgent risks: New risks: RC5: Complex memory operations (PUSH, POP) may require multiple instructions. PUSH/POP might be split into: (1) Inc/dec stack pointer; (2) Read RAM[stack pointer]. The compiler will be able to resolve this issue. Existing risks: Resolved risks:
Plan of work for the next week: Work will begin on Stage 2.1: Core dev. Decoder implementation. Some progress has already made but the decoder is not finished. The processor specification/reference booklet will continued to be updated with implementation specific details of the processor.
Date(s) of supervisory meeting(s) since last Highlight: 13/02/18 09:40
Notes from supervisory meeting(s) held since last Highlight: This discussions was over email; it was decided that a physical meeting would not be beneficial as the current project stage was starting the *PRCO Processor Reference Guide* booklet. Progress on the booklet was shared and a brief overview of the Register-set and Decoder implementation.

1.4 Highlight Report 4

PRCO304: Highlight Report 4

Name: Ben Lancaster

Date: 28/02/2018

Active project stage:
Stage 2.1: Core: Register-set Implementation.
Stage 2.2: Core: ALU, RAM Implementation.

Review of work undertaken:
Stage 2.1: Core: Decoder Implementation:
Simple instructions, ADD, ADDI, MOV, MOVI, SUB, SUBI, LW, SW, instructions can now be decoded. The decoder has been integrated into the pipeline and it can choose and set up appropriate dependencies for the instruction.

Stage 2.2: Core: ALU, RAM Implementation:
ALU development has started. Some basic operations such as ADD, ADDI, SUB, SUBI, and pass-through ops such as MOV, MOVI, have been implemented. On-chip ram development will be starting this week.

Core: Pipeline/control system
A significant development breakthrough for the control/pipeline system has been achieved. I'm calling it a feed-forward pipeline as the flow of control only moves in the forward direction and when the previous module has completed.

Compiler: Text parser development starting:
Work into a simple text parser has begun including file opening, reading character by character, and a parser stack.

Risks and Challenges:
Urgent risks:
New risks:
Existing risks:
RC5: Complex memory operations (PUSH, POP) may require multiple instructions. PUSH/POP might be split into: (1) Inc/dec stack pointer; (2) Read RAM[stack pointer]. The compiler will be able to resolve this issue.
Resolved risks:

Plan of work for the next week:
Work will continue for 1 more week on stage 2.1 and 2.2 as per the time plan.
The processor specification/reference booklet will continued to be updated with implementation specific details of the processor.

Date(s) of supervisory meeting(s) since last Highlight:
21/02/18 13:00 - 13:4

Notes from supervisory meeting(s) held since last Highlight:
Discussion included improving time management gantt chart by showing task dependencies; and potential final demo ideas (store ASCII string on SDcard/external memory and have processor loop over and print each character out over RS232.

1.5 Highlight Report 5

PRCO304: Highlight Report 5

Name: Ben Lancaster

Date: 07/03/2018

Active project stage:
(ON-TIME) Stage 2.2: Core: ALU, RAM Implementation.
(EARLY) Stage 3.0: Compiler: Code-generation.

Review of work undertaken:
(ON-TIME) Stage 2.2: Core: ALU, RAM Implementation:
CMP and JMP instructions have been implemented. The CMP instruction is the only 3 register instruction (Type 3) and required a bit of reworking to implement. The CMP instruction subtracts Ra from Rb and sets appropriate status bits (SR_Z, SR_O, SR_E, SR_0) into the Rd register. The JMP instruction also required a bit of reworking as it affects the Program Counter. It is passed an 8-bit immediate containing jump conditions (JMP_EQ, JMP_GE, JMP_LT, etc.) and compares against the SR register specific in the CMP instruction.

(EARLY) Stage 3.0: Compiler: Code-generation.
Work has started ahead-of-schedule on code-generation for the compiler. I have begun implementing functions to encode instructions into the ISA's machine-code format. In addition, the compiler will also print out human-readable assembly in AT&T format.

Real-hardware Implementation:
I have also begun testing the implementation on the FPGA development board. Doing this early allows me to fix critical synthesis problems earlier, reducing risk for the project and demonstration. Figure 1 shows the FPGA core running on the FPGA development board.

Risks and Challenges:
Urgent risks:
New risks:
Existing risks:
RC5: Complex memory operations (PUSH, POP) may require multiple instructions. PUSH/POP might be split into: (1) Inc/dec stack pointer; (2) Read RAM[stack pointer]. The compiler will be able to resolve this issue.
Resolved risks:

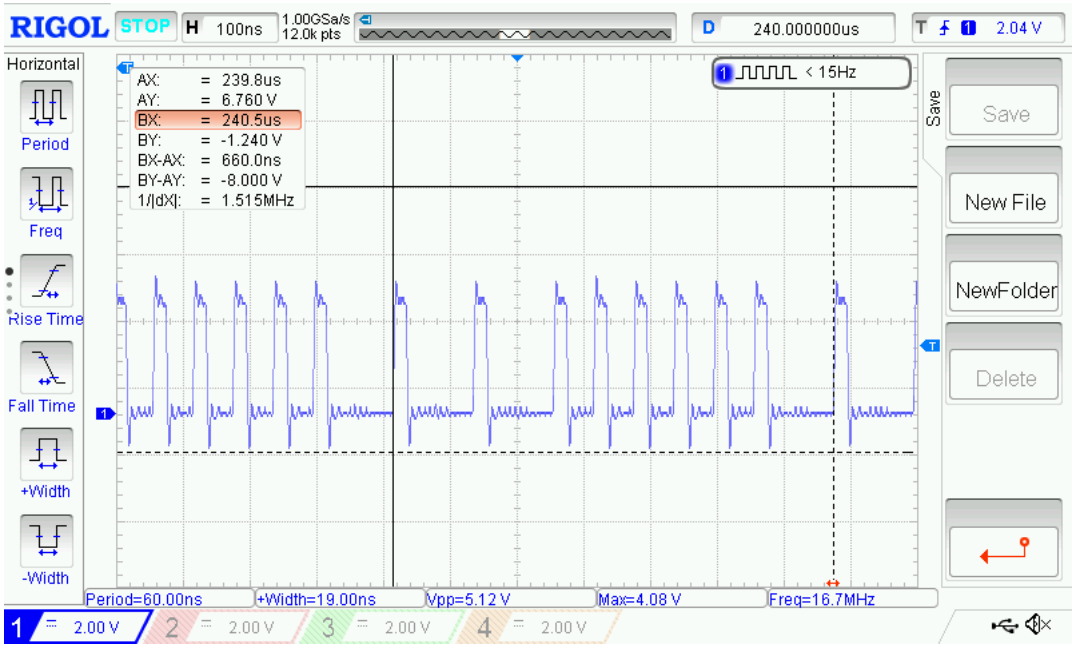
Plan of work for the next week:
Work will begin into the integration of a UART (RS232) communication protocol, allowing us to better demonstrate functionality of the processor and connect to other peripherals.
Work will also begin on implementing an instruction single step cycle button, allowing better demonstration of the core. Currently the demonstration only lasts approximately 800ns.
The processor specification/reference booklet will continued to be updated with implementation specific details of the processor.

Date(s) of supervisory meeting(s) since last Highlight:
01/03/18 (bi-weekly highlight meeting)

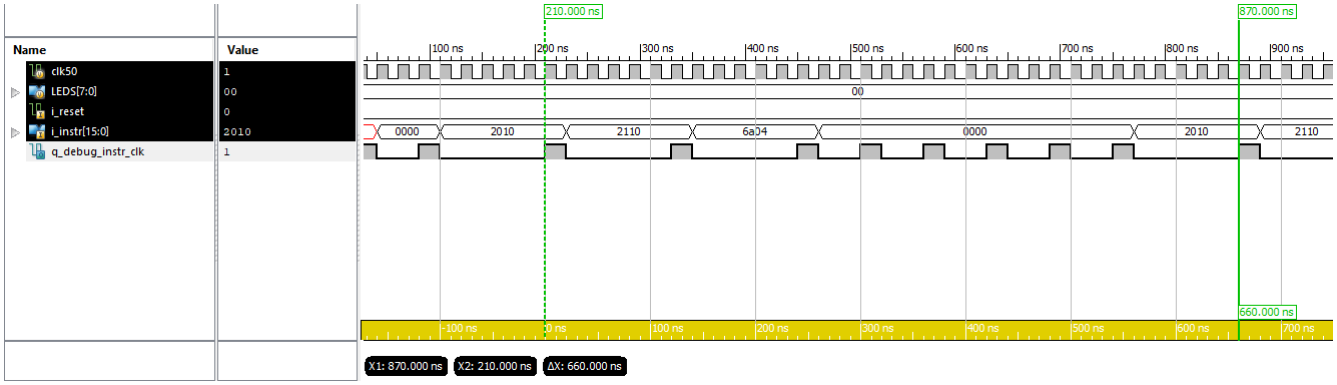
Notes from supervisory meeting(s) held since last Highlight:
Biweekly meetings are held instead of weekly.

2 Highlight Attachments

Highlight 5



(a) Oscilloscope measurement of the *q_debug_instr_clk* signal running on the MiniSpartan6+ development board.



(b) Xilinx iSim simulation view of the *q_debug_instr_clk* signal.

Figure 1: Initial real-hardware implementation on the MiniSpartan6+ (XC6SLX9-3FTG256) development board showing timing of the *q_debug_instr_clk* signal. This signal is a 1 clock pulse indicating the start of an instruction cycle. In this example, instructions: MOVI $10, %Ra; MOVI $10, %Rb; and CMP %Rc, %Ra, %Rb followed by 6 NOP instructions, are used.

We can see that both implementations have a matching 660ns delay between instruction cycles for the same instructions, indicating that the real-hardware FPGA implementation is working correctly.

3 Risks and Challenges

Urgent risks
New risks
Existing risks
Resolved risks

3.1 Project Management

- RC4: Schedule overrun. A gantt time chart has been created to better visualize task durations, requirements, and dependencies.

3.2 CPU Core

- RC5: Complex memory operations (PUSH, POP) may require multiple instructions. PUSH/POP might be split into: (1) Inc/dec stack pointer; (2) Read RAM[stack pointer]. The compiler will be able to resolve this issue.

3.3 Compiler

There are currently no risks/challenges for the compiler.

3.4 Other

There are currently no additional risks/challenges.