

Highlight Reports

PRCO304 - FPGA-based RISC microprocessor

Ben Lancaster

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Revision History

Table 1: Document revisions.

Date	Highlight	Changes
15/02/2018	2	Highlight report 2.
06/02/2018	1	Highlight report 1.

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1 Highlight Reports

1.1 Highlight Report 1

PRCO304: Highlight Report 1
Name: Ben Lancaster
Date: 06/02/2018
Active project stage: Stage 1.1: Research and Requirement Gathering
<p>Review of work undertaken: This week was assigned to work on stage 1.1: Research and requirement gathering.</p> <p>Research and requirement gathering: Research into existing soft-core processor designs has been started to identify their features, targets, and advantages and disadvantages. Key existing soft-core processors found are: - Xilinx' MicroBlaze: a 32-bit Xilinx FPGA embeddable core capable of running operating systems, like Linux. Exposes a configurable GUI to customise the build of the processor to suit designers requirements (like number of GPIO, interrupts, timers, etc.). - ARM Cortex-A9: a 32-bit Xilinx and Altera FPGA core. Features out-of-order execution, compatible with existing ARM Thumb2 C compilers, and multi-core processing.</p> <p>I have used this research to aim my soft-core processor's requirements and architecture. To document and finalize my processors design and requirements, I have started a processor specification and reference document. This document outlines the processors features, architecture, compatibility, and instructions.</p> <p>Additional progress: - Version control set up for documentation, highlight reports, and code bases.</p>
<p>Risks and Challenges: Urgent risks: New risks: Existing risks: RC4: Schedule overrun. A gantt time chart has been created to better visualize task durations and requirements.</p>
<p>Plan of work for the next week: Work will begin on Stage 1.2: Core high level design.</p> <p>Finalised specifications and architecture of the soft-core processor will be put into a processor specification and reference document. Architecture, control, pipelines, will be visualised in this document.</p>
<p>Date(s) of supervisory meeting(s) since last Highlight: This is the 1st highlight report. 30/01/18 - An introductory meeting was held to discuss the project initiation document (PID) and gain feedback on the project.</p>
<p>Notes from supervisory meeting(s) held since last Highlight: Ensure risks are carefully explored and project core deliverables are realistic and achievable.</p>

1.2 Highlight Report 2

PRCO304: Highlight Report 2	
Name:	Ben Lancaster
Date:	15/02/2018
Active project stage:	Stage 1.2: Core high level design
Review of work undertaken:	<p>This week was assigned to work on stage 1.2: Core high level design. gathering.</p> <p>Core high level design:</p> <p>I have spent this week defining a processor specification and creating a processor specification/reference guide booklet (see attached). This booklet will contain both high-level and technical details regarding the design and implementation of the processor, including: register sets, control and pipelining strategies, the ISA and each instruction, and the compiler and how to use it.</p> <p>This booklet will be developed over the life cycle of the project. Although the specification has been clearly defined, the booklet will be incrementally updated as processor features/requirements are added to the implementation (such as instructions, modules, and compiler features).</p> <p>Currently the reference booklet contains: register set definitions, several primitive instructions, and a brief introduction to instruction cycle timing.</p>
Risks and Challenges:	<p>Urgent risks:</p> <p>New risks:</p> <p>Existing risks:</p> <p>RC4: Schedule overrun. A gantt time chart has been created to better visualize task durations and requirements.</p> <p>Resolved risks:</p> <p>RC4: Schedule overrun. A gantt time chart has been created to better visualize task durations and requirements. (See attached time management chart.)</p>
Plan of work for the next week:	<p>Work will begin on Stage 2.0: Core dev. Register set implementation.</p> <p>The register set module will be implemented in Verilog for the processor. Unit tests will be created to verify the timing/behaviour of the module.</p> <p>The processor specification/reference booklet will be updated to describe how the register set has been implemented in the processor.</p>
Date(s) of supervisory meeting(s) since last Highlight:	<p>This is the 1st highlight report.</p> <p>30/01/18 - An introductory meeting was held to discuss the project initiation document (PID) and gain feedback on the project.</p>
Notes from supervisory meeting(s) held since last Highlight:	<p>Ensure risks are carefully explored and project core deliverables are realistic and achievable.</p>