

Weekly Highlight Report Document (Rev. 1.00)

ELEC5881M – Multi-core RISC Processor Design

Ben Lancaster 201280376

MSc (Eng) Embedded Systems Engineering

March 3, 2019

Revision History

Table 1: Document revisions.

Date	Week	Changes
03/03/2019	1	Week 2 report.
25/02/2019	1	Initial week 1 report.

Table of Contents

1	Weekly Reports	2
1.1	Weekly Report 2	3
1.2	Weekly Report 1	4
2	Weekly Report Attachments	5
2.1	Week 1	5
3	Risks and Challenges	6
3.1	Project Management	6
3.2	Other	6

1 Weekly Reports

1.1 Weekly Report 2

Weekly Report 2 – 03/03/19
<p>Active project stage:</p> <p>(ON-TIME) Stage 2.3 – (CORE) Local memory impl & integration</p> <p>(ON-TIME) Stage 3.1 – (CORE) Memory mapped register layout & impl</p>
<p>Review of work undertaken:</p> <p>(ON-TIME) Stage 2.3 – (CORE) Local memory impl & integration The new decoder has been integrated into the pipeline and basic instruction sequences have been verified.</p> <p>(ON-TIME) Stage 3.1 – (CORE) Memory mapped register layout An internal wishbone master interface has been implemented and is controlled by the MMU. A wishbone slave interface has been added to the inputs/outputs of the SoC module. Interaction between cores is still under design, although it will not use Wishbone.</p>
<p>Risks and Challenges:</p> <p>RC2: Multiple tests and deadlines for other modules.</p>
<p>Plan of work for the next week:</p> <p>Stage 2.3 – (CORE) Local memory impl & integration</p> <p>Stage 3.1 – (CORE) Memory mapped register layout</p>
<p>Date(s) of supervisory meeting(s) since last Highlight:</p> <p>26/02/19 – Weekly highlight meeting</p>
<p>Notes from supervisory meeting(s) held since last Highlight:</p> <p>Discussion about target FPGAs: It was decided to target Xilinx Spartan 6 with ISE and Altera Cyclone V with Quartus.</p>

1.2 Weekly Report 1

Weekly Report 1 – 25/02/19
<p>Active project stage:</p> <p>(ON-TIME) Stage 1.2 – (CORE) Stage/Time Allocation Planning</p> <p>(ON-TIME) Stage 2.1 – (CORE) Decoder, Register set, impl & integration</p>
<p>Review of work undertaken:</p> <p>Project tasks and deliverables have been formalised and broken up into smaller tasks.</p> <p>(ON-TIME) Stage 1.2 – (CORE) Stage/Time Allocation Planning</p> <p>The project has been broken up into smaller tasks. Each task has been assigned a start date and expected duration. A gantt chart has also been produced. Images of the gantt chart and task list are included in section 2.1.</p> <p>(ON-TIME) Stage 2.1 – (CORE) Decoder, Register set, impl & integration</p> <p>The new decoder for the new ISA has been built and has been somewhat integrated into the pipeline through the <code>vmicro16_idex</code> module.</p>
<p>Risks and Challenges:</p> <p>Resolved risks:</p> <p>RC1 – Project planning not adequately performed. The project should be broken down into smaller tasks and each task should be assigned a priority and timeslot.</p>
<p>Plan of work for the next week:</p> <p>Stage 2.1 – Continue integrating the new decoder into the CPU module.</p>
<p>Date(s) of supervisory meeting(s) since last Highlight:</p> <p>19/02/19 – Weekly highlight meeting</p>
<p>Notes from supervisory meeting(s) held since last Highlight:</p> <p>RC1 – It was decided to perform a weekly highlight report, which details progress, challenges, and obstacles.</p>

2 Weekly Report Attachments

2.1 Week 1

Stage ID	Task	Start Date	Duration
1	(CORE) Research	04-Feb	7
1.1	(CORE) Requirement gathering/review	11-Feb	14
1.1	(CORE) Processor specification, architecture, ISA	18-Feb	100
1.2	(CORE) Stage/Time Allocation Planning	25-Feb	7
2.1	(CORE) Decoder, Register Set, impl & integration	25-Feb	14
2.2	(CORE) Register set impl & integration	04-Mar	14
2.3	(CORE) Local memory impl & integration	11-Mar	14
X	Intense Coursework/Test month	04-Mar	31
3.1	(CORE) Memory mapped register layout & impl	01-Apr	21
3.2	(CORE) Wishbone peripheral bus connected to MMU	08-Apr	21
3.3	(CORE) Pipelined implementation and verification	15-Apr	21
3.1	(CORE) Cache memory design & impl	22-Apr	28
4.1	(CORE) Multi-core communication interface		
4.2	(CORE) Shared-memory controller		
4.4	(CORE) Scalable multi-core interface (10s of cores)		
4.3	(CORE) Multi-core example program (reduction)		
5.1	(EXT) SPI-FPGA interface for OTG programming		14
5.2	(EXT) FPGA-PC interfacing		28
5.3	(EXT) FPGA-PC debugging (instruction breakpoints)		28
6.1	(EXT) Compiler backend for vmicro16		7
6.2	(EXT) Compiler support for multi-core codegen		21
7.1	(CORE) Wishbone peripherals for demo	01-Aug	7
8	Final Report	11-Mar	150

Figure 1: Deliverables have been formalised and their development has been broken up into stages. Green/yellow colour simply identifies tasks in a new stage.

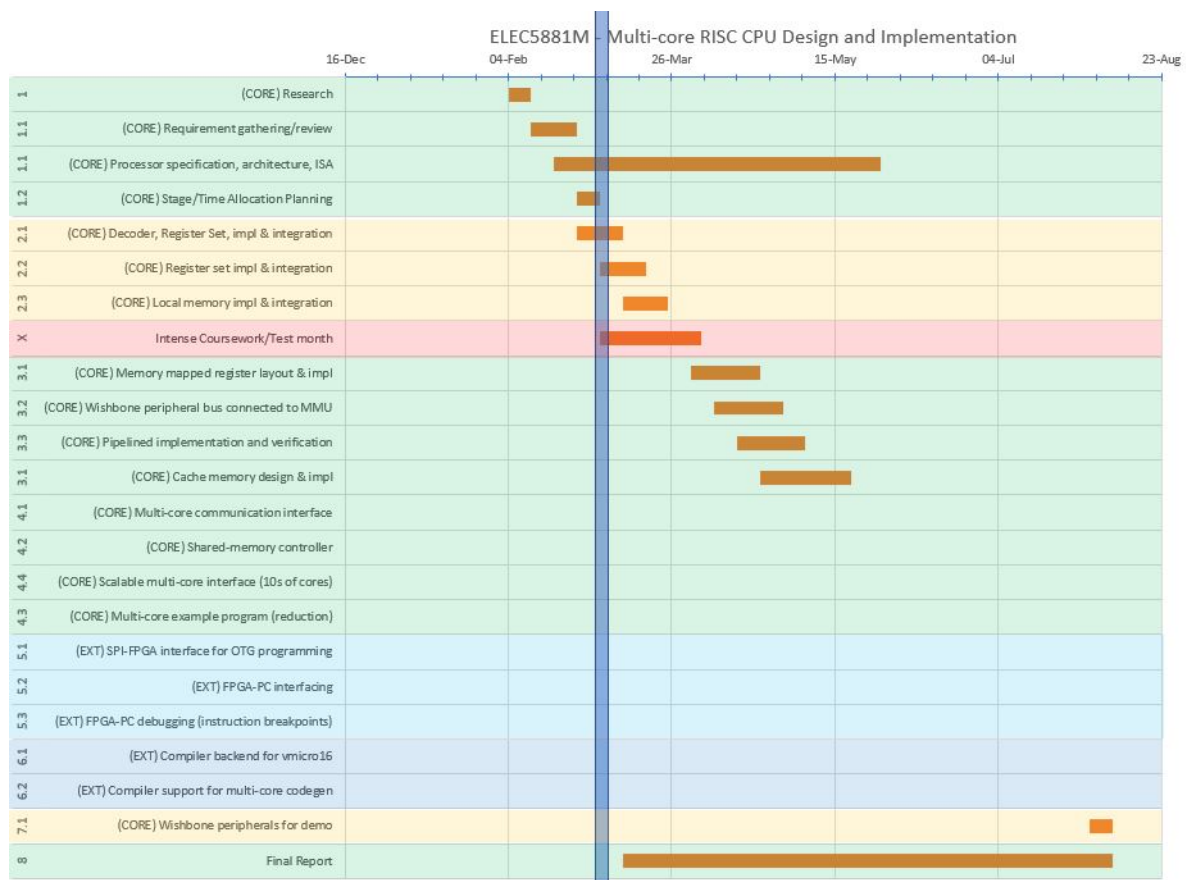


Figure 2: Visualisation of the stages in a Gantt chart.

3 Risks and Challenges

Urgent risks:

- RC2: Multiple tests and deadlines for other modules.

New risks

Existing risks

Resolved risks

3.1 Project Management

- RC1: Project planning not adequately performed. The project should be broken down into smaller tasks and each task should be assigned a priority and timeslot.

3.2 Other

There are currently no additional risks/challenges.