Weekly Highlight Report Document (Rev. 1.00)

ELEC5881M – Multi-core RISC Processor Design

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Revision History

Table 1: Document revisions.

Date	Week	Changes
03/03/2019	1	Week 2 report.
25/02/2019	1	Initial week 1 report.

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1 Weekly Reports

1.1 Weekly Report 5

Weekly Report 5 – 25/03/19
Active project stage: (ON-TIME) Stage 2.3 – (CORE) Local memory impl & integration (ON-TIME) Stage 3.1 – (CORE) Memory mapped register layout (ON-TIME) Stage 8.0 – (CORE) Final Report
Review of work undertaken: Minimal contributions to the project have been made due to high workload and demand from other modules. **(EARLY) Stage 8.0 – (CORE) Final Report** Some work has been started on the interim report.
Risks and Challenges: RC2: Multiple tests and deadlines for other modules.
Plan of work for the next week: Next weeks goals are the same as this weeks due to RC2. Stage 2.3 – (CORE) Local memory impl & integration Stage 3.1 – (CORE) Memory mapped register layout
Date(s) of supervisory meeting(s) since last Highlight: 19/03/19 – Weekly highlight meeting (skipped due to other commitments).
Notes from supervisory meeting(s) held since last Highlight: /

1.2 Weekly Report 4

Weekly Report 4 – 18/03/19
Active project stage: (ON-TIME) Stage 2.3 – (CORE) Local memory impl & integration (ON-TIME) Stage 3.1 – (CORE) Memory mapped register layout & impl
Review of work undertaken: Minimal contributions to the project have been made due to high workload and demand from other modules.
Risks and Challenges: RC2: Multiple tests and deadlines for other modules.
Plan of work for the next week: Next weeks goals are the same as this weeks due to RC2. Stage 2.3 – (CORE) Local memory impl & integration Stage 3.1 – (CORE) Memory mapped register layout
Date(s) of supervisory meeting(s) since last Highlight: 12/03/19 – Weekly highlight meeting (skipped due to other commitments).
Notes from supervisory meeting(s) held since last Highlight: /

1.3 Weekly Report 3

Weekly Report 3 – 11/03/19
Active project stage: (ON-TIME) Stage 2.3 – (CORE) Local memory impl & integration (ON-TIME) Stage 3.1 – (CORE) Memory mapped register layout & impl
Review of work undertaken: Minimal contributions to the project have been made due to high workload and demand from other modules.
Risks and Challenges: RC2: Multiple tests and deadlines for other modules.
Plan of work for the next week: Next weeks goals are the same as this weeks due to RC2. Stage 2.3 – (CORE) Local memory impl & integration. Stage 3.1 – (CORE) Memory mapped register layout.
Date(s) of supervisory meeting(s) since last Highlight: 05/03/19 – Weekly highlight meeting.
Notes from supervisory meeting(s) held since last Highlight: Discussion about time management to allow for time to be spent on other modules.

1.4 Weekly Report 2

Weekly Report 2 – 03/03/19
Active project stage: (ON-TIME) Stage 2.3 – (CORE) Local memory impl & integration (ON-TIME) Stage 3.1 – (CORE) Memory mapped register layout & impl
Review of work undertaken: **(ON-TIME) Stage 2.3 – (CORE) Local memory impl & integration** The new decoder has been integrated into the pipeline and basic instruction sequences have been verified. **(ON-TIME) Stage 3.1 – (CORE) Memory mapped register layout** An internal wishbone master interface has been implemented and is controlled by the MMU. A wishbone slave interface has been added to the inputs/outputs of the SoC module. Interaction between cores is still under design, although it will not use Wishbone.
Risks and Challenges: RC2: Multiple tests and deadlines for other modules.
Plan of work for the next week: Stage 2.3 – (CORE) Local memory impl & integration Stage 3.1 – (CORE) Memory mapped register layout
Date(s) of supervisory meeting(s) since last Highlight: 26/02/19 – Weekly highlight meeting
Notes from supervisory meeting(s) held since last Highlight: Discussion about target FPGAs: It was decided to target Xilinx Spartan 6 with ISE and Altera Cyclone V with Quartus.

1.5 Weekly Report 1

Weekly Report 1 – 25/02/19
Active project stage: (ON-TIME) Stage 1.2 – (CORE) Stage/Time Allocation Planning (ON-TIME) Stage 2.1 – (CORE) Decoder, Register set, impl & integration
Review of work undertaken: Project tasks and deliverables have been formalised and broken up into smaller tasks. **(ON-TIME) Stage 1.2 – (CORE) Stage/Time Allocation Planning** The project has been broken up into smaller tasks. Each task has been assigned a start date and expected duration. A gantt chart has also been produced. Images of the gantt chart and task list are included in section 2.1. **(ON-TIME) Stage 2.1 – (CORE) Decoder, Register set, impl & integration** The new decoder for the new ISA has been built and has been somewhat integrated into the pipeline through the `vmicro16_idex` module.
Risks and Challenges: Resolved risks: RC1 – Project planning not adequately performed. The project should be broken down into smaller tasks and each task should be assigned a priority and timeslot.
Plan of work for the next week: Stage 2.1 – Continue integrating the new decoder into the CPU module.
Date(s) of supervisory meeting(s) since last Highlight: 19/02/19 – Weekly highlight meeting
Notes from supervisory meeting(s) held since last Highlight: RC1 – It was decided to perform a weekly highlight report, which details progress, challenges, and obstacles.

2 Weekly Report Attachments

2.1 Week 1

Stage ID	Task	Start Dat	Duration
1	(CORE) Research	04-Feb	7
1.1	(CORE) Requirement gathering/review	11-Feb	14
1.1	(CORE) Processor specification, architecture, ISA	18-Feb	100
1.2	(CORE) Stage/Time Allocation Planning	25-Feb	7
2.1	(CORE) Decoder, Register Set, impl & integration	25-Feb	14
2.2	(CORE) Register set impl & integration	04-Mar	14
2.3	(CORE) Local memory impl & integration	11-Mar	14
X	Intense Coursework/Test month	04-Mar	31
3.1	(CORE) Memory mapped register layout & impl	01-Apr	21
3.2	(CORE) Wishbone peripheral bus connected to MMU	08-Apr	21
3.3	(CORE) Pipelined implementation and verification	15-Apr	21
3.1	(CORE) Cache memory design & impl	22-Apr	28
4.1	(CORE) Multi-core communication interface		
4.2	(CORE) Shared-memory controller		
4.4	(CORE) Scalable multi-core interface (10s of cores)		
4.3	(CORE) Multi-core example program (reduction)		
5.1	(EXT) SPI-FPGA interface for OTG programming		14
5.2	(EXT) FPGA-PC interfacing		28
5.3	(EXT) FPGA-PC debugging (instruction breakpoints)		28
6.1	(EXT) Compiler backend for vmicro16		7
6.2	(EXT) Compiler support for multi-core codegen		21
7.1	(CORE) Wishbone peripherals for demo	01-Aug	7
8	Final Report	11-Mar	150

Figure 1: Deliverables have been formalised and their development has been broken up into stages. Green/yellow colour simply identifies tasks in a new stage.

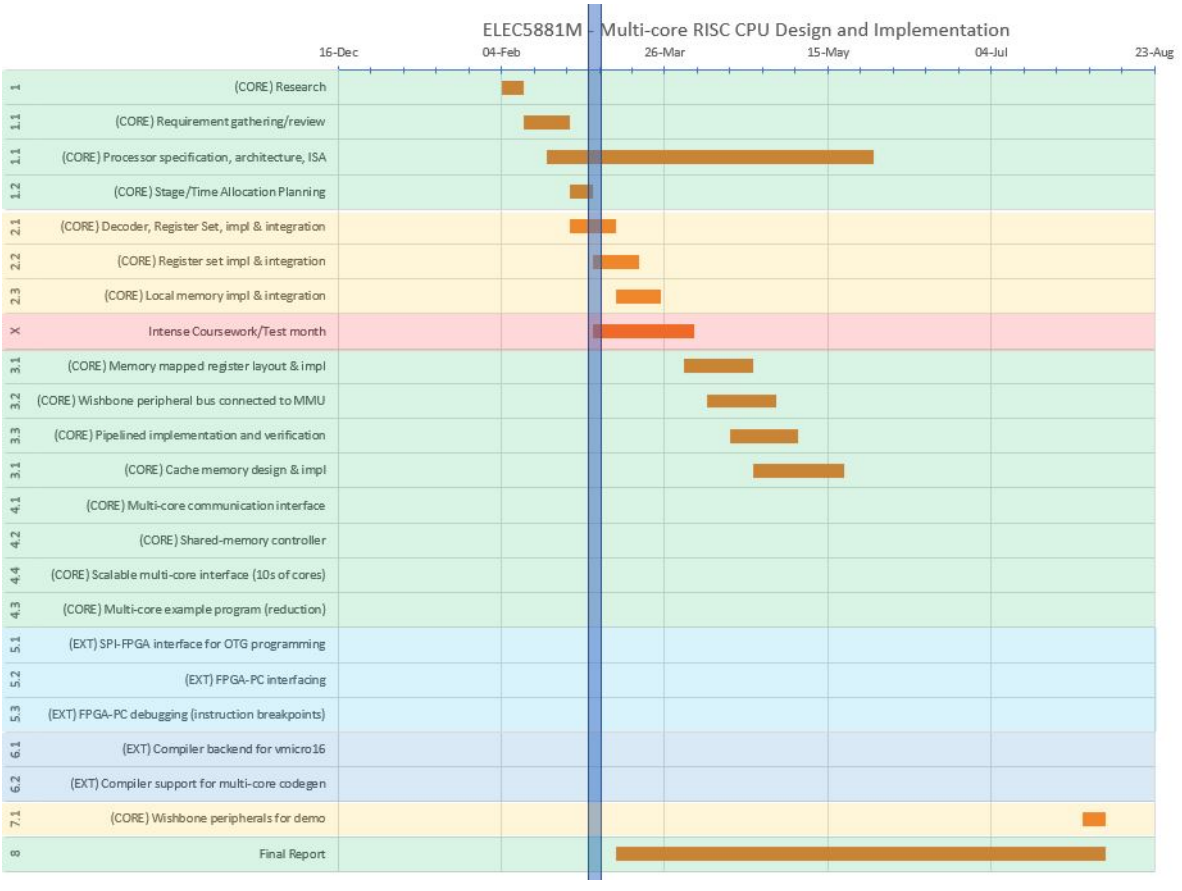

Figure 2: Visualisation of the stages in a Gantt chart.

3 Risks and Challenges

Urgent risks:

- RC2: Multiple tests and deadlines for other modules.

New risks
Existing risks
Resolved risks

3.1 Project Management

- RC1: Project planning not adequately performed. The project should be broken down into smaller tasks and each task should be assigned a priority and timeslot.

3.2 Other

There are currently no additional risks/challenges.