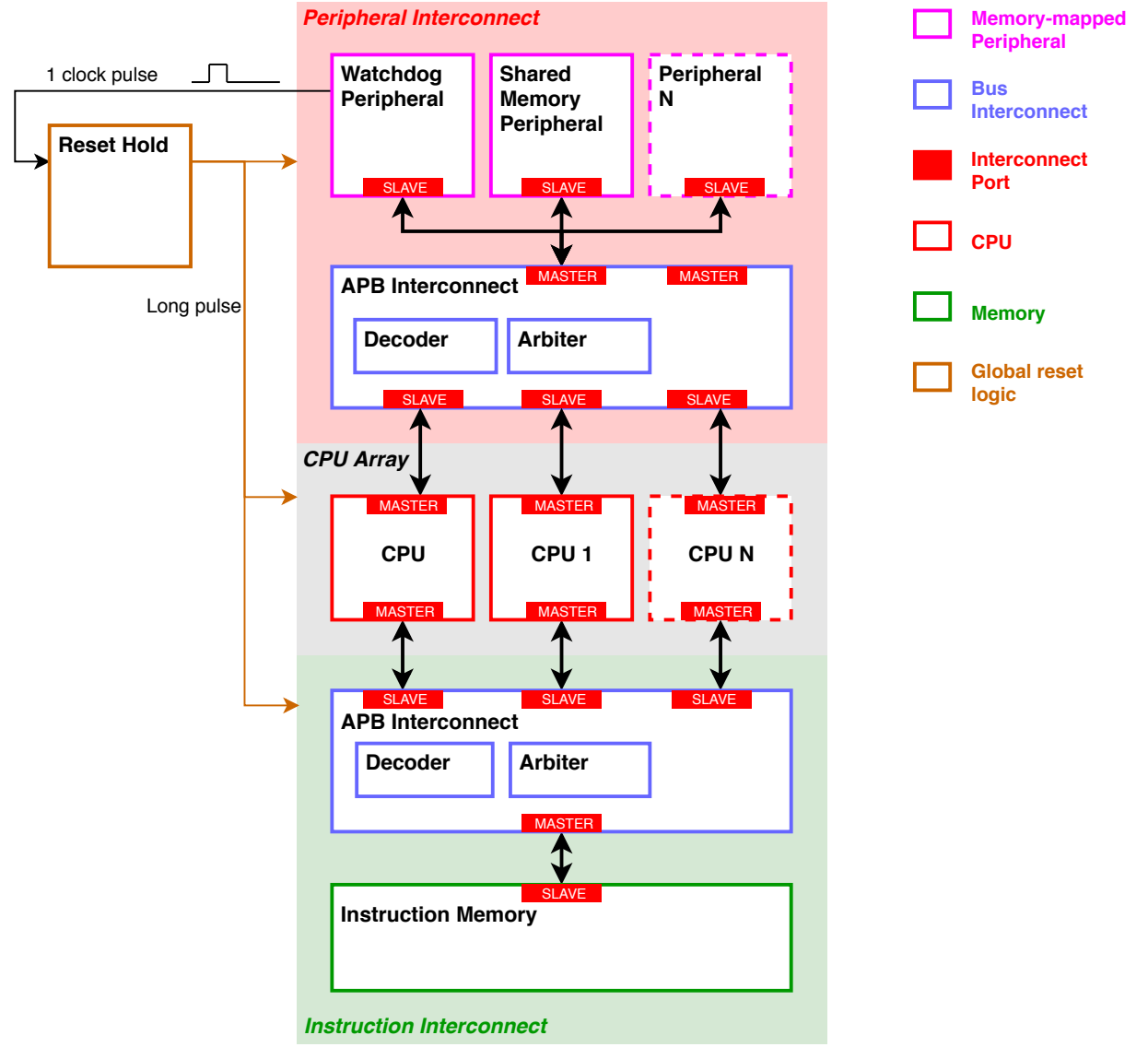
Peripheral Interconnect
1 clock pulse
Reset Hold
Long pulse
Watchdog Peripheral
Shared Memory Peripheral
Peripheral N
SLAVE
SLAVE
SLAVE
APB Interconnect
MASTER
MASTER
Decoder
Arbiter
SLAVE
SLAVE
SLAVE
CPU Array
MASTER
CPU
MASTER
MASTER
CPU 1
MASTER
MASTER
CPU N
MASTER
SLAVE
SLAVE
SLAVE
APB Interconnect
Decoder
Arbiter
MASTER
SLAVE
Instruction Memory
Instruction Interconnect
Memory-mapped Peripheral
Bus Interconnect
Interconnect Port
CPU
Memory
Global reset logic