Multi-core RISC Processor Design & Implementation

Demonstration Viva

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ELEC5881M - Main Project

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Why Multi-core?

Block Title

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Why RISC?

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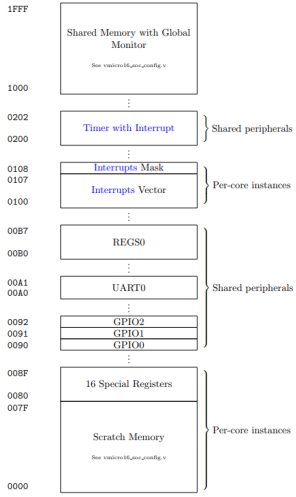
- **Software/Assembly compiler**
  PRCO304 programming language/Intel assembly syntax.

Top Level Hierarchy

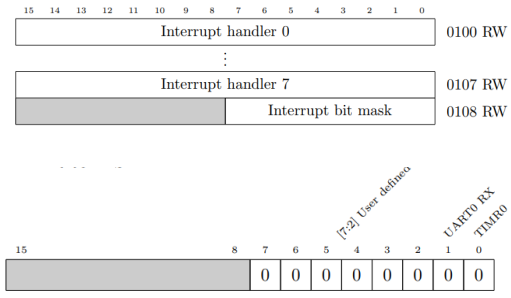
Memory Map



- **Shared Memory with Global Monitor**
- Timer with Interrupt
- Per-core Interrupt Vector and Mask
- Shared Register Set
- UART Transceiver
- Multiple GPIO ports
- Per-core scratch memory
- **Per-core Special Registers**
- Customisable by designers

Interconnect

Interrupts




```
1  entry:
2      // Set interrupt vector at 0x100
3      // Move address of isr0 function to vector[0]
4      movi    r0, isr0
5      // create 0x100 value by left shifting 1 8 bits
6      movi    r1, #0x1
7      movi    r2, #0x8
8      lshft   r1, r2
9      // write isr0 address to vector[0]
10     sw      r0, r1
11
12     // enable all interrupts by writing 0x0f to 0x108
13     movi    r0, #0x0f
14     sw      r0, r1 + #0x8
15     halt                    // enter low power idle state
16
17 isr0:                       // arbitrary name
18     movi    r0, #0xff       // do something
19     intr                    // return from interrupt
```

Demo: 2 Core LED toggle (GPIO0) with TIMR0 1s interrupt (interrupts_2.s)

Timer Interrupt Example

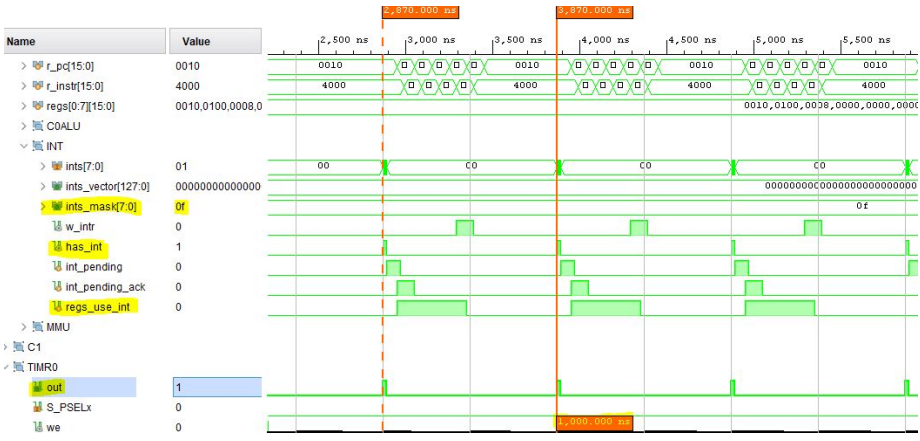


Figure: TIMR0 1us interrupt with context switching

HW/SW Requirements

Hardware:

- **Bus Arbitration**
  (scheduling: priority, rotating, etc.)

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Software:

- Semaphores/Mutexes
  (exclusive memory access)
- Thread synchronisation
  (memory barriers)
- **Context identification**
  What core am I?
  How many cores?
  How much memory?

Context Identification

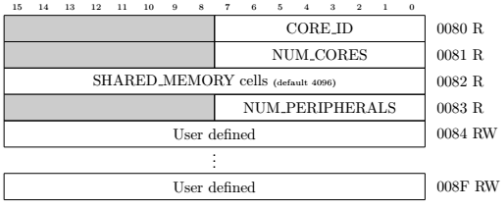

Figure: Special Registers 0x0080 to 0x008F

```
entry:
    // get core idx 0x80 in r7
    movi    r7, #0x80
    lw      r7, r7

    // Branch away if not core 0
    cmp     r7, r0
    movi    r0, exit
    br      r0, BR_NE

    // Core 0 only instructions
    nop     r0, r0
    nop     r0, r0
    nop     r0, r0

exit:
    halt    r0, r0
```

Results

Results 1

1 Introduction

2 Top Level Design

3 Multi-core Functionality

4 Results

5 Conclusion

Accomplishments

Future Improvements

Accomplishments

- **Near complete System-on-Chip design with various peripherals**
  Timers, GPIO, UART, Registers, Memory
- **Common multi-thread/core synchronisation primitives**
  Semaphores, Mutexes, Memory Barriers, Atomic Instructions
- **AMBA APB bus interface with Global Monitor**
  Timers, GPIO, UART, Registers, Memory
- **Working shared bus arbitration**
  Schedules access to shared resources
- **Working FPGA implementation for a 96 core design**
  Nearly fills Cyclone V FPGA on the DE1-SoC
- **Interrupts with hardware context-switching**
  Low latency to react to interrupt
- **Acknowledges design limitations and attempts to overcome**
  LUT resources, block memories, power and temperature requirements

Future Improvements

- **Working Global Reset**
  Timers, GPIO, UART, Registers, Memory
- **Common multi-thread/core synchronisation primitives**
  Semaphores, Mutexes, Memory Barriers, Atomic Instructions
- **AMBA APB bus interface with Global Monitor**
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