Multi-core RISC Processor Design and Implementation (Rev. 1.00)

ELEC5881M - Interim Report

Ben David Lancaster
Student ID: 201280376

Submitted in accordance with the requirements for the degree of
Master of Science (MSc)
in Embedded Systems Engineering

Supervisor: Dr. David Cowell
Assessor: Mr David Moore

University of Leeds
School of Electrical and Electronic Engineering

April 11, 2019

Revision History

Date	Version	Changes
20/05/2018	3.14	Add background research to appendix.
19/05/2018	3.13	Update abstract to align with guidelines.
19/05/2018	3.12	Fix ISA pseudo-codes.
11/03/2018	1.00	Initial section outline.

Table 1: Document revisions.

Abstract

Lorem ipsum dolor sit amet, consectetuer adipiscing elit. Ut purus elit, vestibulum ut, placerat ac, adipiscing vitae, felis. Curabitur dictum gravida mauris. Nam arcu libero, nonummy eget, consectetuer id, vulputate a, magna. Donec vehicula augue eu neque. Pellentesque habitant morbi tristique senectus et netus et malesuada fames ac turpis egestas. Mauris ut leo. Cras viverra metus rhoncus sem. Nulla et lectus vestibulum urna fringilla ultrices. Phasellus eu tellus sit amet tortor gravida placerat. Integer sapien est, iaculis in, pretium quis, viverra ac, nunc. Praesent eget sem vel leo ultrices bibendum. Aenean faucibus. Morbi dolor nulla, malesuada eu, pulvinar at, mollis ac, nulla. Curabitur auctor semper nulla. Donec varius orci eget risus. Duis nibh mi, congue eu, accumsan eleifend, sagittis quis, diam. Duis eget orci sit amet orci dignissim rutrum.

Nam dui ligula, fringilla a, euismod sodales, sollicitudin vel, wisi. Morbi auctor lorem non justo. Nam lacus libero, pretium at, lobortis vitae, ultricies et, tellus. Donec aliquet, tortor sed accumsan bibendum, erat ligula aliquet magna, vitae ornare odio metus a mi. Morbi ac orci et nisl hendrerit mollis. Suspendisse ut massa. Cras nec ante. Pellentesque a nulla. Cum sociis natoque penatibus et magnis dis parturient montes, nascetur ridiculus mus. Aliquam tincidunt urna. Nulla ullamcorper vestibulum turpis. Pellentesque cursus luctus mauris.

Nulla malesuada porttitor diam. Donec felis erat, congue non, volutpat at, tincidunt tristique, libero. Vivamus viverra fermentum felis. Donec nonummy pellentesque ante. Phasellus adipiscing semper elit. Proin fermentum massa ac quam. Sed diam turpis, molestie vitae, placerat a, molestie nec, leo. Maecenas lacinia. Nam ipsum ligula, eleifend at, accumsan nec, suscipit a, ipsum. Morbi blandit ligula feugiat magna. Nunc eleifend consequat lorem. Sed lacinia nulla vitae enim. Pellentesque tincidunt purus vel magna. Integer non enim. Praesent euismod nunc eu purus. Donec bibendum quam in tellus. Nullam cursus pulvinar lectus. Donec et mi. Nam vulputate metus eu enim. Vestibulum pellentesque felis eu massa.

Acknowledgements

I would like to thank my project supervisors Nigel Barlow and Serge Thill for their support and guidance throughout this project.

I would also like to thank James Spalding (Spirent Communications) and firmware team for their encouragement, ideas, and industrial sponsorship supporting this final project.

Declaration of Academic Integrity

The candidate confirms that the work submitted is his/her own, except where work which has formed part of jointly-authored publications has been included. The contribution of the candidate and the other authors to this work has been explicitly indicated in the report. The candidate confirms that appropriate credit has been given within the report where reference has been made to the work of others.

This copy has been supplied on the understanding that no quotation from the report may be published without proper acknowledgement. The candidate, however, confirms his/her consent to the University of Leeds copying and distributing all or part of this work in any forms and using third parties, who might be outside the University, to monitor breaches of regulations, to verify whether this work contains plagiarised material, and for quality assurance purposes.

The candidate confirms that the details of any mitigating circumstances have been submitted to the Student Support Office at the School of Electronic and Electrical Engineering, at the University of Leeds.

Name: Ben David Lancaster
Date: April 11, 2019

Table of Contents

[1] [2] [3]

References

[1] J. Balkind, M. McKeown, Y. Fu, T. Nguyen, Y. Zhou, A. Lavrov, M. Shahrad, A. Fuchs, S. Payne, X. Liang *et al.*, "Openpiton: An open source manycore research framework," in *ACM SIGARCH Computer Architecture News*, vol. 44, no. 2. ACM, 2016, pp. 217–232.

[2] N. Satish, M. Harris, and M. Garland, "Designing efficient sorting algorithms for manycore gpus," in *2009 IEEE International Symposium on Parallel & Distributed Processing*. IEEE, 2009, pp. 1–10.

[3] S. Binet, P. Calafiura, S. Snyder, W. Wiedenmann, and F. Winklmeier, "Harnessing multicores: Strategies and implementations in atlas," in *Journal of Physics: Conference Series*, vol. 219, no. 4. IOP Publishing, 2010, p. 042002.

Chapter 1

Abstract (not in toc)

Chapter 2

Declaration of Academic Integrity (not in toc)

Chapter 3

Acknowledgements (not in toc)

Chapter 4

Introduction

4.1 Why Multi-core?

4.2 Why RISC?

4.3 Why FPGA?

Chapter 5

Background

5.1 Single core vs. Multi-core vs. Many-core

5.2 Network-on-chip

5.2.1 OpenPiton

5.3 Summary

Chapter 6

Project Management

6.1 Project Deliverables

The project's deliverables are split into two sections: core deliverables (CD) – each deliverable must be satisfied for the project to be a minimum viable product (MVP), and extended deliverables (ED) – deliverables that are not required for an MVP, features that only improve upon an existing feature.

6.1.1 Core Deliverables (CD)

The project's core deliverables are described below.

CD1. Design a compact 16-bit RISC instruction set architecture.

CD2. Produce a synthesisable Verilog RISC core that implements the ISA in **CD1.**.

CD3. Design and implement an on-chip interconnect for multi-core processing (between 2 to 32 cores) using the RISC core from **CD2.**.

CD4. Analyse performance of serial and parallel software algorithms, such as parallel DFT [**?**], on the processor.

6.1.2 Extended Deliverables (ED)

The project's extended deliverables are described below.

ED1. Produce a RISC core with an instructions-per-clock (IPC) rating of at least 1.0 (a single-cycle CPU).

ED2. Produce a scalable multi-core interconnect supporting arbitrary (more than 32) RISC core instances (manycore) using Network-on-Chip (NoC) architecture.

ED3. Produce a compiler-backend for the PRCO304 [**?**] compiler to support the ISA from1 **CD1.**. This will make it easier to build complex multi-core software for the processor.

6.2 Project Timeline

6.2.1 Project Stages

6.2.2 Timeline

6.3 Resources

6.3.1 Terasic DE1-SoC Development Board

6.3.2 Minispartan 6+ FPGA Development Board

Chapter 7

Current Progress

7.1 RISC Core

7.1.1 Instruction Set Architecture

7.1.2 Implementation

7.1.3 Verification

Chapter 8

Future Progress

8.1 Multi-core Functionality

8.2 Interconnect Goals

8.3 Interconnect Layout

8.3.1 Bus Design

8.3.2 Core Pin Assignments

8.4 Core-to-core Communication

8.5 Shared-Resource Control

8.5.1 Resource Scheduling

8.6 Verification

8.7 Conclusion

Chapter 9

RISC Core Design

9.1 Design Goals

9.2 Instruction Set Architecture

9.2.1 Data Sizes

9.2.2 Registers

9.2.3 Endianness

9.3 High Level Design

9.4 Memory-mapped peripherals

9.4.1 Wishbone Master Bus

9.5 Optimisations

9.5.1 Pipelining

9.5.2 Stall Avoidance

9.6 Core Verification

9.7 Conclusion

Chapter 10

Multi-core Communication Design

10.1 Interconnect Goals

10.2 Interconnect Layout

10.2.1 Bus Design

10.2.2 Core Pin Assignments

10.3 Core-to-core Communication

10.4 Shared-Resource Control

10.4.1 Resource Scheduling

10.5 Verification

10.6 Conclusion

Chapter 11

Core Analysis

11.1 FPGA Implementation Analysis

11.1.1 Space/Resource Usage

11.1.2 Static Timing Analysis

11.2 Speed Analysis

11.2.1 Parallel Reduction Algorithms

11.2.2 Parallel DFT Algorithm

Chapter 12

Conclusion

12.1 RISC Core Review

12.2 Multi-core Review

12.3 Verification Review

12.4 Goal Review