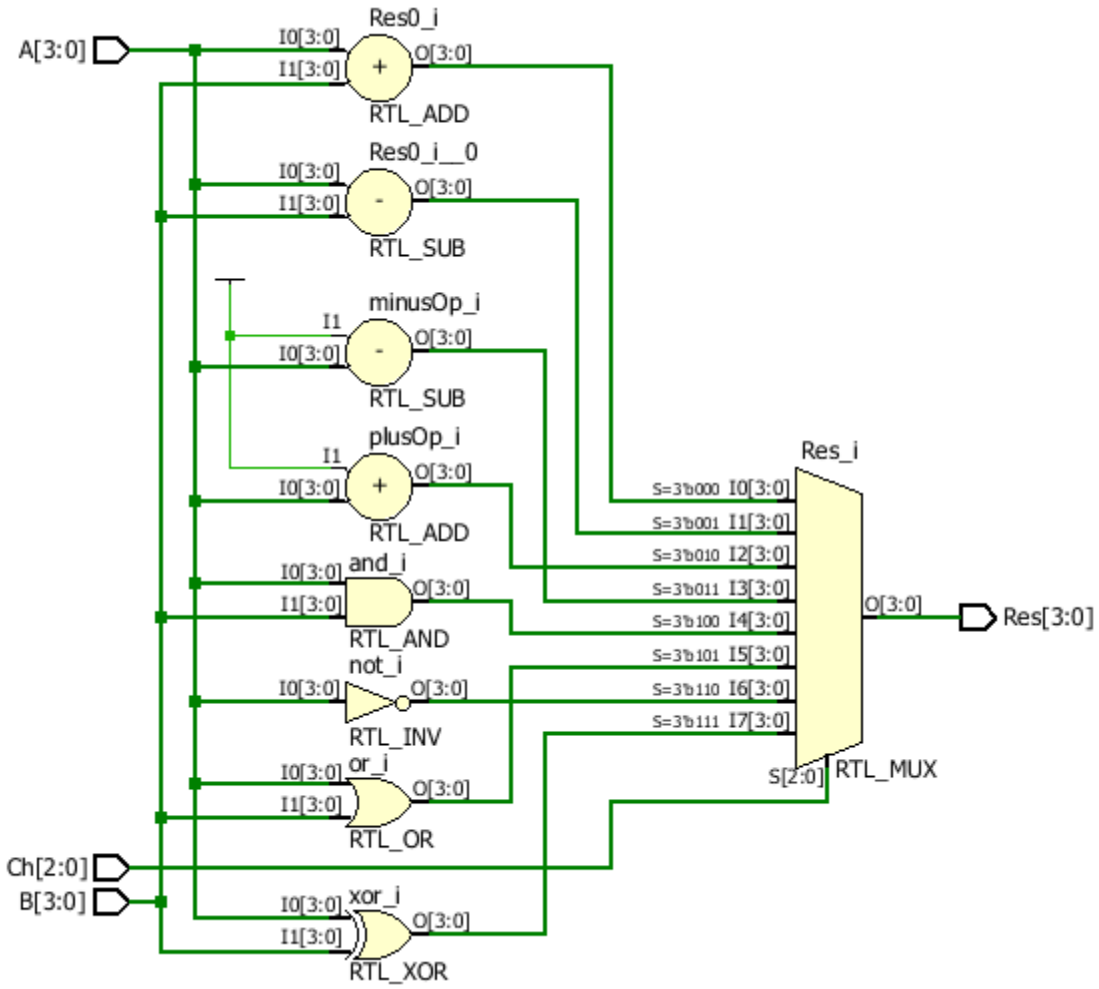
ALU Model (Behavioral):

VHDL code:

```
use IEEE.NUMERIC_STD.ALL;

entity alu_b is
    Port ( A : in unsigned (3 downto 0);
           B : in unsigned (3 downto 0);
           Ch : in STD_LOGIC_VECTOR (2 downto 0);
           Res : out unsigned (3 downto 0));
end alu_b;


architecture Behavioral of alu_b is


begin
    process(A,B,Ch)
    begin
    case Ch is
       when "000"=>Res<=A+B;
       when "001"=>Res<=A-B;
       when "010"=>Res<=A+1;
       when "011"=>Res<=A-1;
       when "100"=>Res<=A AND B;
       when "101"=>Res<=A OR B;
       when "110"=>Res<=NOT A;
       when "111"=>Res<=A XOR B;
       when others=>NULL;
    end case;
    end process;
```

end Behavioral;

RTL Diagram:



TBW Code:

entity alu_b_tb is

-- Port ( );

end alu_b_tb;

architecture Behavioral of alu_b_tb is

component alu_b is

Port (A : in unsigned (3 downto 0);

B : in unsigned (3 downto 0);

```
        Ch : in STD_LOGIC_VECTOR (2 downto 0);
        Res : out unsigned (3 downto 0));
end component;

signal A1 : unsigned (3 downto 0) := "1000";
signal B1 : unsigned (3 downto 0) := "0010";
signal Ch1 : STD_LOGIC_VECTOR (2 downto 0) := "000";
signal Res1 : unsigned (3 downto 0);

begin
uut: alu_b port map (A=>A1, B=>B1, Ch=>Ch1, Res=>Res1);
stim_proc: process
begin
wait for 100ns;
Ch1 <= "000";
wait for 100ns;
Ch1 <= "001";
wait for 100ns;
Ch1 <= "010";
wait for 100ns;
Ch1 <= "011";
wait for 100ns;
Ch1 <= "100";
wait for 100ns;
Ch1 <= "101";
wait for 100ns;
Ch1 <= "110";
```

wait for 100ns;

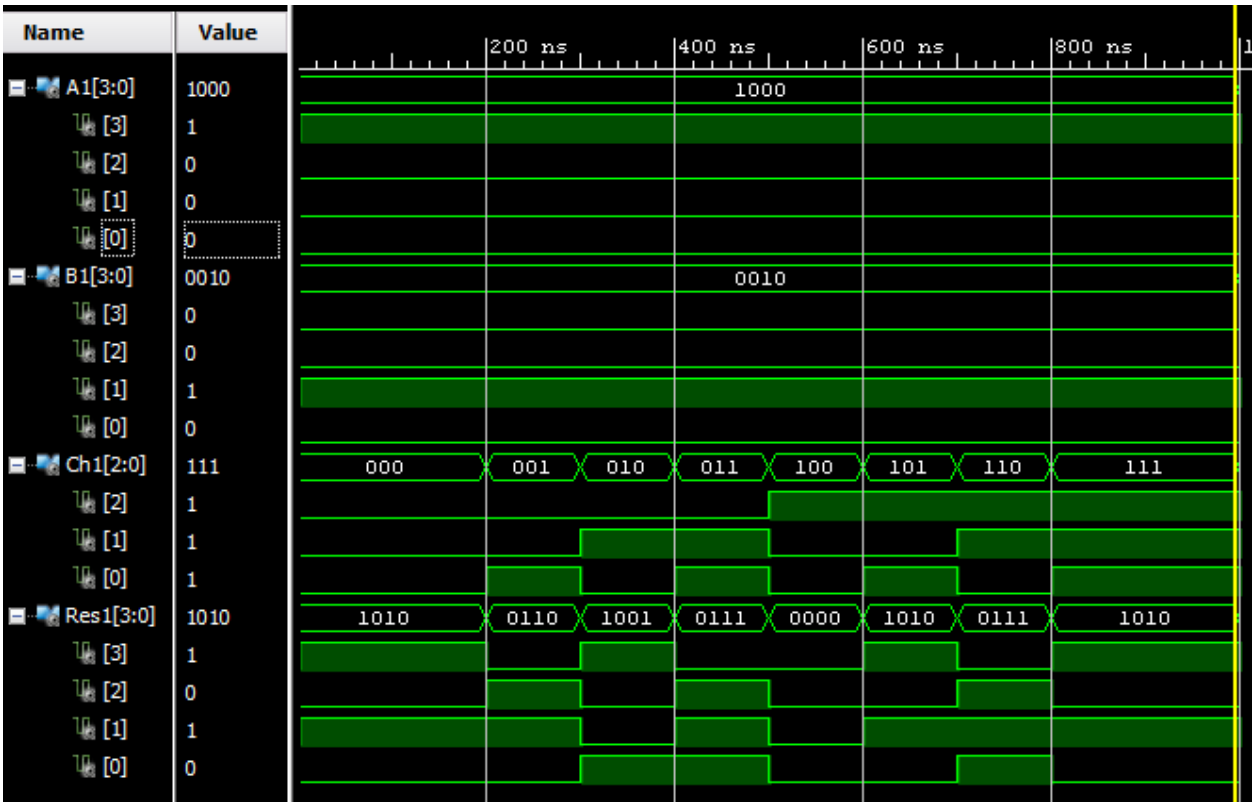
Ch1 <= "111";

wait;

end process;

end Behavioral;

Waveform:



Full Adder (Structural):

VHDL code:

entity full_adder_structural is

Port (X : in STD_LOGIC;

Y : in STD_LOGIC;

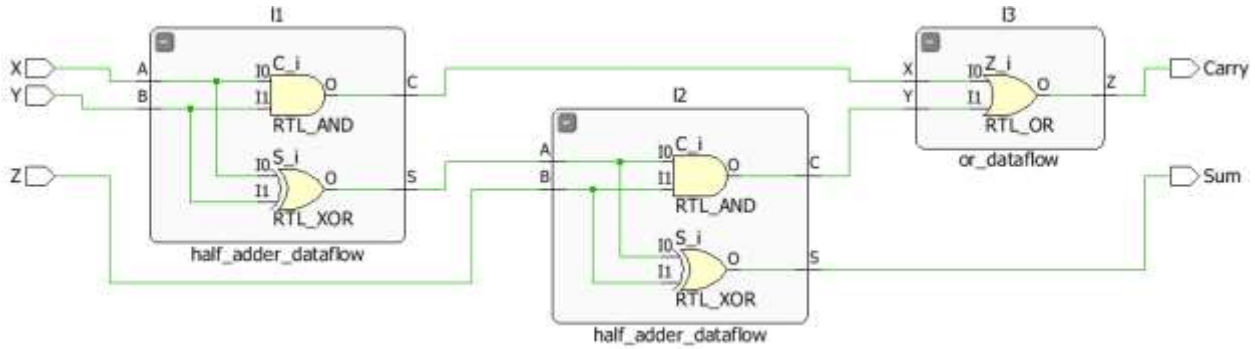
Z : in STD_LOGIC;

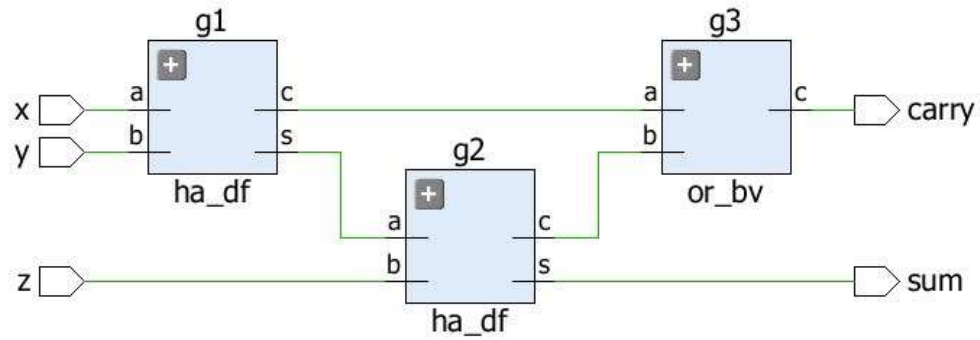
Sum : out STD_LOGIC;

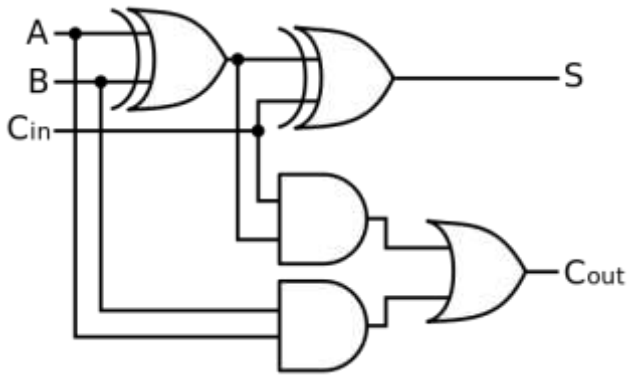
```
        Carry : out STD_LOGIC);
end full_adder_structural;

architecture Structural of full_adder_structural is

component half_adder_dataflow is
    Port ( A : in STD_LOGIC;
        B : in STD_LOGIC;
        S : out STD_LOGIC;
        C : out STD_LOGIC);
end component;

component or_dataflow is
    Port ( X : in STD_LOGIC;
        Y : in STD_LOGIC;
        Z : out STD_LOGIC);
end component;

signal S1: STD_LOGIC;
signal C1: STD_LOGIC;
signal C2: STD_LOGIC;

begin

l1:half_adder_dataflow port map(X,Y,S1,C1);
l2:half_adder_dataflow port map(S1,Z,Sum,C2);
l3:or_dataflow port map(C1,C2,Carry);
```

end Structural;

RTL Diagram:







Day 4 Assignment

1 Design ALU with 4 logical and 4 arithmetic operations.

2 Design Structural model for 8:1 Mux using 4:1 and 2:1 Mux

3. Design Structural model for Full adder using half adder and or gate

Those who are in EDAplayground

Do Half Subtractor and Full Subtractor along with ALU