VHDL Lab Day3

Multiplexer

MULTIPLEXER

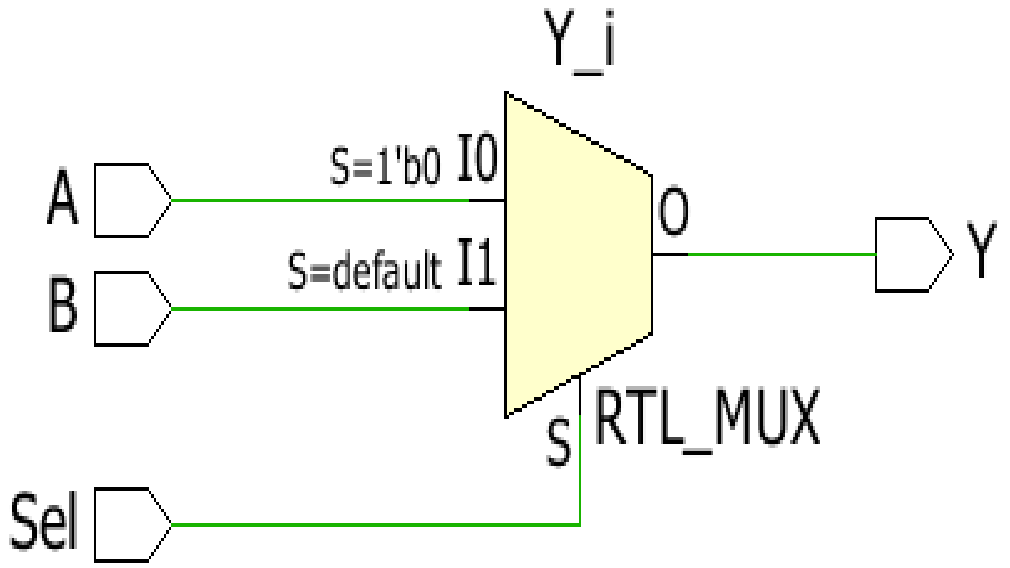
- A multiplexer (or **mux**) is a common digital circuit used to mix a lot of signals into just one.
- If we want multiple sources of data to share a single common data line, we have to use a multiplexer to run them into that line.
- Every multiplexer has at least one select line. (2^n inputs requires n select lines), which is used to select which input signal gets relayed to the output.
- In a 2-to-1 multiplexer, there's just one select line, 2 inputs and 1 output.
- Think of a mux as a "digital switch". The select line is the throw on the switch, it chooses which of the many inputs get to be the output.

2:1 MUX (Dataflow):

```
entity mux_2_1_dataflow is
    Port ( A : in STD_LOGIC;
           B : in STD_LOGIC;
           Sel : in STD_LOGIC;
           Y : out STD_LOGIC);
end mux_2_1_dataflow;


architecture Dataflow of mux_2_1_dataflow is


begin
    Y<=A when Sel='0' else B;
end Dataflow;
```



2:1 MUX (Behavioral):

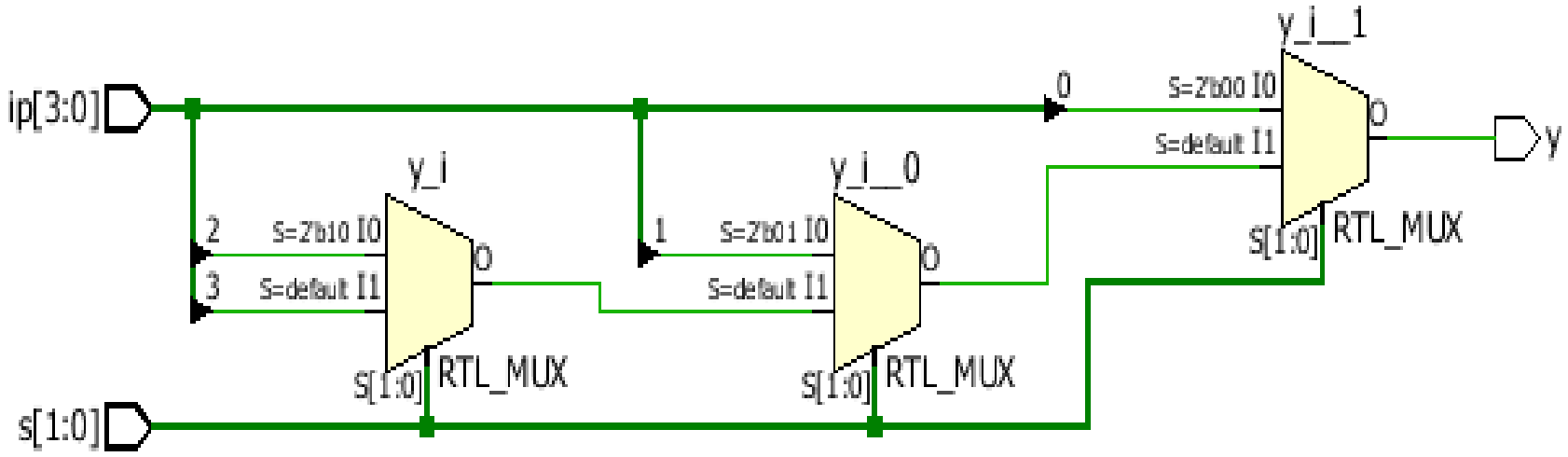
```
architecture Behavioral of mux_2_1_behavioral is
begin
    process(A,B,Sel)
    begin
    if(Sel='0')then
        Y<=A;
    else
        Y<=B;
    end if;
end process;
end Behavioral;
```

4:1 MUX (Dataflow):

VHDL code:

```
entity mux_4_1_dataflow is
    Port ( ip : in STD_LOGIC_VECTOR (3 downto 0);
           s : in STD_LOGIC_VECTOR (1 downto 0);
           y : out STD_LOGIC);
end mux_4_1_dataflow;
```

```
architecture Dataflow of mux_4_1_dataflow is
 begin
    y<=ip(0) when s="00" else
       ip(1) when s="01" else
       ip(2) when s="10" else
       ip(3);
end Dataflow;
```

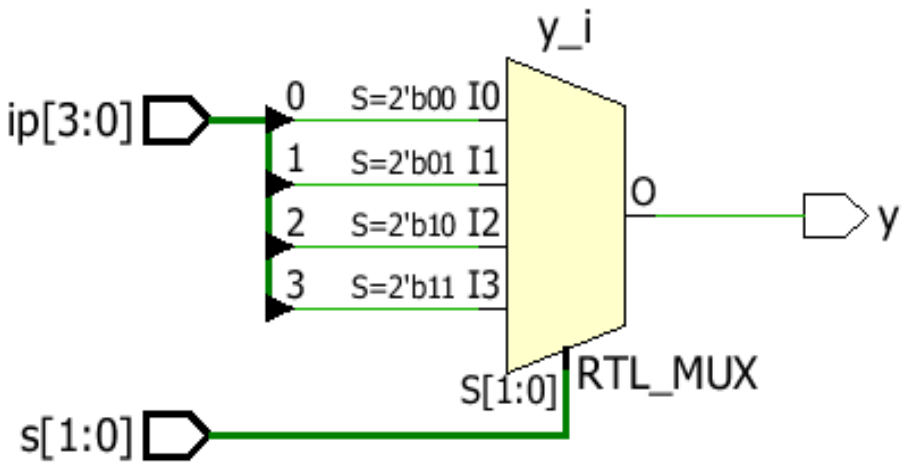


4:1 MUX (Behavioral):

VHDL code:

```
entity mux_4_1_behavioral is
    Port ( ip : in STD_LOGIC_VECTOR (3 downto 0);
           s : in STD_LOGIC_VECTOR (1 downto 0);
           y : out STD_LOGIC);
end mux_4_1_behavioral;

architecture Behavioral of mux_4_1_behavioral is
 begin
process(ip,s)
    begin
    case s is
        when "00" =>
            y<=ip(0);
        when "01" =>
            y<=ip(1);
        when "10" =>
            y<=ip(2);
        when "11" =>
            y<=ip(3);
        when others=>NULL;
    end case;
    end process;
end Behavioral;
```



TBW Code:

```
entity mux_4_1_behavioral_tb is
--    Port ( );
end mux_4_1_behavioral_tb;
architecture Behavioral of mux_4_1_behavioral_tb is
component mux_4_1_behavioral is
    Port ( ip : in STD_LOGIC_VECTOR (3 downto 0);
           s : in STD_LOGIC_VECTOR (1 downto 0);
           y : out STD_LOGIC);
end component;
signal ip1 : STD_LOGIC_VECTOR (3 downto 0) := "0101";
signal s1 : STD_LOGIC_VECTOR (1 downto 0) := "00";
signal y1 : STD_LOGIC;
begin
uut: mux_4_1_behavioral port map (ip=>ip1, s=>s1, y=>y1);
stim_proc: process
begin
wait for 100ns;
s1 <= "00";
wait for 100ns;
s1 <= "01";
wait for 100ns;
s1 <= "10";
wait for 100ns;
s1 <= "11";
wait;
end process;
end Behavioral;
```

3:8 Decoder (Dataflow):

VHDL code:

```
entity decoder_3_8_dataflow is
    Port ( ip : in STD_LOGIC_VECTOR (2 downto 0);
           op : out STD_LOGIC_VECTOR (7 downto 0));
end decoder_3_8_dataflow;
```

```
architecture Dataflow of decoder_3_8_dataflow is


begin
    op(0) <= '1' when ip="000" else '0';
    op(1) <= '1' when ip="001" else '0';
    op(2) <= '1' when ip="010" else '0';
    op(3) <= '1' when ip="011" else '0';
    op(4) <= '1' when ip="100" else '0';
    op(5) <= '1' when ip="101" else '0';
    op(6) <= '1' when ip="110" else '0';
    op(7) <= '1' when ip="111" else '0';
end Dataflow;
```

Comparator 4 Bit (Dataflow):

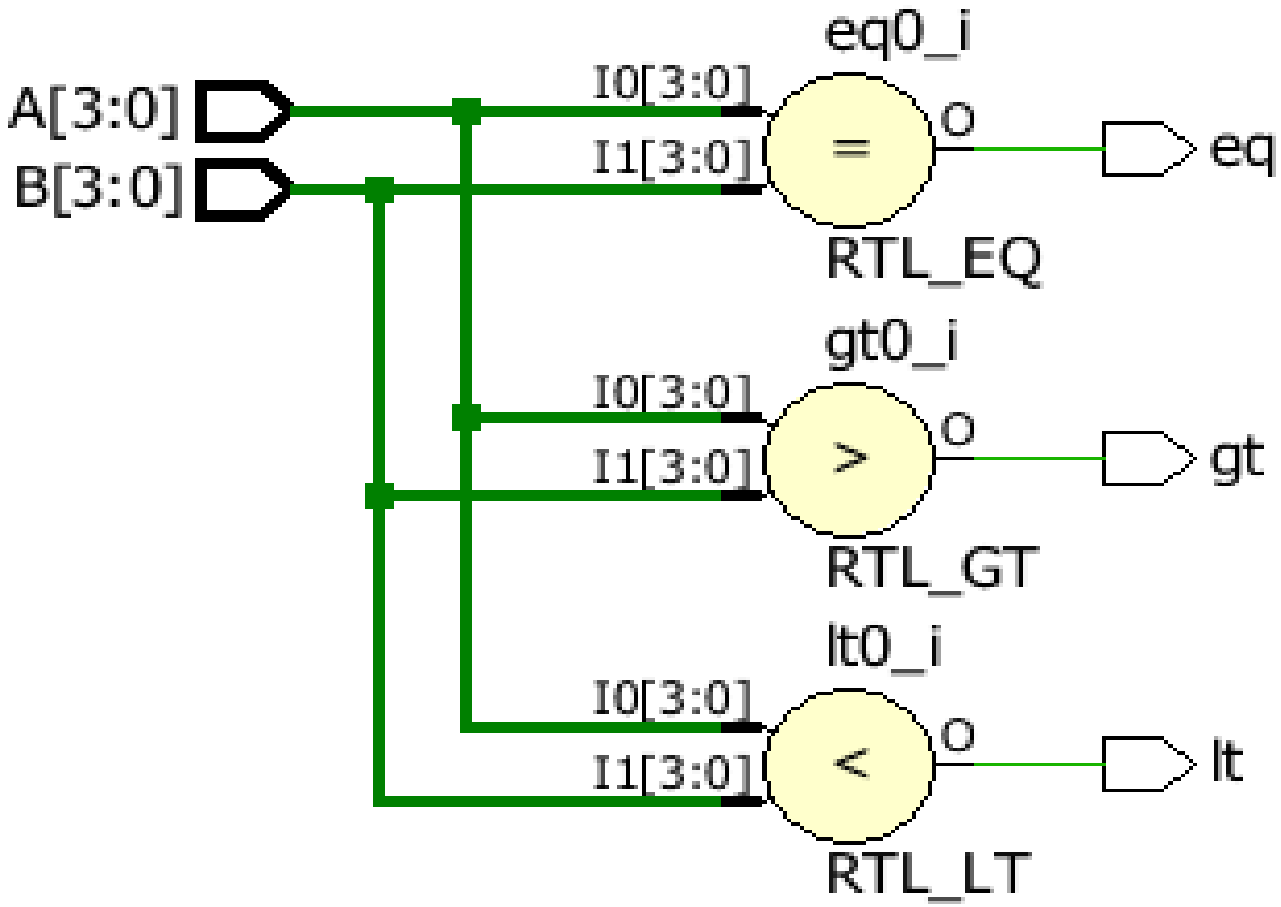
VHDL code:

```
entity comparator_4 is
    Port ( A : in STD_LOGIC_VECTOR (3 downto 0);
           B : in STD_LOGIC_VECTOR (3 downto 0);
           eq : out STD_LOGIC;
           gt : out STD_LOGIC;
           lt : out STD_LOGIC);
end comparator_4;
```

```
architecture Dataflow of comparator_4 is


begin
    eq<='1' when A=B else '0';
    gt<='1' when A>B else '0';
    lt<='1' when A<B else '0';
end Dataflow;
```

RTL Diagram:


A[3:0]
B[3:0]
eq0_i
I0[3:0]
I1[3:0]
=
O
eq
RTL_EQ
gt0_i
I0[3:0]
I1[3:0]
>
O
gt
RTL_GT
lt0_i
I0[3:0]
I1[3:0]
<
O
lt
RTL_LT

Assignment 3 Day 3

- Design and simulate Data Flow and Behavioural model of
- 2:1 Mux
- 4:1 Mux
- 3:8 Decoder
- Design Dataflow model of 4bits Comparator