ASSIGNMENT – III

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STREAM: CSE-A

ROLL NUMBER: 1951007

SUBJECT: COMPUTER ARCHITECTURE LAB

2:1 MUX

Dataflow:

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

entity mux\_2x1 is

Port ( A : in STD\_LOGIC;

B : in STD\_LOGIC;

Sel : in STD\_LOGIC;

Y : out STD\_LOGIC);

end mux\_2x1;

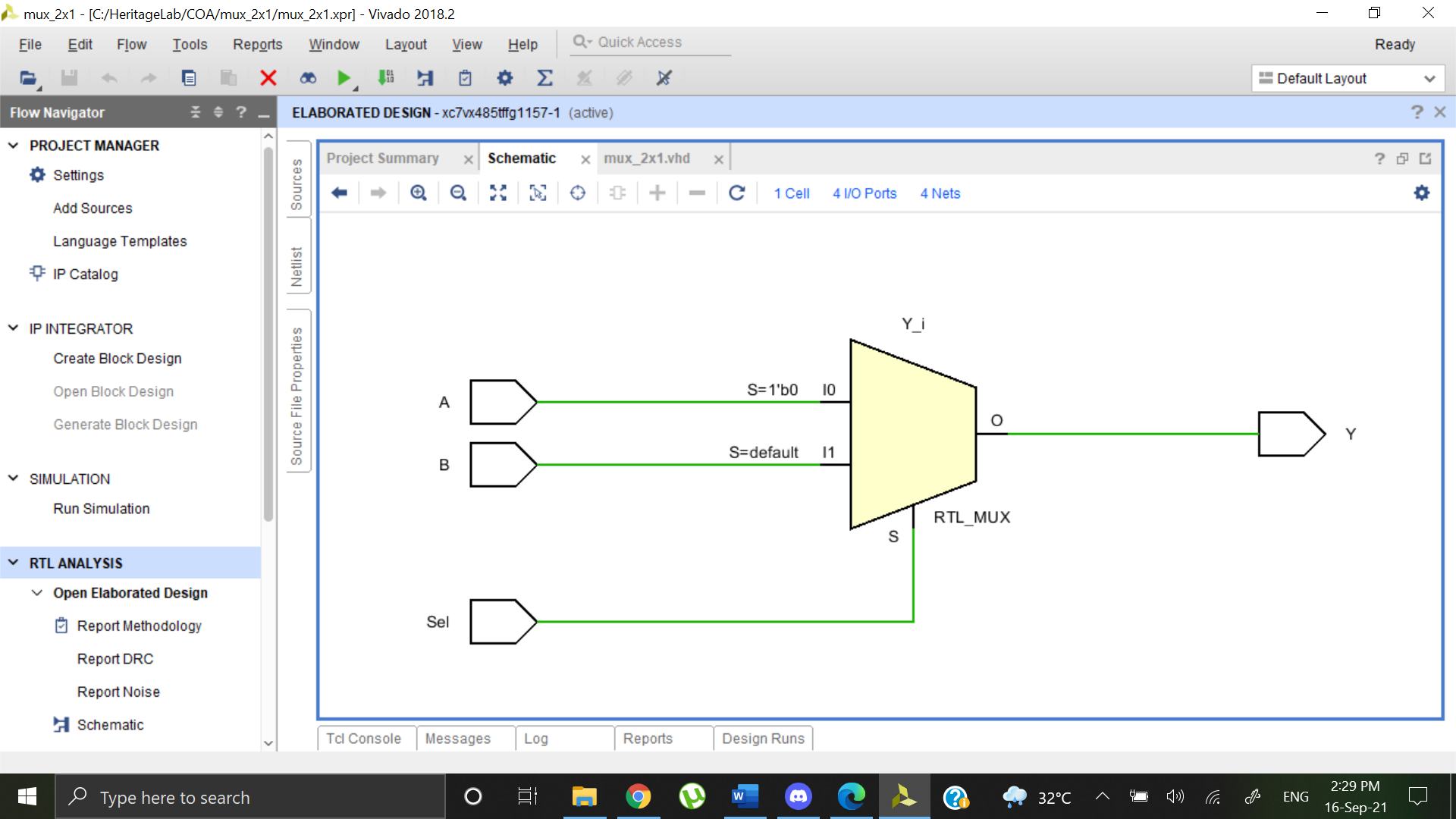
architecture Dataflow of mux\_2x1 is

begin

Y<=A when Sel='0' else B;

end Dataflow;

Elaborated Design:



Behavioral:

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

entity mux\_2x1 is

Port ( A : in STD\_LOGIC;

B : in STD\_LOGIC;

Sel : in STD\_LOGIC;

Y : out STD\_LOGIC);

end mux\_2x1;

architecture Behavioral of mux\_2x1 is

begin

process(A,B,Sel)

begin

if(Sel='0')then

Y<=A;

else

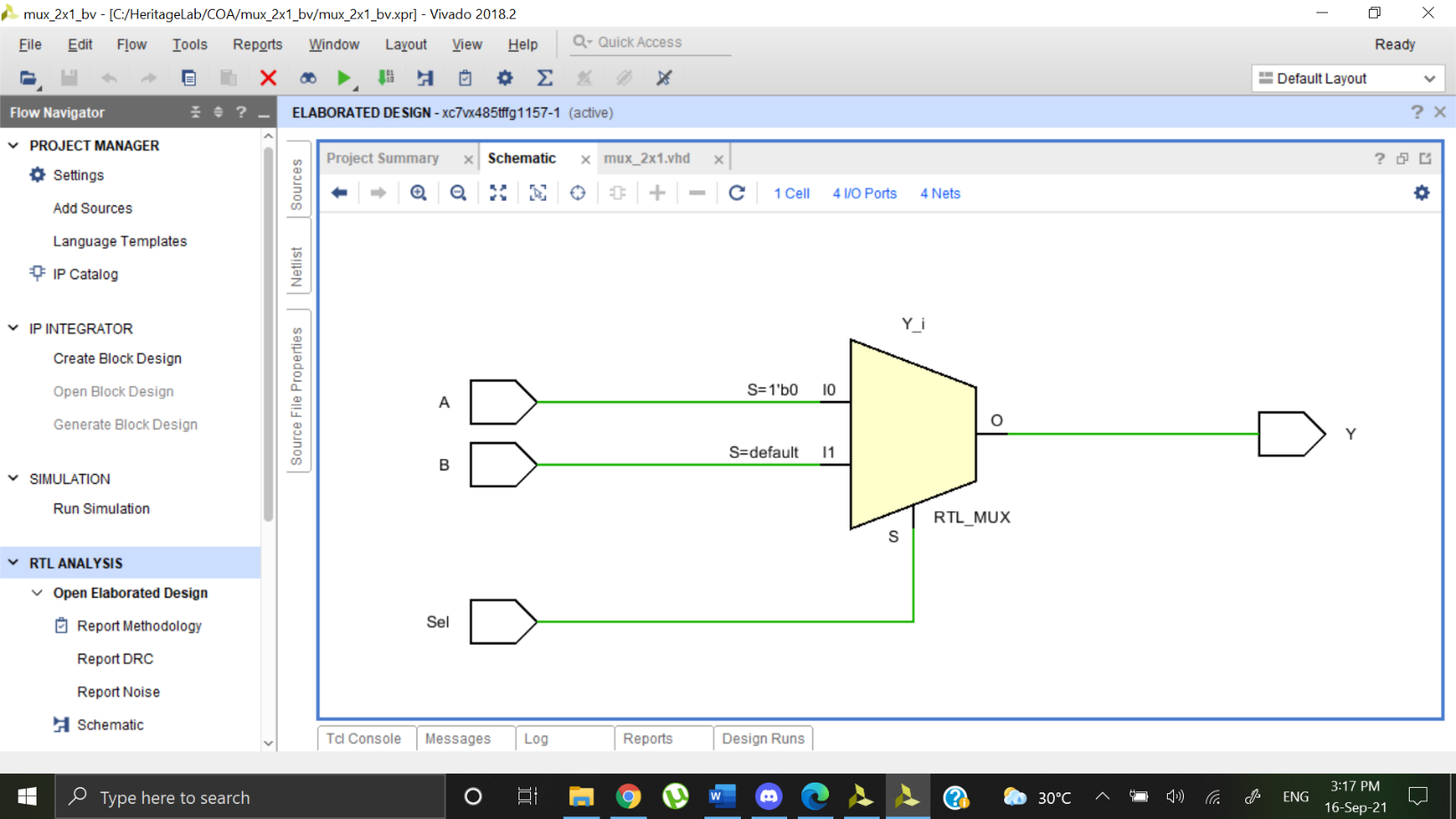
Y<=B;

end if;

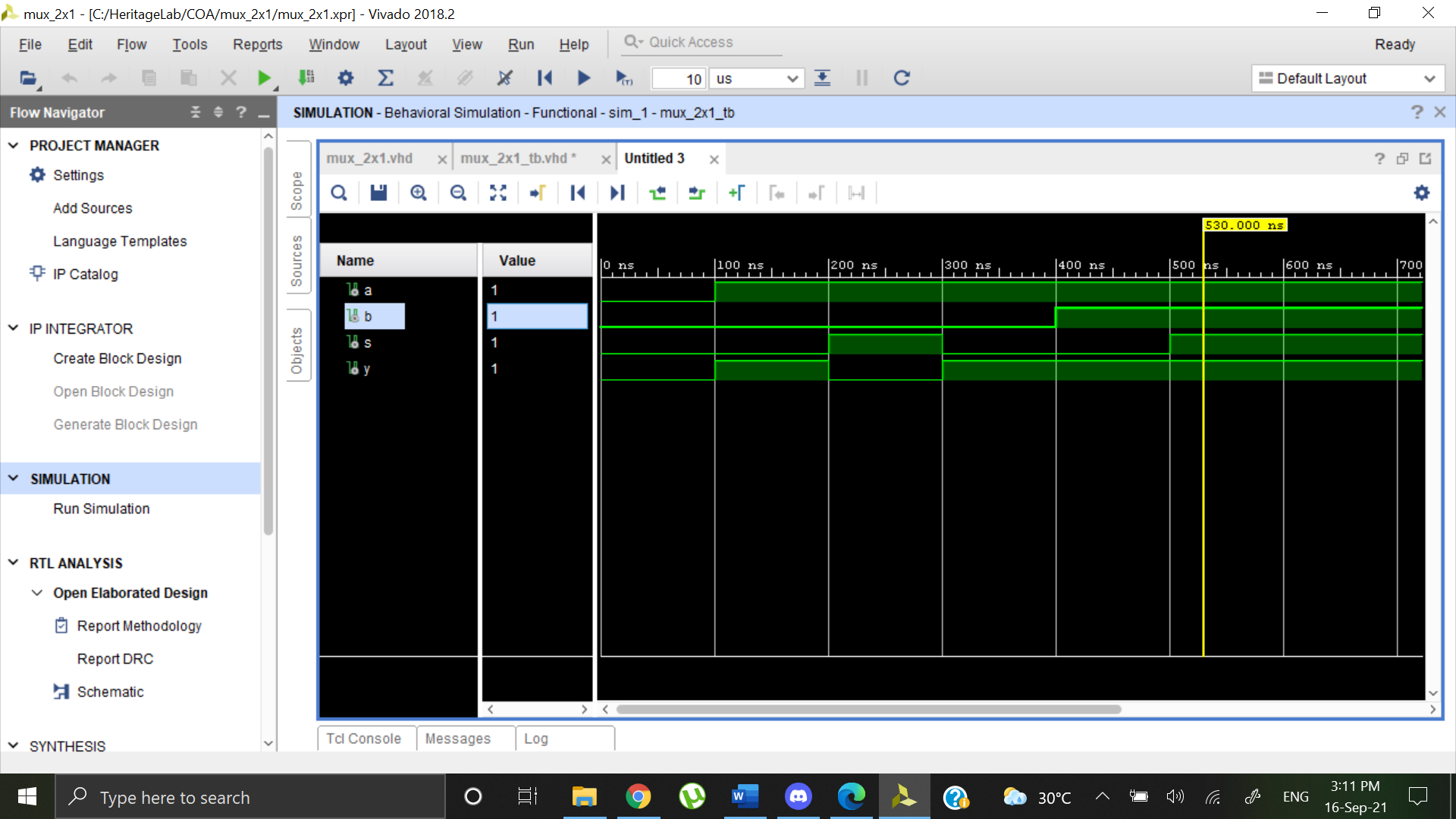
end process;

end Behavioral;

Elaborated Design:



Output Waveform:



4:1 MUX

Dataflow:

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

entity mux\_4x1 is

Port ( ip : in STD\_LOGIC\_VECTOR (3 downto 0);

s : in STD\_LOGIC\_VECTOR (1 downto 0);

y : out STD\_LOGIC);

end mux\_4x1;

architecture Dataflow of mux\_4x1 is

begin

y<=ip(0) when s="00" else

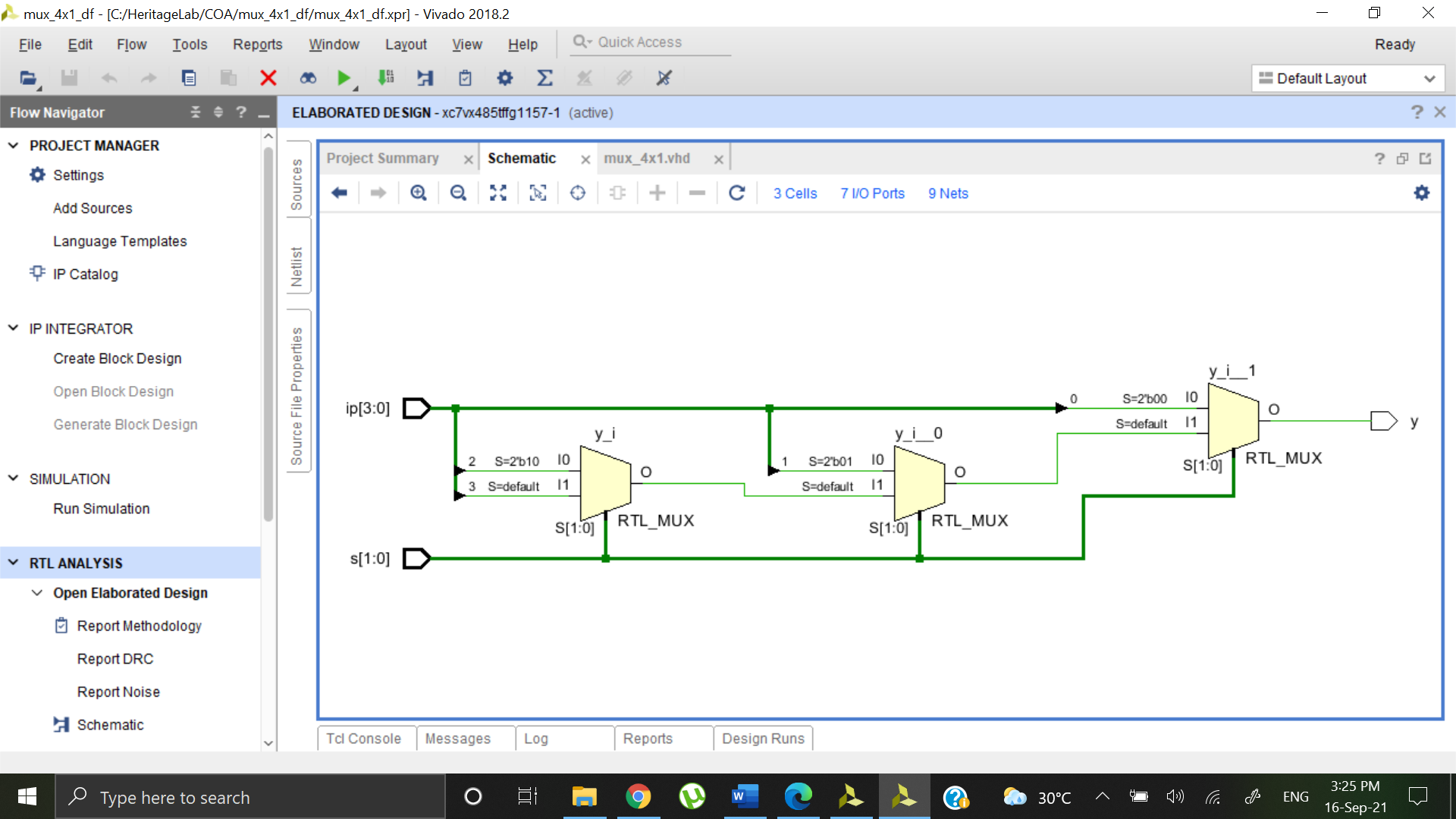
ip(1) when s="01" else

ip(2) when s="10" else

ip(3);

end Dataflow;

Elaborated Design:



Behavioral:

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

entity mux\_4x1 is

Port ( ip : in STD\_LOGIC\_VECTOR (3 downto 0);

s : in STD\_LOGIC\_VECTOR (1 downto 0);

y : out STD\_LOGIC);

end mux\_4x1;

architecture Behavioral of mux\_4x1 is

begin

process(ip,s)

begin

case s is

when "00" => y<=ip(0);

when "01" => y<=ip(1);

when "10" => y<=ip(2);

when "11" => y<=ip(3);

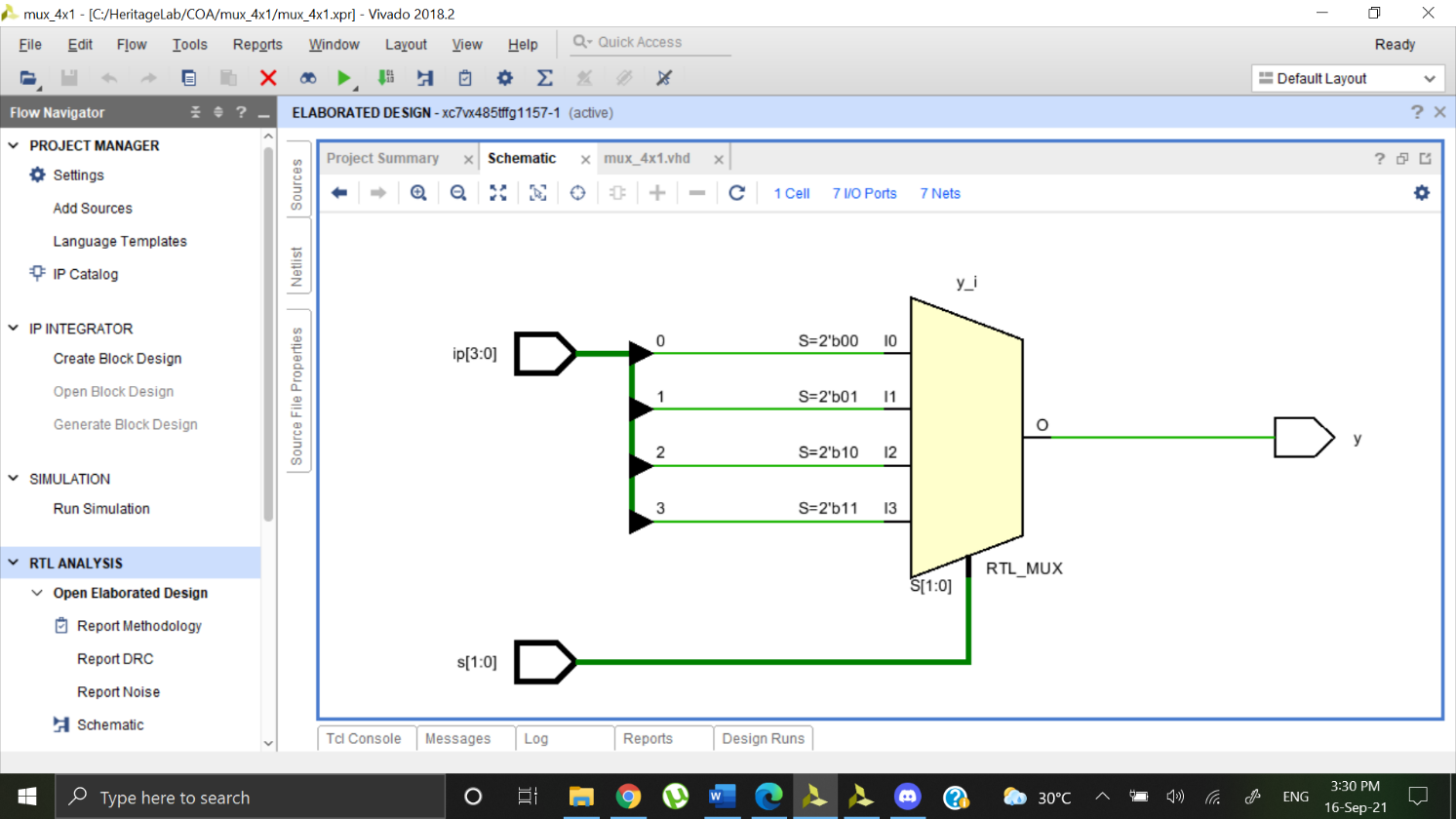
when others=>NULL;

end case;

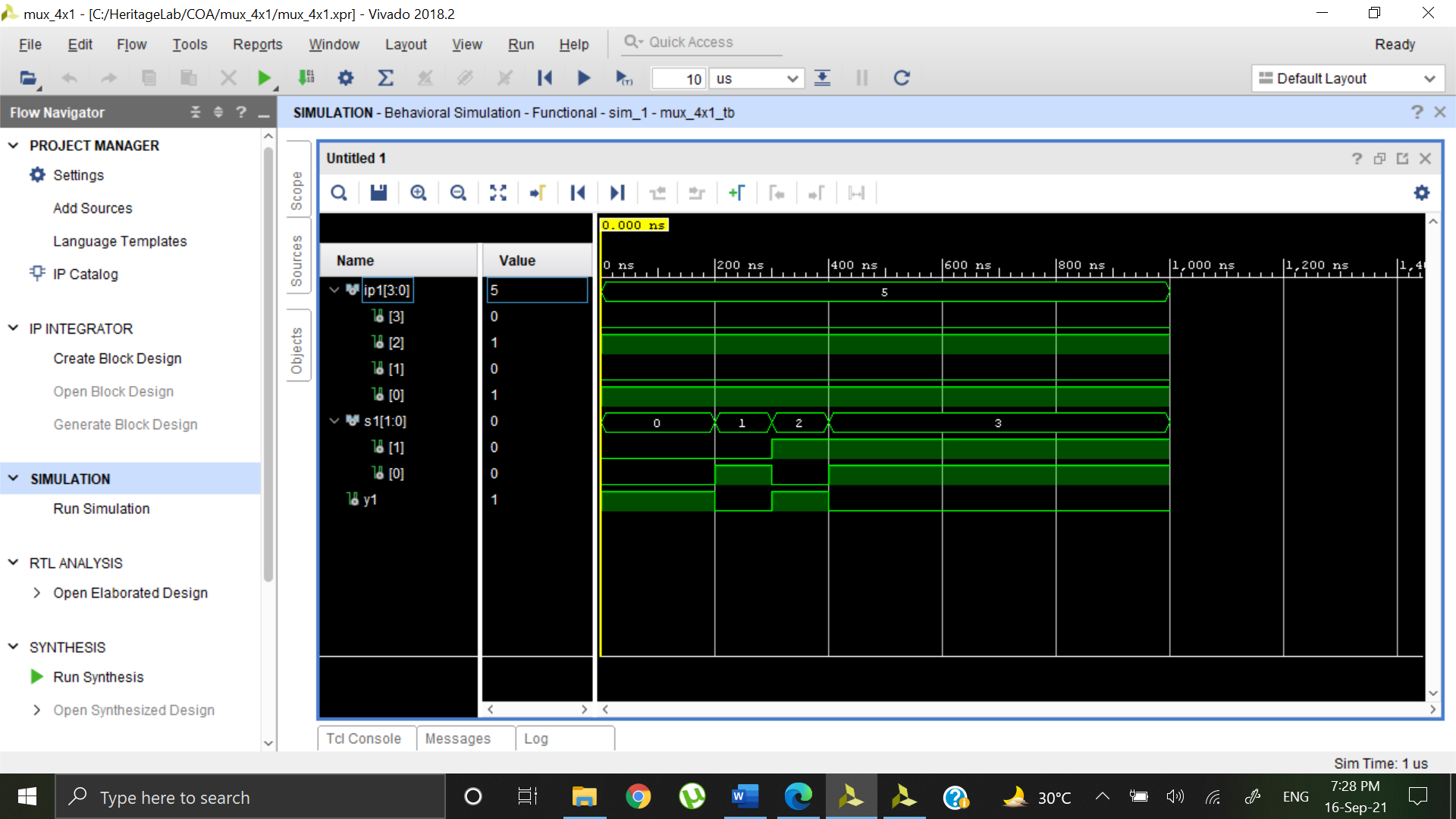
end process;

end Behavioral;

Elaborated Design:



Output Waveform:



3:8 Decoder

Dataflow:

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

entity decoder\_3x8 is

Port ( ip : in STD\_LOGIC\_VECTOR (2 downto 0);

op : out STD\_LOGIC\_VECTOR (7 downto 0));

end decoder\_3x8;

architecture Behavioral of decoder\_3x8 is

begin

op(0) <= '1' when ip="000" else '0';

op(1) <= '1' when ip="001" else '0';

op(2) <= '1' when ip="010" else '0';

op(3) <= '1' when ip="011" else '0';

op(4) <= '1' when ip="100" else '0';

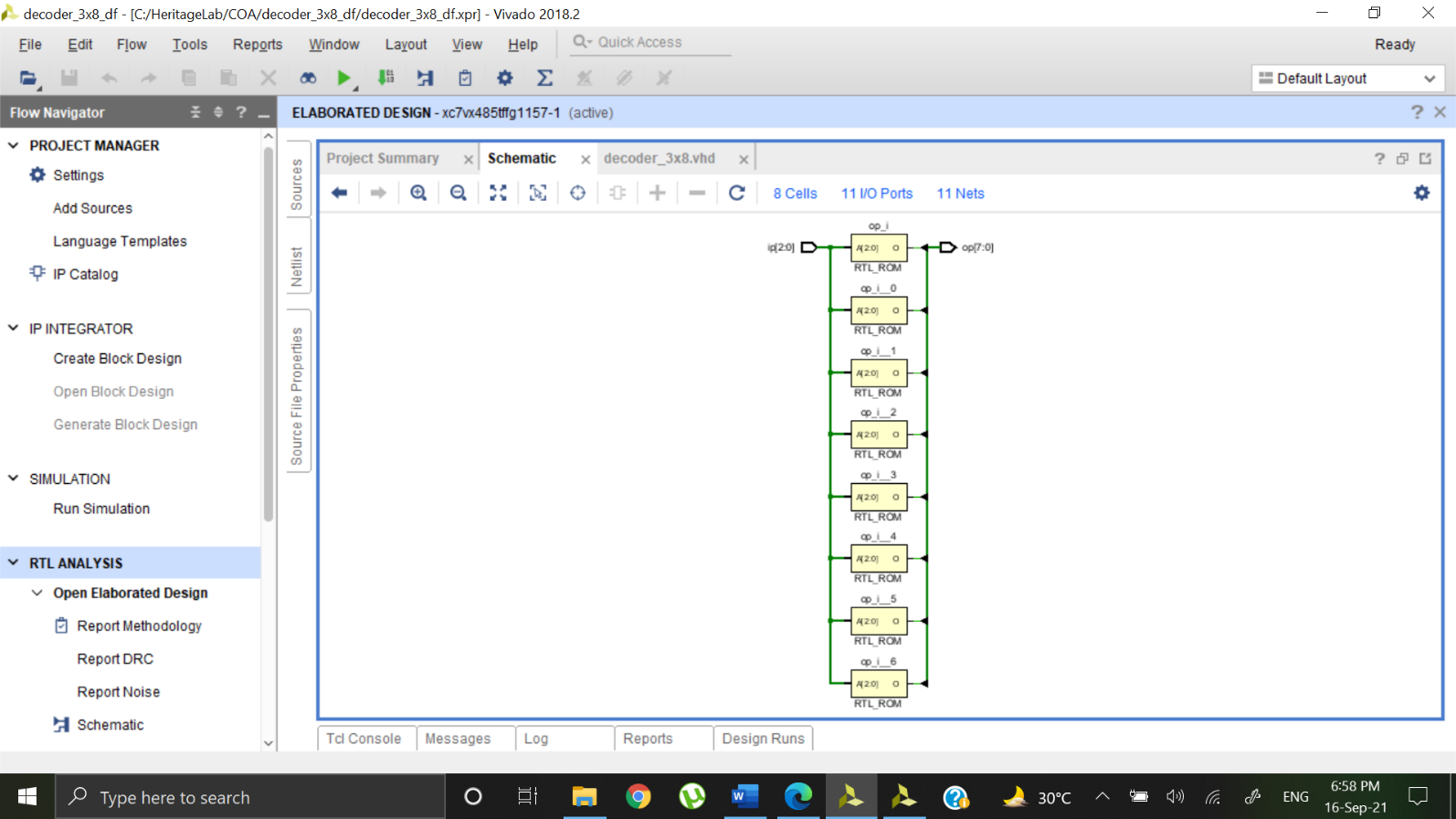
op(5) <= '1' when ip="101" else '0';

op(6) <= '1' when ip="110" else '0';

op(7) <= '1' when ip="111" else '0';

end Behavioral;

Elaborated Design:



Behavioral:

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

entity decoder is

Port ( input : in STD\_LOGIC\_VECTOR (2 downto 0);

output : out STD\_LOGIC\_VECTOR (7 downto 0));

end decoder;

architecture Behavioral of decoder is

begin

process(input)

begin

output<= "00000000";

case input is

when "000" => output(0)<= '1';

when "001" => output(1)<= '1';

when "010" => output(2)<= '1';

when "011" => output(3)<= '1';

when "100" => output(4)<= '1';

when "101" => output(5)<= '1';

when "110" => output(6)<= '1';

when "111" => output(7)<= '1';

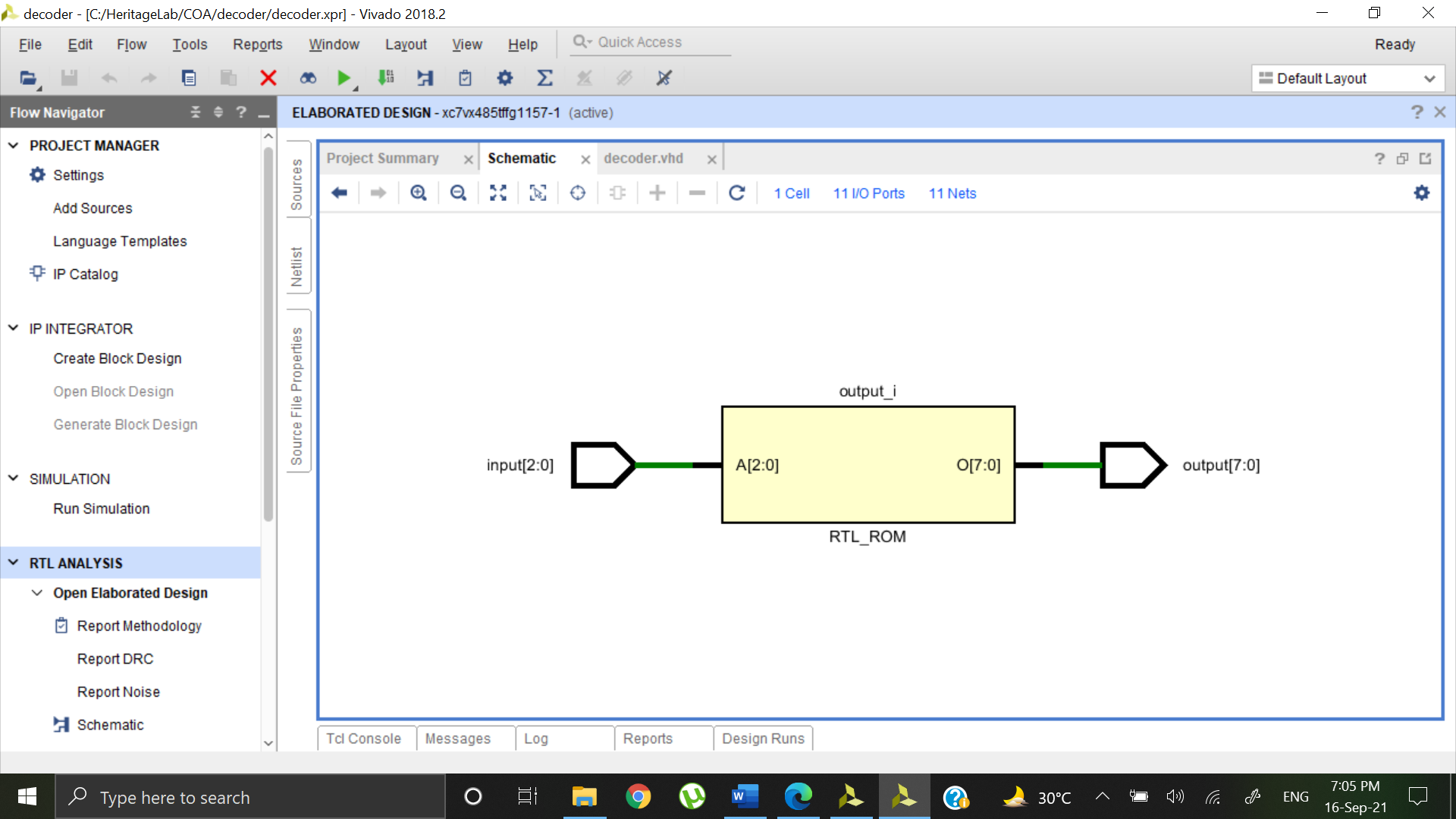
when others=> NULL;

end case;

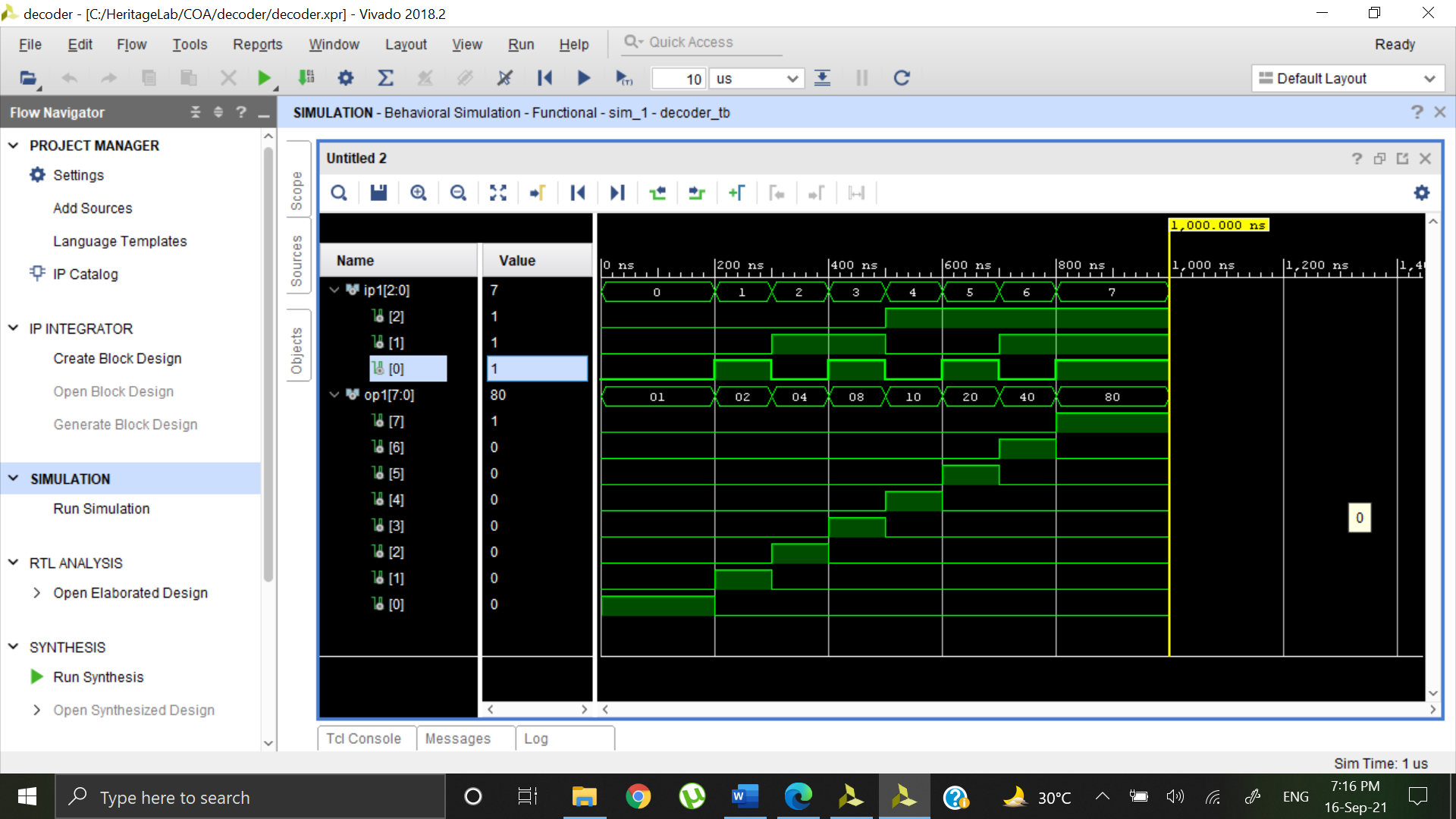
end process;

end Behavioral;

Elaborated Design:



Output Waveform:



Comparator

Dataflow:

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

entity comparator is

Port ( A : in STD\_LOGIC\_VECTOR (3 downto 0);

B : in STD\_LOGIC\_VECTOR (3 downto 0);

eq : out STD\_LOGIC;

gt : out STD\_LOGIC;

lt : out STD\_LOGIC);

end comparator;

architecture Dataflow of comparator is

begin

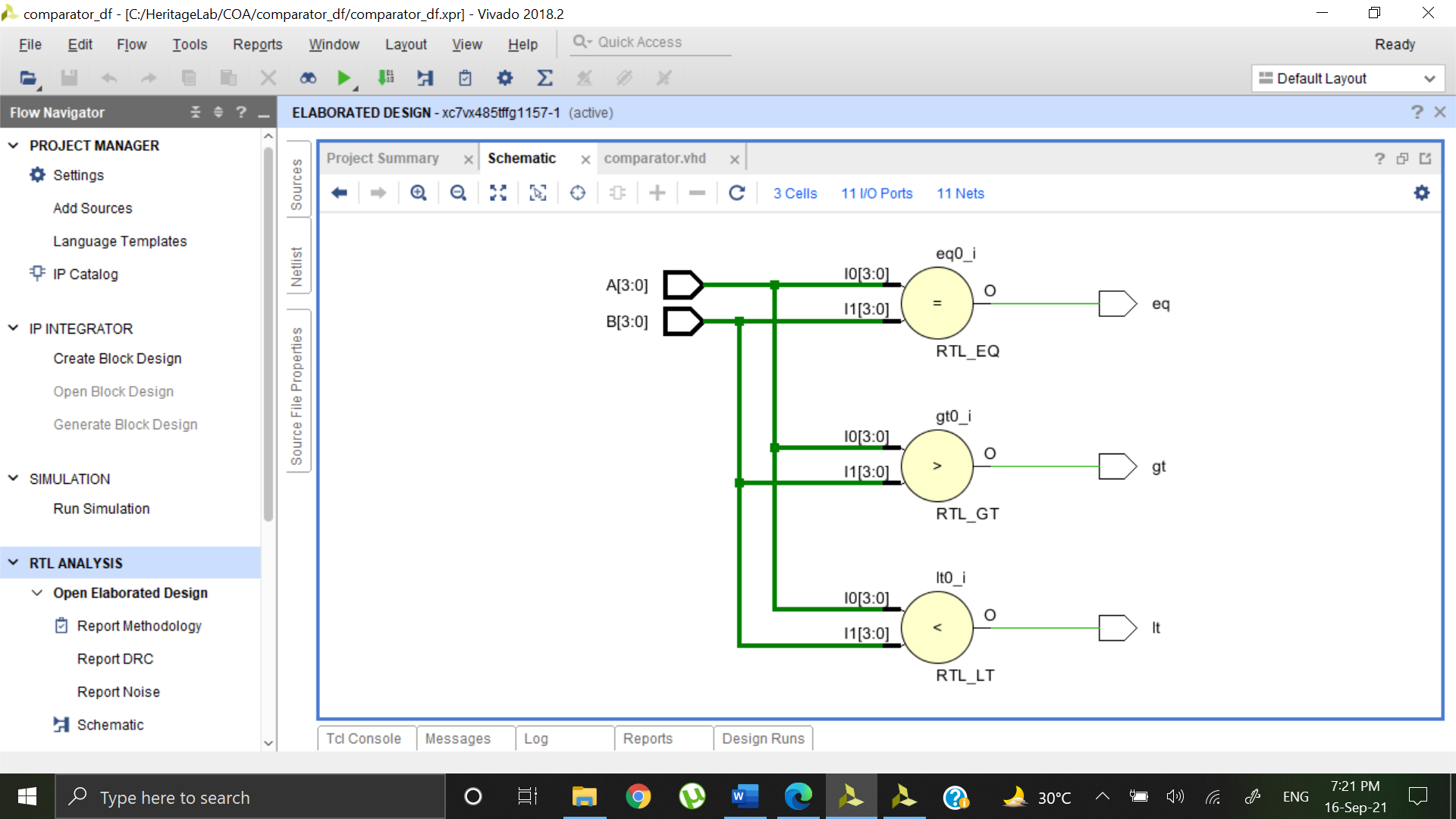
eq<='1' when A=B else '0';

gt<='1' when A>B else '0';

lt<='1' when A<B else '0';

end Dataflow;

Elaborated Design:



Output Waveform:

