ASSIGNMENT- IV

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STREAM: CSE-A

ROLL NUMBER: 1951007

SUBJECT: COMPUTER ARCHITECTURE LAB

**Question 1:**

Design ALU with 4 logical and 4 arithmetic operations

**Structural Code**

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

use IEEE.NUMERIC\_STD.ALL;

entity alu is

Port ( A : in unsigned (3 downto 0);

B : in unsigned(3 downto 0);

Ch : in STD\_LOGIC\_VECTOR (2 downto 0);

Res : out unsigned(3 downto 0));

end alu;

architecture Behavioral of alu is

begin

process(A,B,Ch)

begin

case Ch is

when "000"=>Res<=A+B;

when "001"=>Res<=A-B;

when "010"=>Res<=A+1;

when "011"=>Res<=A-1;

when "100"=>Res<=A AND B;

when "101"=>Res<=A OR B;

when "110"=>Res<=NOT A;

when "111"=>Res<=A XOR B;

when others=>NULL;

end case;

end process;

end Behavioral;

**Test Bench Code**

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

use IEEE.NUMERIC\_STD.ALL;

entity alu\_tb is

-- Port ( );

end alu\_tb;

architecture Behavioral of alu\_tb is

component alu is

Port ( A : in unsigned (3 downto 0);

B : in unsigned (3 downto 0);

Ch : in STD\_LOGIC\_VECTOR (2 downto 0);

Res : out unsigned (3 downto 0));

end component;

signal A1 : unsigned (3 downto 0) := "1000";

signal B1 : unsigned (3 downto 0) := "0010";

signal Ch1 : STD\_LOGIC\_VECTOR (2 downto 0) := "000";

signal Res1 : unsigned (3 downto 0);

begin

uut: alu port map (A=>A1, B=>B1, Ch=>Ch1, Res=>Res1);

stim\_proc: process

begin

wait for 100ns;

Ch1 <= "000";

wait for 100ns;

Ch1 <= "001";

wait for 100ns;

Ch1 <= "010";

wait for 100ns;

Ch1 <= "011";

wait for 100ns;

Ch1 <= "100";

wait for 100ns;

Ch1 <= "101";

wait for 100ns;

Ch1 <= "110";

wait for 100ns;

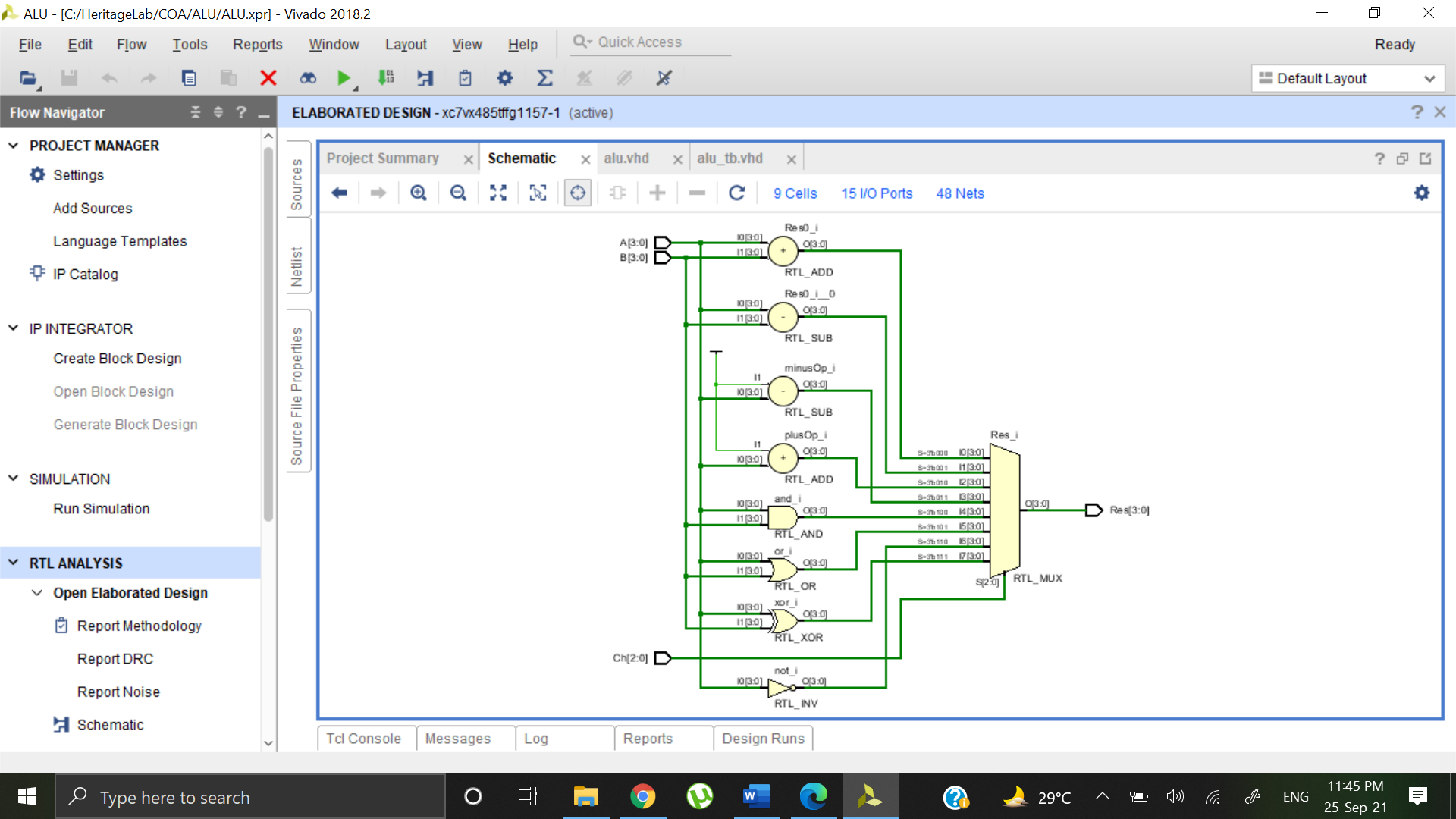
Ch1 <= "111";

wait;

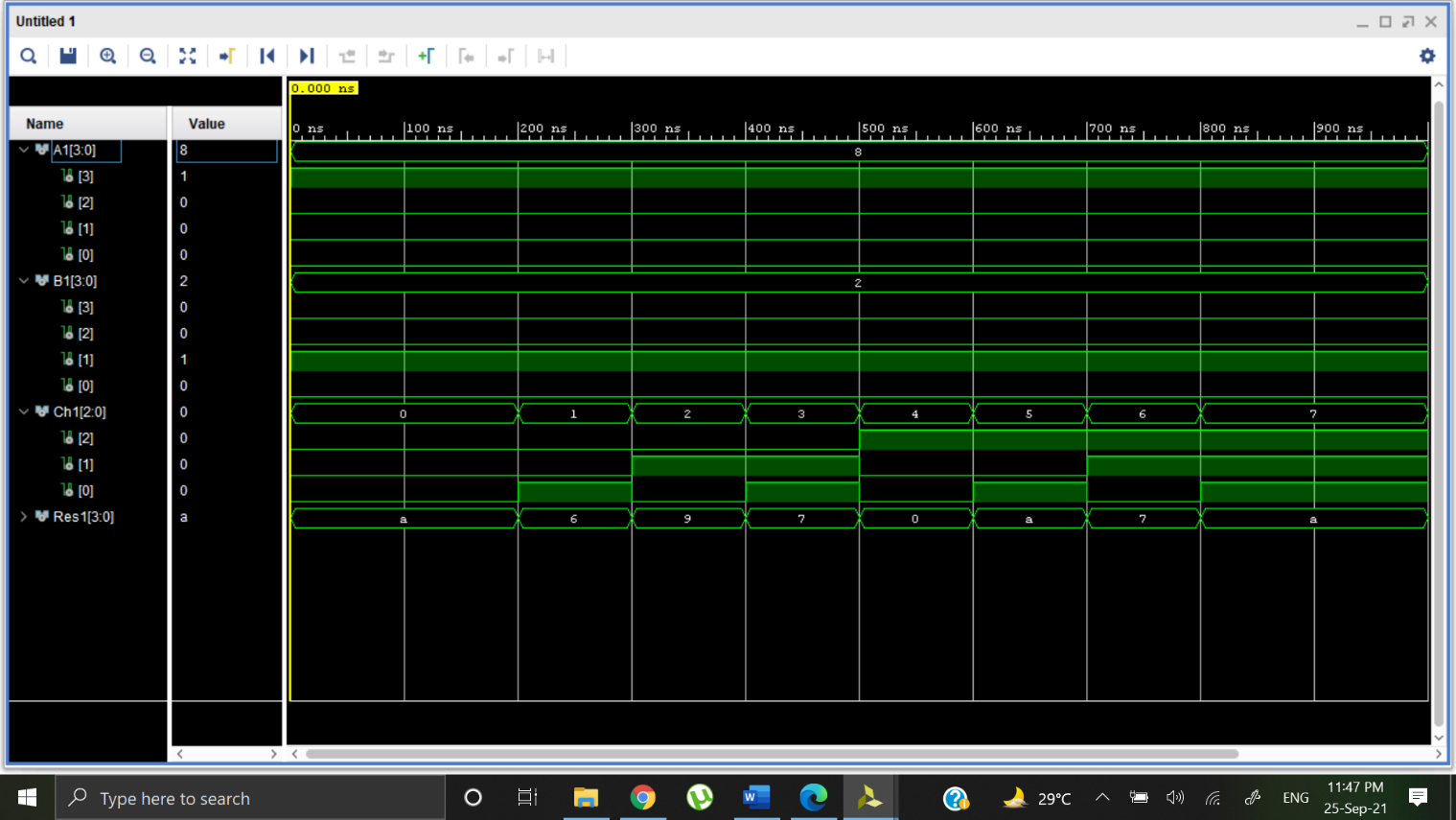
end process;

end Behavioral;

**Schematic**



**Output Waveform**



**Question 2:**

Design Structural model for 8:1 Mux using 4:1 and 2:1 Mux

**Structural Code**

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

entity mux\_8x1 is

Port ( ip : in STD\_LOGIC\_VECTOR (7 downto 0);

s : in STD\_LOGIC\_VECTOR (2 downto 0);

y : out STD\_LOGIC);

end mux\_8x1;

architecture Behavioral of mux\_8x1 is

component mux\_2x1 is

Port ( A : in STD\_LOGIC;

B : in STD\_LOGIC;

Sel : in STD\_LOGIC;

Y : out STD\_LOGIC);

end component;

component mux\_4x1 is

Port ( ip : in STD\_LOGIC\_VECTOR (3 downto 0);

s : in STD\_LOGIC\_VECTOR (1 downto 0);

y : out STD\_LOGIC);

end component;

signal Y1: STD\_LOGIC;

signal Y2: STD\_LOGIC;

begin

l1:mux\_4x1 port map(ip(7 downto 4),s(1 downto 0),Y1);

l2:mux\_4x1 port map(ip(3 downto 0),s(1 downto 0),Y2);

l3:mux\_2x1 port map(Y2,Y1,s(2),Y);

end Behavioral;

**Test Bench Code**

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

entity mux\_8x1\_tb is

-- Port ( );

end mux\_8x1\_tb;

architecture Behavioral of mux\_8x1\_tb is

component mux\_8x1 is

Port ( ip : in STD\_LOGIC\_VECTOR (7 downto 0);

s : in STD\_LOGIC\_VECTOR (2 downto 0);

y : out STD\_LOGIC);

end component;

signal ip1: STD\_LOGIC\_VECTOR (7 downto 0):="00000000";

signal sell: STD\_LOGIC\_VECTOR (2 downto 0):="000";

signal Y1: STD\_LOGIC :='0';

begin

uut: mux\_8x1 port map(ip=>ip1, s=>sell, Y=>Y1);

stim\_proc: process

begin

wait for 100ns;

ip1 <= "10010101";

sell <= "010";

wait for 100ns;

ip1 <= "10110011";

sell <= "011";

wait for 100ns;

ip1 <= "10001100";

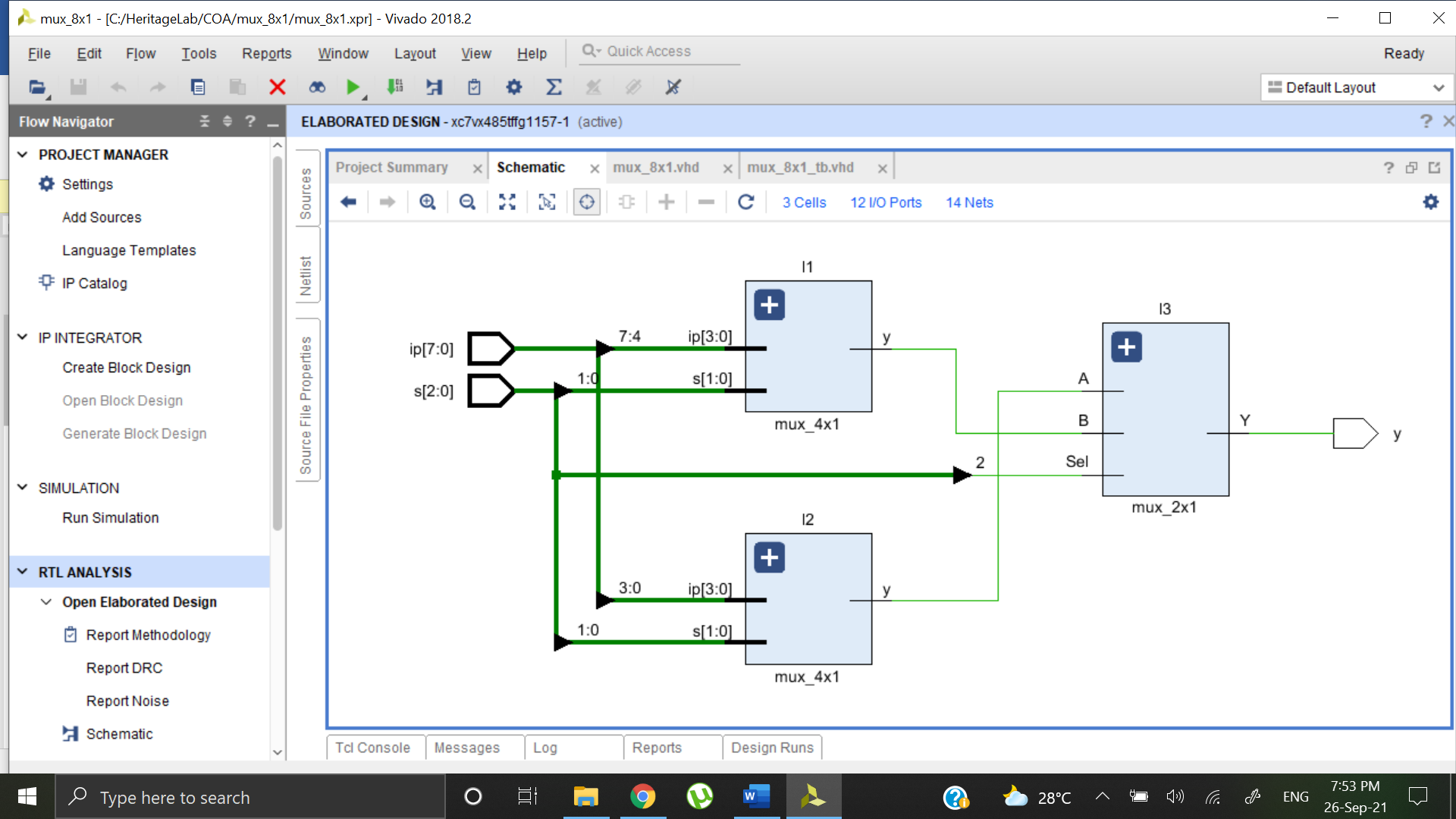
sell <= "001";

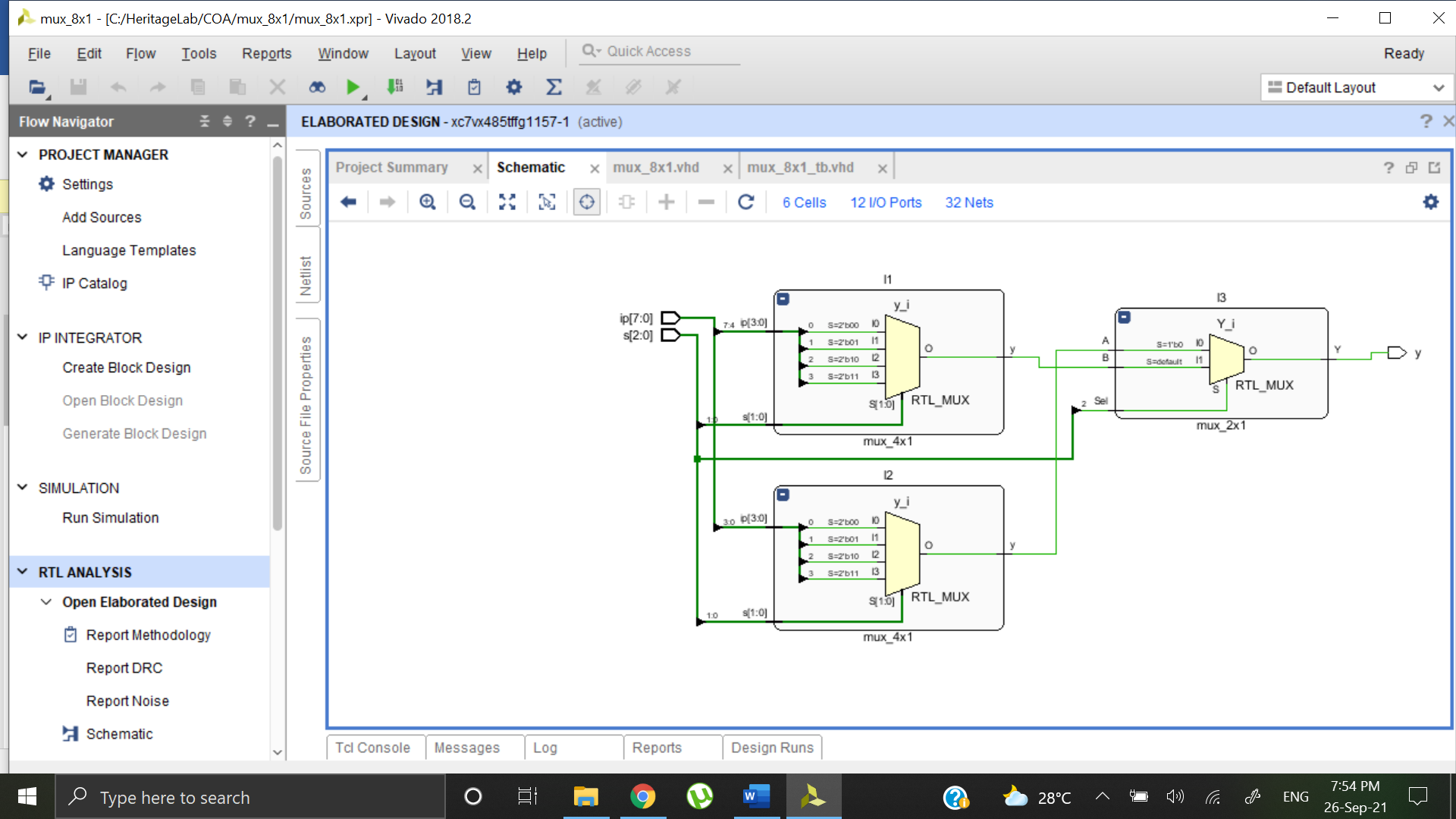
wait;

end process;

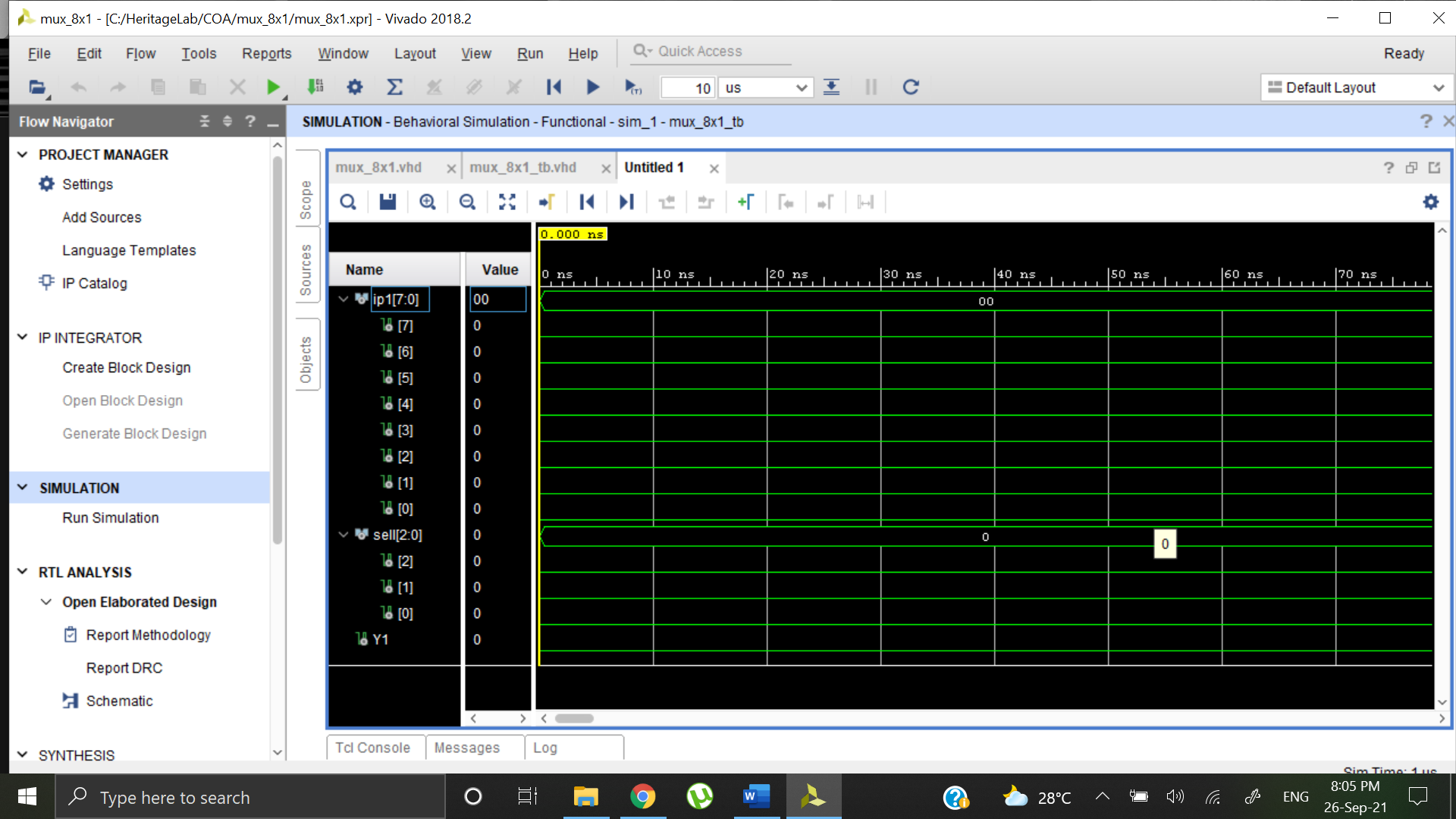
end Behavioral;

**Schematic**





**Output Waveform**



**Question 3**

Design Structural model for Full adder using half adder and or gate

**Structural Code**

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

entity fullad is

Port ( X : in STD\_LOGIC;

Y : in STD\_LOGIC;

Z : in STD\_LOGIC;

Sum : out STD\_LOGIC;

Carry : out STD\_LOGIC);

end fullad;

architecture Structural of fullad is

component halfad\_bv is

Port ( A : in STD\_LOGIC;

B : in STD\_LOGIC;

S : out STD\_LOGIC;

C : out STD\_LOGIC);

end component;

component or\_bv is

Port ( X : in STD\_LOGIC;

Y : in STD\_LOGIC;

Z : out STD\_LOGIC);

end component;

signal S1: STD\_LOGIC;

signal C1: STD\_LOGIC;

signal C2: STD\_LOGIC;

begin

l1:halfad\_bv port map(X,Y,S1,C1);

l2:halfad\_bv port map(S1,Z,Sum,C2);

l3:or\_bv port map(C1,C2,Carry);

end Structural;

**Test Bench Code**

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

entity fullad\_tb is

-- Port ( );

end fullad\_tb;

architecture Behavioral of fullad\_tb is

component fullad is

Port ( X : in STD\_LOGIC;

Y : in STD\_LOGIC;

Z : in STD\_LOGIC;

Sum : out STD\_LOGIC;

Carry : out STD\_LOGIC);

end component;

signal X1 : STD\_LOGIC := '0';

signal Y1 : STD\_LOGIC := '0';

signal Z1 : STD\_LOGIC := '0';

signal Sum1 : STD\_LOGIC;

signal Carry1 : STD\_LOGIC;

begin

uut: fullad PORT MAP(X=>X1,Y=>Y1,Z=>Z1,Sum=>Sum1,Carry=>Carry1);

stim\_proc: process

begin

wait for 100 ns;

X1<='0';

Y1<='0';

Z1<='0';

wait for 100 ns;

X1<='0';

Y1<='0';

Z1<='1';

wait for 100 ns;

X1<='0';

Y1<='1';

Z1<='0';

wait for 100 ns;

X1<='0';

Y1<='1';

Z1<='1';

wait for 100 ns;

X1<='1';

Y1<='0';

Z1<='0';

wait for 100 ns;

X1<='1';

Y1<='0';

Z1<='1';

wait for 100 ns;

X1<='1';

Y1<='1';

Z1<='0';

wait for 100 ns;

X1<='1';

Y1<='1';

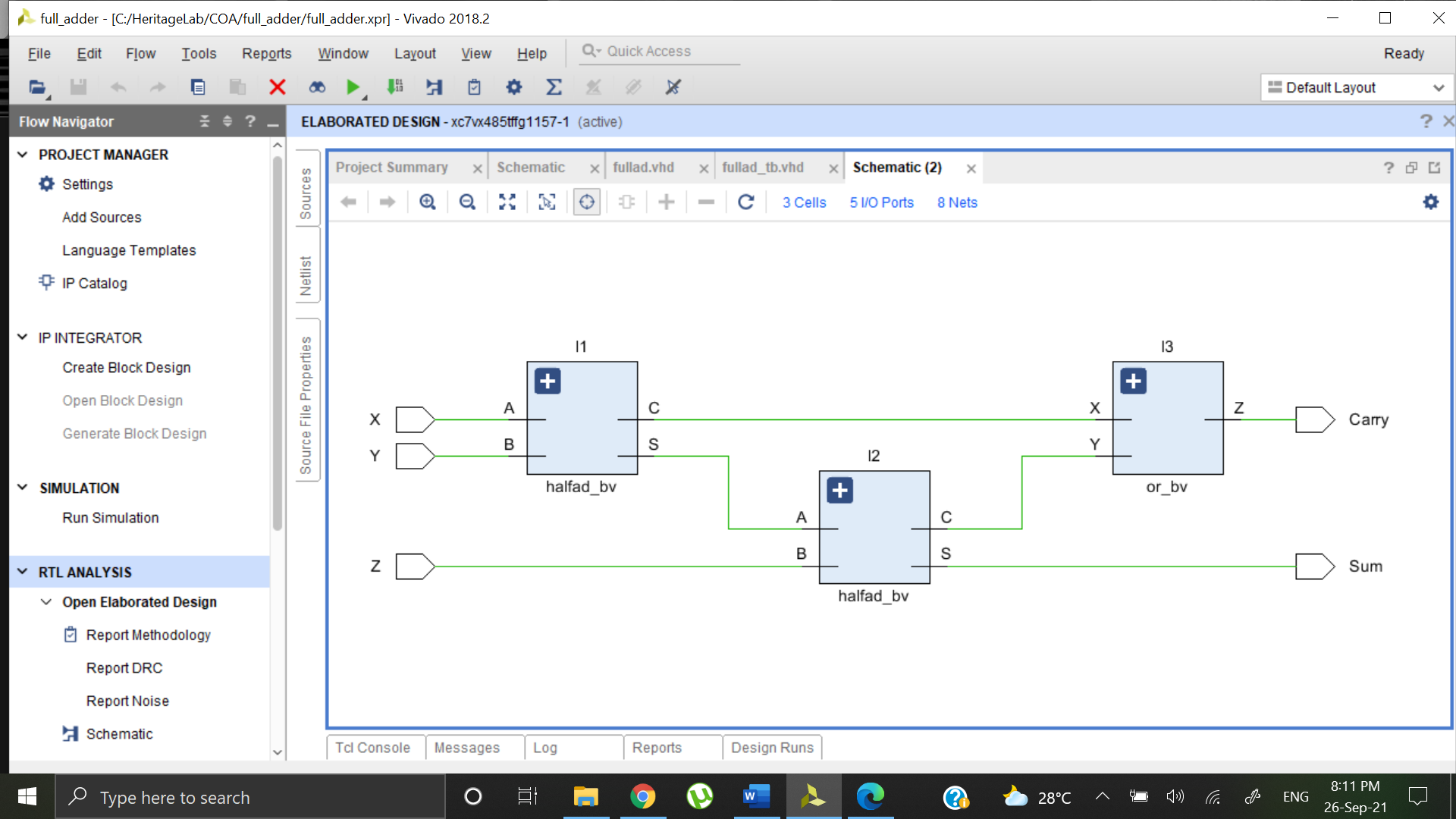
Z1<='1';

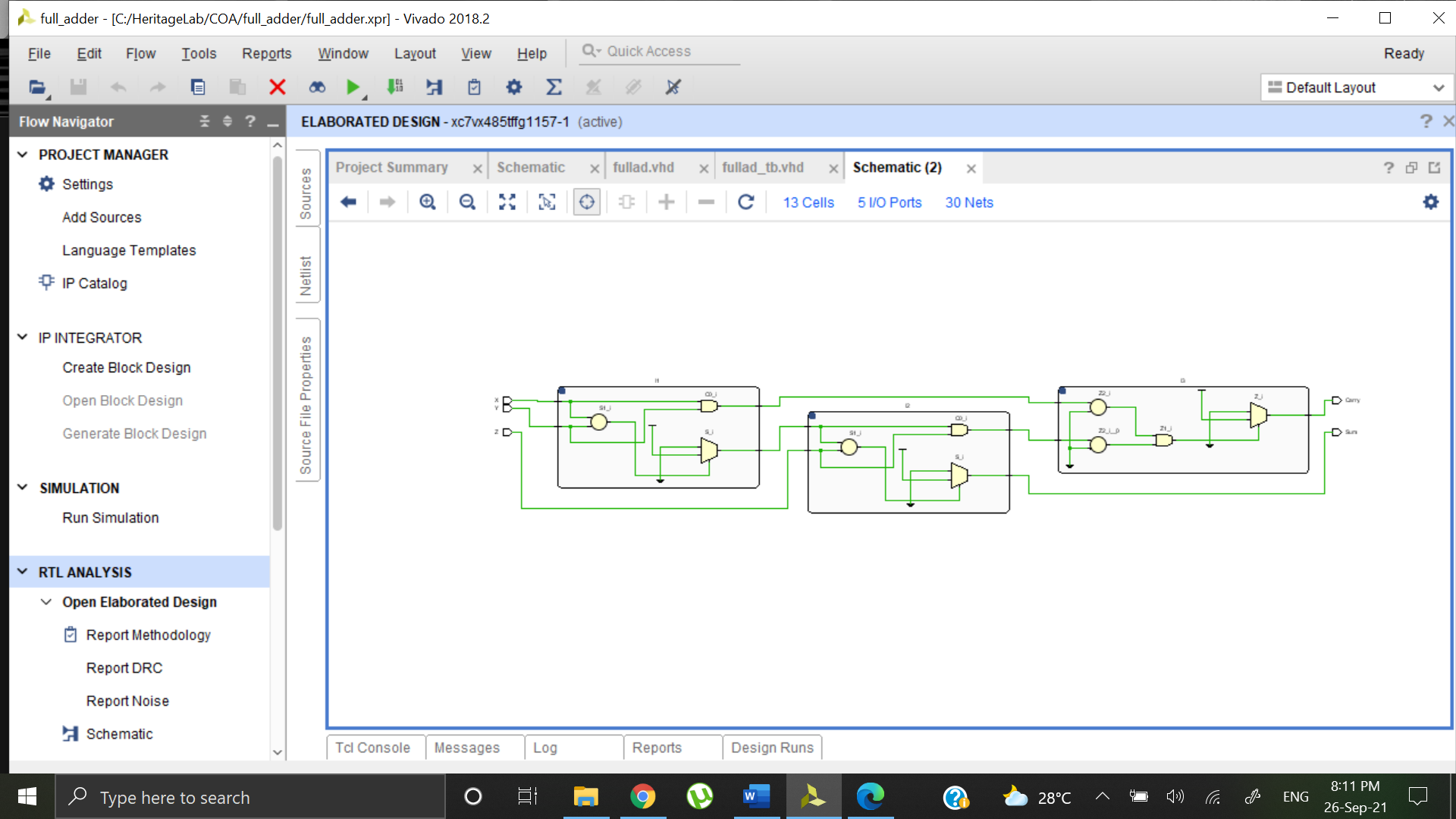
wait;

end process;

end Behavioral;

**Schematic**





**Output Waveform**

