ICS 2104: COMPUTER ORGANIZATION AND ARCHITECTURE CAT 2 – GROUP A

TIME: 1 HOUR

Answer ALL the Questions

a) Convert the following C++ code snippet into equivalent assembly instructions. Assume all variables are unsigned 32-bit integers stored in memory. [4 Marks]

Ans = Ans = (A - C) * (D + E);

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; Calculate (A - C)
mov eax, [A]          ; Load A into eax
sub eax, [C]          ; Subtract C from eax, eax = A - C
; Calculate (D + E)
mov ebx, [D]          ; Load D into ebx
add ebx, [E]          ; Add E to ebx, ebx = D + E
; Multiply (A - C) * (D + E)
mul ebx          ; Unsigned multiply eax by ebx
; Store the lower 32 bits of the result into Ans
mov [Ans], eax
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b) Name and briefly describe the components contained in the Solid-State Drives (SSDs). [5 Marks]

i. Controller: Provides SSD device level interfacing and firmware execution.
ii. Addressing: Logic that performs the selection function across the flash memory components.
iii. Data buffer/cache: High speed RAM memory components used for speed matching and to increase data throughput.
iv. Error correction: Logic for error detection and correction.
v. Flash memory components: Individual NAND flash chips.

c) A security alarm system activates an alarm under the following conditions:
The door sensor (D) is triggered (D = 1) and the system is armed (A = 1), or the window sensor (W) is triggered (W = 1) and the system is armed (A = 1).

i. Write the Boolean expression for the alarm output (Alarm). [2 Marks]

Alarm=(D·A)+(W·A)

Factor out A: Alarm=A·(D+W)

ii. Construct the truth table showing all the possible input combinations. [3 Marks]

iii. Draw the logic circuit diagram for the simplified Boolean expression using AND, and OR gates. [3 Marks]

OR gate with inputs: D, W

AND gate with inputs: output of OR gate and A

Output of AND gate is Alarm

d) Name and briefly describe the memory instructions for moving data between memory and the registers. [3 Marks]

i. I/O instructions to transfer programs and data into memory and the results of computations back out to the user.

ii. Test instructions to test the value of a data word or the status of a computation.

iii. Branch instructions to branch to a different set of instructions depending on the decision made.

e) State the two design issues that arise in implementing interrupt driven Input /Output. [2 Marks]

i. First, because there will almost invariably be multiple I/O modules, how does the processor determine which device issued the interrupt?

ii. Second, if multiple interrupts have occurred, how does the processor decide which one to process?

f) The semiconductor memory cell consists of three functional terminals capable of carrying an electrical signal. Name and briefly describe them. [3 Marks]

i. The select terminal: Selects a memory cell for a read or write operation.

ii. The control terminal indicates read or write.

iii. For writing, the other terminal provides an electrical signal that sets the state of the cell to 1 or 0. For reading, that terminal is used for output of the cell's state.

g) Explain briefly how register allocation via graph colouring helps optimize register usage. [2 Marks]

Register allocation via graph coloring assigns variables to registers such that no two interfering variables share the same register, minimizing the number of registers used and reducing memory access

h) The choice of the mapping function dictates how the cache is organized. Names and briefly describe the three techniques used. [3 Marks]

i. Direct Mapping - The technique maps each block of main memory into only one possible cache line. The mapping function is easily implemented using the main memory address.

ii. Associative mapping overcomes the disadvantage of direct mapping by permitting each main memory block to be loaded into any line of the cache. The cache control logic interprets a memory address as a Tag and a Word field.

iii. Set-associative mapping is a compromise that exhibits the strengths of both the direct and associative approaches while reducing their disadvantages. The cache consists of number sets, each of which consists of several lines.