ICS 2104: COMPUTER ORGANIZATION AND ARCHITECTURE CAT I – GROUP C

TIME: 1 HOUR

Answer ALL the Questions

a) Briefly describe the functional elements of a single core. [3 Marks]

i. Instruction logic: This includes the tasks involved in fetching instructions and decoding each instruction to determine the instruction operation and the memory locations of any operands.

ii. Arithmetic and logic unit (ALU): Performs the operation specified by an instruction.

iii. Load/store logic: Manages the transfer of data to and from main memory via cache.

b) Describe the states of a basic instruction cycle. [7 Marks]

i. Instruction address calculation (IAC): Determines the address of the next instruction to be executed.

ii. Instruction fetch (IF): Read instruction from its memory location into the processor.

iii. Instruction operation decoding (IOD): Analyze instruction to determine type of operation to be performed and operand(s) to be used.

iv. Operand address calculation (OAC): If the operation involves reference to an operand in memory or available via I/O, then determine the address of the operand.

v. Operand fetch (OF): Fetch the operand from memory or read it in from I/O.

vi. Data operation (DO): Perform the operation indicated in the instruction.

vii. Operand store (OS): Write the result into memory or out to I/O.

c) Convert the hexadecimal number 6ED.B4 into a decimal number. [4 Marks]

Step 1: Convert the integer part "6ED" (hex) to decimal

Step 2: Convert the fractional part "B4" (hex) to decimal

Final decimal value: 1773 + 0.703125 = 1773.703125

d) Convert the Convert the octal number 4715_8 into a hexadecimal number. [4 Marks]

Step 1: Convert Octal (4715) to Decimal

Step 2: Convert Decimal (2509) to Hexadecimal

Write the remainders in reverse order: $9CD_{16}$

Final Answer: $4715_8 = 9CD_{16}$

e) Briefly describe the three approaches to achieving increased processor speed. [3 Marks]

i. Increase the hardware speed of the processor. This increase is fundamentally due to shrinking the size of the logic gates on the processor chip, so that more gates can be packed together more tightly and to increasing the clock rate. An increase in clock rate means that individual operations are executed more rapidly.

ii. Increase the size and speed of caches that are interposed between the processor and main memory. By dedicating a portion of the processor chip itself to the cache, cache access times drop significantly.

iii. Make changes to the processor organization and architecture that increase the effective speed of instruction execution. Typically, this involves using parallelism in one form or another.

f) Illustrate the profound consequences of Moore's law on transistors. [5 Marks]

i. The cost of a chip has remained virtually unchanged during this period of rapid growth in density. This means that the cost of computer logic and memory circuitry has fallen at a dramatic rate.

ii. Because logic and memory elements are placed closer together on more densely packed chips, the electrical path length is shortened, increasing operating speed.

iii. The computer becomes smaller, making it more convenient to place in a variety of environments.

iv. There is a reduction in power requirements.

v. The interconnections on the integrated circuit are much more reliable than solder connections. With more circuitry on each chip, there are fewer inter-chip connections.

g) Briefly discuss the QuickPath Interconnect (QPI) protocol layers. [4 Marks]

i. Physical: Consists of the actual wires carrying the signals, as well as circuitry and logic to support ancillary features required in the transmission and receipt of the 1s

and 0s. The unit of transfer at the Physical layer is 20 bits, which is called a Phit (physical unit).

ii. Link: Responsible for reliable transmission and flow control. The Link layer's unit of transfer is an 80-bit Flit (flow control unit).

iii. Routing: Provides the framework for directing packets through the fabric.

iv. Protocol: The high-level set of rules for exchanging packets of data between devices. A packet is comprised of an integral number of Flits.