ICS 2104: COMPUTER ORGANIZATION AND ARCHITECTURE CAT I – GROUP B

TIME: 1 HOUR

Answer ALL the Questions

a) Convert the decimal number 645.786 into a binary number. [6 Marks]

Step 1: Convert Integer Part (645) to Binary

645 (decimal) = 1010000101 (binary)

Step 2: Convert Fractional Part (0.786) to Binary

b) Distinguish between structure and function as used to describe a computer system. [2 Marks]

Structure is the way in which the components are interrelated, and function is the operation of each individual component as part of the structure.

c) Discuss the significant characteristics of QuickPath Interconnect and other point-to-point interconnect schemes. [6 Marks]

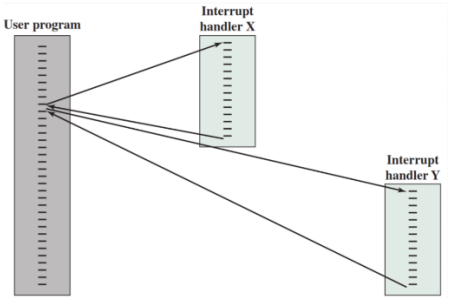
i. Multiple direct connections: Multiple components within the system enjoy direct pairwise connections to other components. This eliminates the need for arbitration found in shared transmission systems.

ii. Layered protocol architecture: As found in network environments, such as TCP/IP-based data networks, these processor-level interconnects use a layered protocol architecture, rather than the simple use of control signals found in shared bus arrangements.

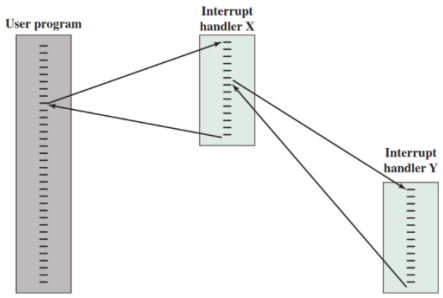
iii. Packetized data transfer: Data are not sent as a raw bit stream. Rather, data are sent as a sequence of packets, each of which includes control headers and error control codes.

d) Using relevant diagrams, list and explain the two approaches to dealing with multiple interrupts. [6 Marks]

i. To disable interrupts while an interrupt is being processed. A disabled interrupt means that the processor can and will ignore that interrupt request signal. If an interrupt occurs during this time, it generally remains pending and will be checked by the processor after the processor has enabled interrupts. Thus, when a user program is executing, and an interrupt occurs, interrupts are disabled immediately. After the interrupt handler routine completes, interrupts are enabled before resuming the user program, and the processor checks to see if additional interrupts have occurred.



ii. Define priorities for interrupts and to allow an interrupt of higher priority to cause a lower-priority interrupt handler to be itself interrupted.



e) Briefly describe the major structural components of a CPU. [4 Marks]

i. Control unit: Controls the operation of the CPU and hence the computer.

ii. Arithmetic and logic unit (ALU): Performs the computer's data processing functions.

iii. Registers: Provides storage internal to the CPU.

iv. CPU interconnection: Some mechanism that provides for communication among the control unit, ALU, and registers.

f) Designers constantly strive to balance the throughput, and processing demands of the processor components, main memory, I/O devices, and the interconnection structures. State

the two constantly evolving factors that compel designers to rethink their strategies in balancing designing for performance. [2 Marks]

i. The rate at which performance is changing in the various technology areas (processor, buses, memory, peripherals) differs greatly from one type of element to another.

ii. New applications and new peripheral devices constantly change the nature of the demand on the system in terms of typical instruction profile and the data access patterns.

g) Briefly discuss the four address spaces supported by the PCIe Transaction Layer. [4 Marks]

i. Memory: The memory space includes system main memory. It also includes PCIe I/O devices. Certain ranges of memory addresses map into I/O devices.

ii. I/O: This address space is used for legacy PCI devices, with reserved memory address ranges used to address legacy I/O devices.

iii. Configuration: This address space enables the TL to read/write configuration registers associated with I/O devices.

iv. Message: This address space is for control signals related to interrupts, error handling, and power management.