ICS 2104: COMPUTER ORGANIZATION AND ARCHITECTURE CAT I – GROUP A

TIME: 1 HOUR

Answer ALL the Questions

a) Convert the decimal number 5467 into a hexadecimal number. [3 Marks]

5467÷16=341 remainder 11 → 11 in hex is B

341÷16=21 remainder 5

21÷16=1 remainder 5

1÷16=0 remainder 1

Final answer: $5467_{10} = 155B_{16}$

b) Convert the binary number 1010000101 into a decimal number. [3 Marks]

c) Distinguish between computer organization and computer architecture. [2 Marks]

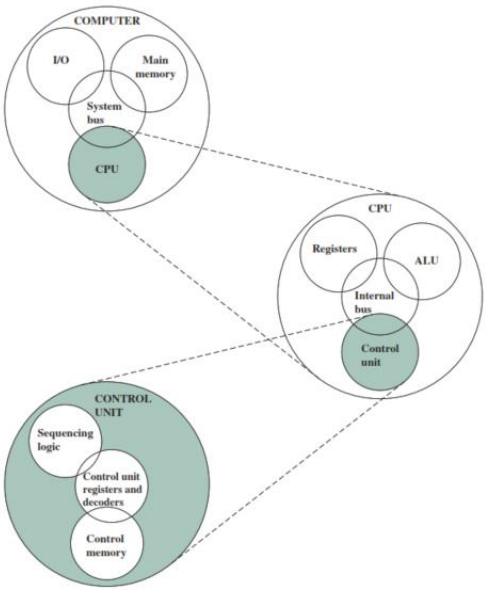
Computer architecture refers to those attributes of a system visible to a programmer or, put another way, those attributes that have a direct impact on the logical execution of a program.

Computer organization refers to the operational units and their interconnections that realize the architectural specifications.

d) Explain the three functional groups defined in system bus. [3 Marks]

The data lines provide a path for moving data among system modules. The address lines are used to designate the source or destination of the data on the data bus. The control lines are used to control the access to and the use of the data and address lines.

e) Using a diagram to show the top-level structure of a computer, briefly describe the main structural components of a computer. [5 Marks]



i. Central processing unit (CPU): Controls the operation of the computer and performs its data processing functions; often simply referred to as processor.

ii. Main memory: Stores data.

iii. I/O: Moves data between the computer and its external environment.

iv. System interconnection: Some mechanism that provides for communication among CPU, main memory, and I/O.

f) Differentiate base metric, peak metric, speed metric, and rate metric. [4 Marks]

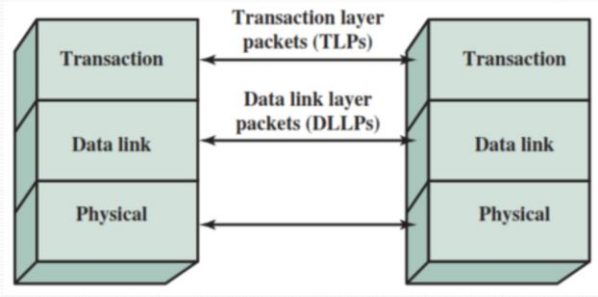
Base metric: These are required for all reported results and have strict guidelines for compilation. In essence, the standard compiler with default settings should be used on each system under test to achieve comparable results.

Peak metric: This enables users to attempt to optimize system performance by optimizing the compiler output. For example, different compiler options may be used on each benchmark, and feedback-directed optimization is allowed.

Speed metric: This is simply a measurement of the time it takes to execute a compiled benchmark. The speed metric is used for comparing the ability of a computer to complete single tasks.

Rate metric: This is a measurement of how many tasks a computer can accomplish in a certain amount of time; this is called a throughput, capacity, or rate measure. The rate metric allows the system under test to execute simultaneous tasks to take advantage of multiple processors.

g) Accompanied by a diagram representation, discuss the PCIe protocol layers. [4 Marks]



i. Physical: Consists of the actual wires carrying the signals, as well as circuitry and logic to support ancillary features required in the transmission and receipt of the 1s and 0s.

ii. Data link: Is responsible for reliable transmission and flow control. Data packets generated and consumed by the DLL are called Data Link Layer Packets (DLLPs).

iii. Transaction: Generates and consumes data packets used to implement load/store data transfer mechanisms and manages the flow control of those packets between the two components on a link.

h) Using the provided diagram illustrating a partial program execution with memory and register contents in hexadecimal, explain the fetch and execute cycle as demonstrated. Describe how the processor retrieves, decodes, and executes instructions based on the information shown. [6 Marks]

i. The PC contains 300, the address of the first instruction. This instruction (the value 1940 in hexadecimal) is loaded into the instruction register IR, and the PC is incremented. Note that this process involves the use of a memory address register and a memory buffer register. For simplicity, these intermediate registers are ignored.

ii. The first 4 bits (first hexadecimal digit) in the IR indicate that the AC is to be loaded. The remaining 12 bits (three hexadecimal digits) specify the address (940) from which data are to be loaded.

iii. The next instruction (5941) is fetched from location 301, and the PC is incremented.

iv. The old contents of the AC and the contents of location 941 are added, and the result is stored in the AC.

v. The next instruction (2941) is fetched from location 302, and the PC is incremented.

vi. The contents of the AC are stored in location 941.