Dual Channel 24-Bit Analog-to-Digital Converter (ADC) with PGA

DESCRIPTION

Based on Avia Semiconductor's patented technology, HX717 is a precision 24-bit analog-to-digital converter (ADC) with very low noise input PGA, designed for weigh scales and industrial control measurement applications to interface directly with small output signal sensors. HX717 is almost pin compatible to HX711, with on chip regulator.

The input multiplexer selects either Channel A or B differential input to the low-noise programmable gain amplifier (PGA). Channel A can be programmed with a gain of 128, or 64, corresponding to a full-scale differential input voltage of ±20mV, or ±40mV respectively, when a 5V supply is connected to VREF pin. Channel B has a selectable gain of 64 or 8. On-chip power supply regulator eliminates the need for an external supply regulator to provide analog power for the ADC and the sensor.

There is no programming needed for the internal registers. All controls to the HX717 are through the pins.

FEATURES

- **Two selectable differential input channels**
- **On-chip active low noise PGA with selectable gain of 8, 64 and 128**
- **On-chip power supply regulator for load-cell**
- **On-chip oscillator requiring no external component with optional external clock input**
- **On-chip power-on-reset**
- **Simple digital control and serial interface: pin-driven controls, no programming needed**
- **Selectable 10, 20, 80 or 320SPS output data rate**
- **Simultaneous 50 and 60Hz supply rejection**
- **Current consumption including on-chip analog power supply regulator: normal operation < 1.7mA, power down < 1uA**
- **Operation supply voltage range: 2.7 ~ 5.5V**
- **Operation temperature range: -40 ~ +85℃**
- **16 pin SOP-16 package**

APPLICATIONS

- **Weigh Scales**
- **Industrial Process Control and Measurements**

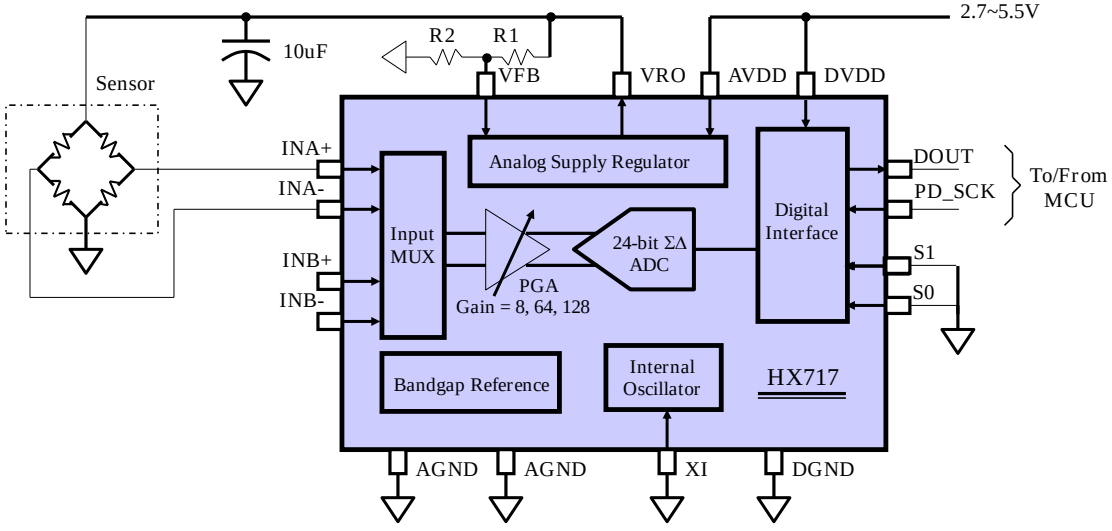
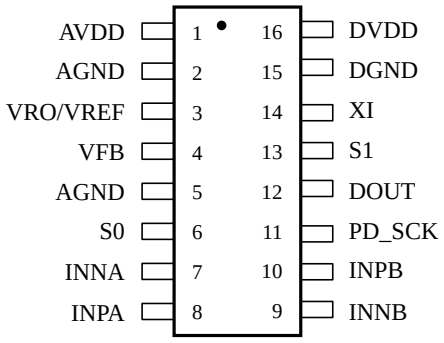


Fig. 1 HX717 Typical application block diagram

Pin Description



HX717

SOP-16L Package

Pin #	Name	Function	Description
1	AVDD	Power	Analog supply: 2.7 ~ 5.5V (AVDD must be ≥DVDD)
2	AGND	Ground	Analog ground
3	VRO/VREF	Analog I/O	Regulator output/AD conversion reference input 1.8 ~ 5.5V
4	VFB	Analog Input	Regulator control input
5	AGND	Ground	Analog ground
6	S0	Digital Input	Output data rate control
7	INA-	Analog Input	Channel A negative input
8	INA+	Analog Input	Channel A positive input
9	INB-	Analog Input	Channel B negative input
10	INB+	Analog Input	Channel B positive input
11	PD_SCK	Digital Input	Power down control (high active) and serial clock input
12	DOUT	Digital Output	Serial data output
13	S1	Digital Input	Output data rate control
14	XI	Digital Input	External clock input, 0: use on-chip oscillator
15	DGND	Ground	Digital ground
16	DVDD	Power	Digital supply: 2.7 ~ 5.5V (DVDD must be ≤AVDD)

Table 1 Pin Description

KEY ELECTRICAL CHARACTERISTICS

(AVDD=DVDD=VREF=5.0V, Gain=128, Rate=10Hz, unless specifically specified)

Parameters	Note	Min	Typical	Max	Unit
Differential input full scale range （FSR）	V(INP) - V(INN)		±0.5*(VREF/GAIN)		V
Input common-mode range: (V(INP)+V(INN))/2-AGND	PGA=8	0		AVDD	V
	PGA=128, 64	0.9		AVDD-1.5	
VREF input voltage range	VREF = RP - RN	1.8		AVDD	V
Noise-Free Bits(1)	f_o = 10Hz， VREF = 5.0V		18.2		Bits
	f_o = 20Hz， VREF = 5.0V		17.7		Bits
	f_o = 80Hz， VREF = 5.0V		16.7		Bits
	f_o = 320Hz， VREF = 5.0V		15.8		Bits
A/D output data rate（f_o）			10/20/80/320		Hz
A/D output number of bits	No missing code		24		Bits
Output data format	2’complement	800000		7FFFFF	HEX
Output data settling time(2)			$4/f_o$		mS
Integral none linearity（INL）			±0.001		%of FS
Input offset			0.01		mV
Equivalent input referred noise	At 0.1Hz		14		nV/√Hz
Temperature Drift	Offset drift		±15		nV/℃
	Gain drift		±3		ppm/℃
Power supply rejection ratio			100		dB
Common mode rejection ratio	At DC， VIN=10mV		100		dB
Supply voltage		2.7	5.0	5.5	V
Supply current	In operation,VDD=5V		1.6		mA
	Power down		1		uA

（1）Noise-Free Bits = ln(VREF/GAIN/Peak-to-Peak Noise)/ln(2).

（2）Settling time refers to the time from power up, reset, input channel change and gain change to valid stable output data.

Table 2 Key Electrical Characteristics

Analog Inputs

Channel A differential input is designed to interface directly with a bridge sensor's differential output. It can be programmed with a gain of 128 or 64. The large gains are needed to accommodate the small output signal from the sensor. When 5V supply is used directly at the VREF pin, these gains correspond to a full-scale differential input voltage of ±20mV or ±40mV respectively.

Channel B differential input has a gain of 64 or 8, corresponding to a full scale input voltage range of ±40mV or ±320mV respectively, when 5V supply is used at the VREF pin. When Channel B gain is set at 8, INNB can be connected to GND directly, which is useful for single-ended signal measurements using INPB as single-ended input signal.

A/D Conversion Reference Options

In HX717, the A/D conversion reference voltage VREF is internally connected to VRO pin.

When using internal analog supply regulator for the loadcell, the output voltage can be calculated as: VRO=1.11*(R1+R2)/R2 (Fig.1). VRO should be more than 200mV below AVDD.

When VRO pin is directly connected to AVDD pin, internal analog regulator is not used. The VFB pin should be connected to AVDD as well. The regulator is automatically powered off.

Clock Source Options

By connecting pin XI to Ground, the on-chip oscillator is activated.

If accurate output data rate is needed, external reference clock can be used. An external clock can be connected to XI pin, through a 20pF ac coupled capacitor. This external clock is not required to be a square wave. It can come directly from the crystal output pin of the MCU chip, with amplitude as low as 150mV.

When using external clock, output data rate is directly proportional to the clock frequency. Using an 11.0592MHz input clock produces the output data rate as shown in Table 3. The external clock frequency should not be more than 15MHz.

When using an external clock, the internal oscillator is automatically powered down.

Output Data Rate and Format

When using the on-chip oscillator, output data rate is typically 10, 20, 80 or 320SPS, see Table 3.

S1	S0	Output data rate
0	0	10 Hz
0	1	20 Hz
1	0	80 Hz
1	1	320 Hz

Table 3 Output Data Rate Selection

The output 24 bits of data is in 2's complement format. When input differential signal goes out of the 24-bit range, the output data will be saturated at 800000h (MIN) or 7FFFFFh (MAX), until the input signal comes back to the input range.

Serial Interface

Pin PD_SCK and DOUT are used for data retrieval, input selection, gain selection and power down controls.

When output data is not ready for retrieval, digital output pin DOUT is high. Serial clock input PD_SCK should be low. When DOUT goes to low, it indicates data is ready for retrieval. By applying positive clock pulses at the PD_SCK pin, data is shifted out from the DOUT output pin. Each PD_SCK pulse shifts out one bit, starting with the MSB bit first, until all 24 bits are shifted out. The 25th pulse at PD_SCK input will pull DOUT pin back to high (Fig.2).

Input channel and gain selection are controlled by the numbers of the input PD_SCK pulses.

PD_SCK Pulses	Input channel	Gain
25	A	128
26	B	64
27	A	64
28	B	8

Table 4 Input Channel and Gain Selection

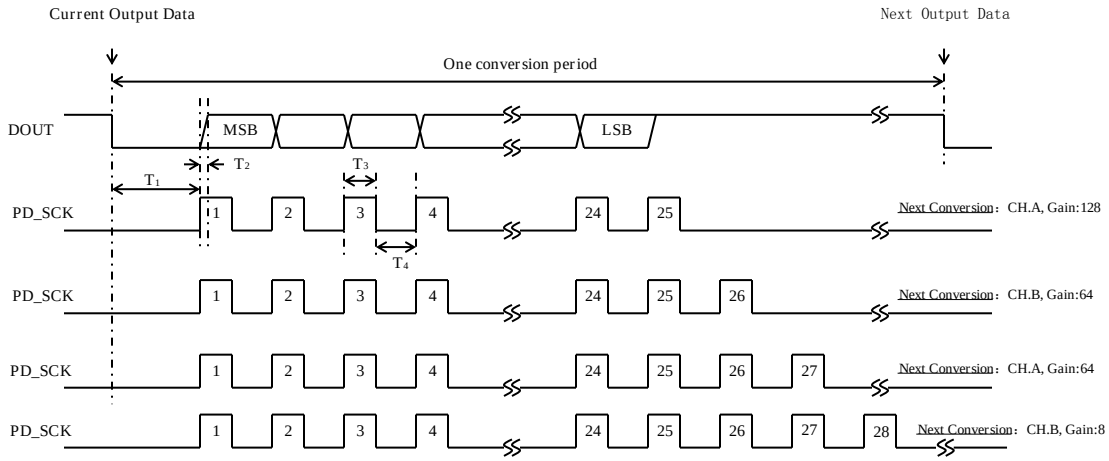


Fig.2 Data output, input and gain selection timing and control

Symbol	Note	MIN	TYP	MAX	Unit
T_1	DOUT falling edge to PD_SCK rising edge	0.1			μs
T_2	PD_SCK rising edge to DOUT data ready			0.1	μs
T_3	PD_SCK high time	0.2	1	50	μs
T_4	PD_SCK low time	0.2	1		μs

Reset and Power-Down Modes

Pin PD_SCK input is used to power down the HX717. When PD_SCK Input is low, chip is in normal working mode.

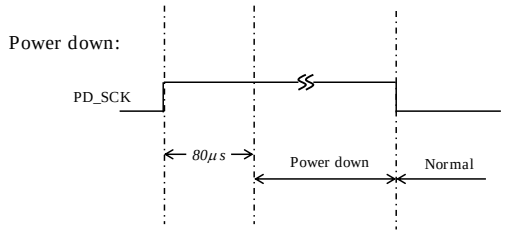


Fig.3 Power down control

When PD_SCK pin changes from low to high and stays high for longer than 80μs, HX717 enters power down mode (Fig.3).

There are 3 power down modes. When PD_SCK input pulses is between 25~28, and stays high after the 25~28th clock pulse rising edge for more than 80uS, only A/D converter is powered down. Current consumption will be less than 360uA.

If PD_SCK input pulses is 29, and stays high after the 29th clock pulse rising edge for more than 80uS, A/D converter and analog regulator are powered down. Current consumption will be less than 280uA.

If PD_SCK input pulses is 30 and stays high after the 30th clock pulse rising edge for more than 80uS, all will be powered down. Current consumption will be less than 1uA.

When PD_SCK returns to low, chip will return back to the setup conditions same as before power down and enter normal operation mode.

If PD_SCK pulse number is changed during the current conversion period, power down should be executed after current conversion period is completed. This is to ensure that the change is saved. When chip returns back to normal operation from power down, it will return to the set up conditions of the last change.

Reference Design

DVDD=AVDD=5.0V, OWR=10Hz (S1=0, S0=0), VRO=4.44V=(1.11*(30K+10K)/10K)

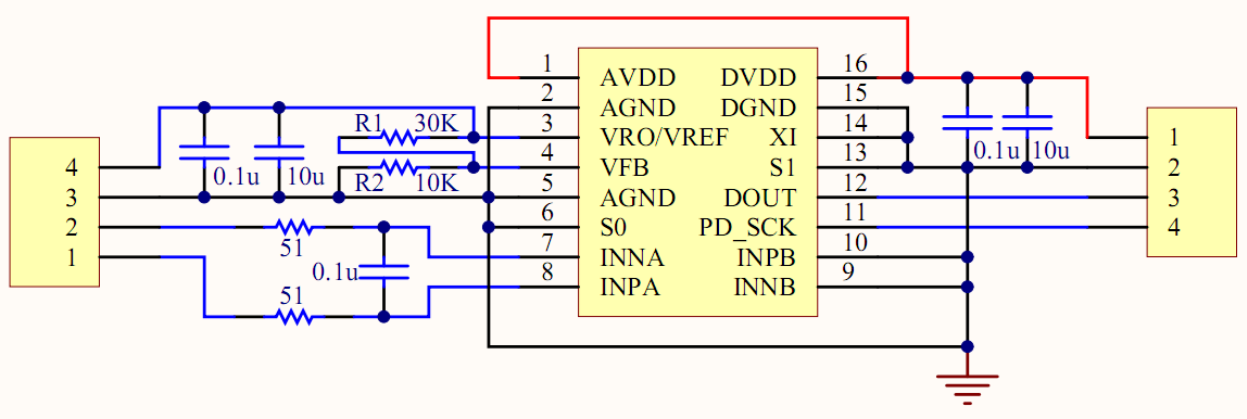


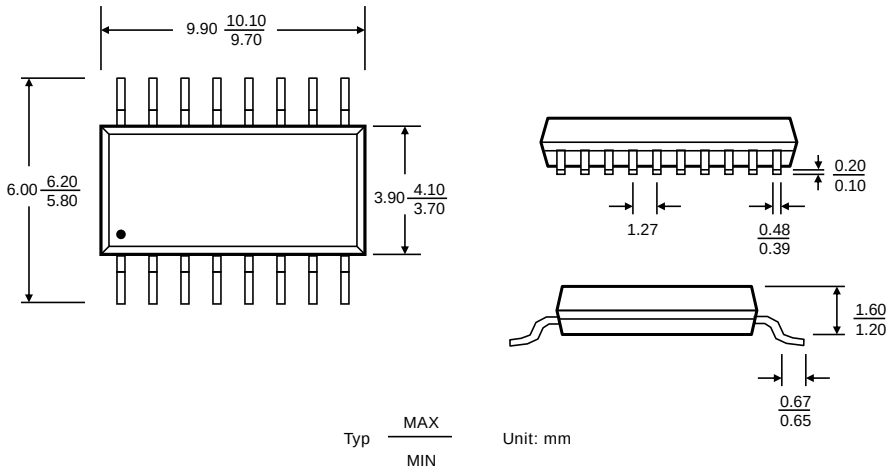
Fig.4 Reference PCB board schematic

Reference Driver (C)

```
ulong  HX717_Read(void)
{
       uchar  i;
       ulong  bcd=0;         // 24 bits

       PD_SCK = 0;
       while (DOUT==1);
       _nop_();              // More than 1uS delay
       _nop_();
       _nop_();
       for (i=0;i<24;i++)
       {
              PD_SCK = 1;    // high time must be less than 50uS
              PD_SCK = 0;
              bcd = bcd<<1;
              if (DOUT==1)  bcd++;
       }
       PD_SCK = 1;
       PD_SCK = 0;
       bcd = bcd^0x800000;   // to unsigned
       return bcd;
}
```

Package Dimensions



SOP-16L Package