24-Bit Analog-to-Digital Converter (ADC) for Weigh Scales

DESCRIPTION

Based on Avia Semiconductor's patented technology, HX71708 is a precision 24-bit analog-to-digital converter (ADC) designed for high precision weigh scales and industrial control applications to interface directly with a bridge sensor.

The input low-noise amplifier (PGA) has a fixed gain of 128, corresponding to a full-scale differential input voltage of ±20mV, when a 5V reference voltage is connected to the VREF pin. On chip oscillator provides the system clock without any external component. On-chip power-on-reset circuitry simplifies digital interface initialization. There is no programming needed for the internal registers. All controls to the HX71708 are through the pins.

FEATURES

- **On-chip low noise amplifier with a gain of 128**
- **On-chip oscillator requiring no external component**
- **On-chip power-on-reset**
- **Simple digital control and serial interface: pin-driven controls, no programming needed**
- **Selectable 10, 20, 80 or 320SPS output data rate**
- **Simultaneous 50 and 60Hz supply rejection**
- **Current consumption: normal operation < 1.5mA, power down < 1uA**
- **Operation supply voltage range: 2.7 ~ 5.5V**
- **Operation temperature range: -40 ~ +85℃**
- **8 pin SOP-8 package**

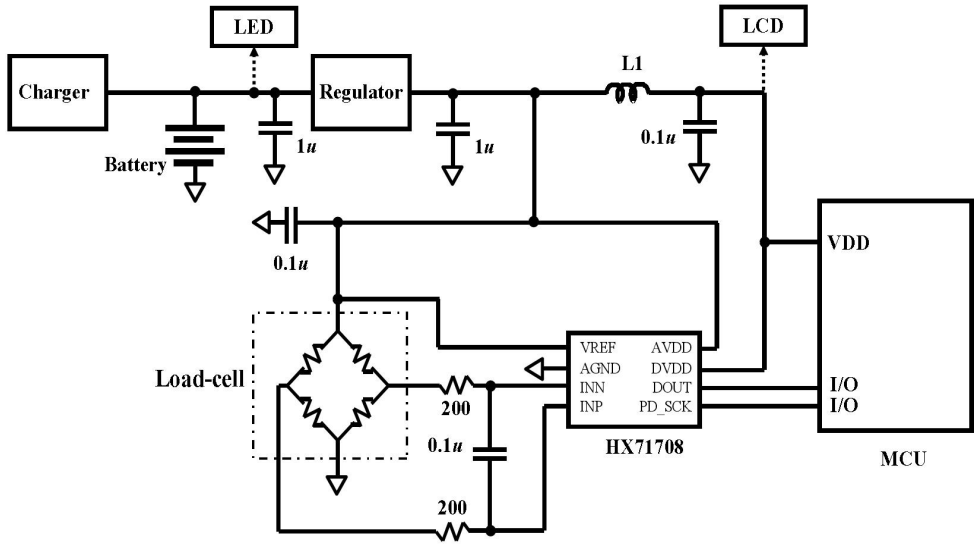
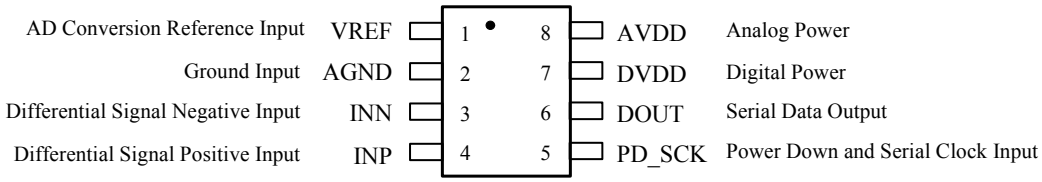


Fig. 1 Typical weigh scale application using HX71708

Pin Description



SOP-8 Package

Pin #	Name	Function	Description
1	VREF	Analog Input	Reference input voltage: 1.8 ~ 5.5V (<=AVDD)
2	AGND	Ground	Analog Ground
3	INN	Analog Input	Differential signal negative input
4	INP	Analog Input	Differential signal positive input
5	PD_SCK	Digital Input	Power down control (high active) and serial clock input
6	DOUT	Digital Output	Serial data output
7	DVDD	Power	Digital supply: 2.7 ~ 5.5V
8	AVDD	Power	Analog supply: 2.7 ~ 5.5V (AVDD must be >= DVDD)

Table 1 Pin Description

KEY ELECTRICAL CHARACTERISTICS

(AVDD=DVDD=VREF=5.0V, Rate=10Hz, unless specifically specified)

Parameters	Note	Min	Typical	Max	Unit
Differential input full scale range (FSR)	V(INP) - V(INN)		±0.5(VREF/GAIN)		V
Input common-mode range	V(INP),V(INN)-AGNG	0.9		AVDD-1.5	V
VREF input voltage range	VREF	1.8		AVDD	V
Noise-Free Bits(1)	f_o = 10Hz, VREF = 5.0V		18.2		Bits
	f_o = 20Hz, VREF = 5.0V		17.7		Bits
	f_o = 80Hz, VREF = 5.0V		16.7		Bits
	f_o = 320Hz, VREF = 5.0V		15.8		Bits
A/D output data rate (f_o)			10/20/80/320		Hz
A/D output number of bits	No missing code		24		Bits
Output data format	2' complement	800000		7FFFFF	HEX
Output data settling time(2)			$4/f_o$		mS
Integral none linearity (INL)			±0.001		%of FS
Input offset			0.01		mV
Equivalent input referred noise	At 0.1Hz		14		nV/√Hz
Temperature Drift	offset drift		±15		nV/℃
	gain drift		±3		ppm/℃
Power supply rejection ratio			100		dB
Common mode rejection ratio	At DC, VIN=10mV		100		dB
Supply voltage		2.7	5.0	5.5	V
Supply current	In operation,VDD=5V		1.5		mA
	Power down		1		uA

（1）Noise-Free Bits = ln(VREF/GAIN/Peak-to-Peak Noise)/ln(2).

（2）Settling time refers to the time from power up, reset, input channel change and gain change to valid stable output data.

Table 2 Key Electrical Characteristics

Analog Input

The differential input is designed to interface directly with a bridge sensor's differential output. It has a fixed gain of 128. The large gains are needed to accommodate the small output signal from the sensor. When a 5V reference is used at the VREF pin, the full-scale differential input voltage range is ±20mV.

Power Supply Options

Digital power supply (DVDD) can be connected directly to AVDD supply. DVDD can also be connect to a different voltage other than AVDD, but should always be less or equal to AVDD. DVDD should be the same or similar voltage as the MCU power supply to ensure proper communication with the MCU.

A/D conversion reference voltage (VREF) should be connected to the load-cell's supply voltage. It can be connected directly to AVDD or through a resistor to reduce the power consumption by the load-cell.

Serial Interface

Pin PD_SCK and DOUT are used for data retrieval, output data rate selection and power down controls.

When output data is not ready for retrieval, digital output pin DOUT is high. Serial clock input PD_SCK should be low. When DOUT goes to low, it indicates data is ready for retrieval. By applying 25~28 positive clock pulses at the PD_SCK pin, data is shifted out from the DOUT output pin. Each PD_SCK pulse shifts out one bit, starting with the MSB bit first, until all 24 bits are shifted out. The 25th pulse at PD_SCK input will pull DOUT pin back to high (Fig.2).

Output data rate selection is controlled by the number of the input PD_SCK pulses (Table 3). PD_SCK clock pulses should not be less than 25 within one conversion period, to avoid causing serial communication error.

PD_SCK Pulses	Output Data Rate
25	10 Hz
26	20 Hz
27	80Hz
28	320 Hz

Table 3 Output Data Rate Selection

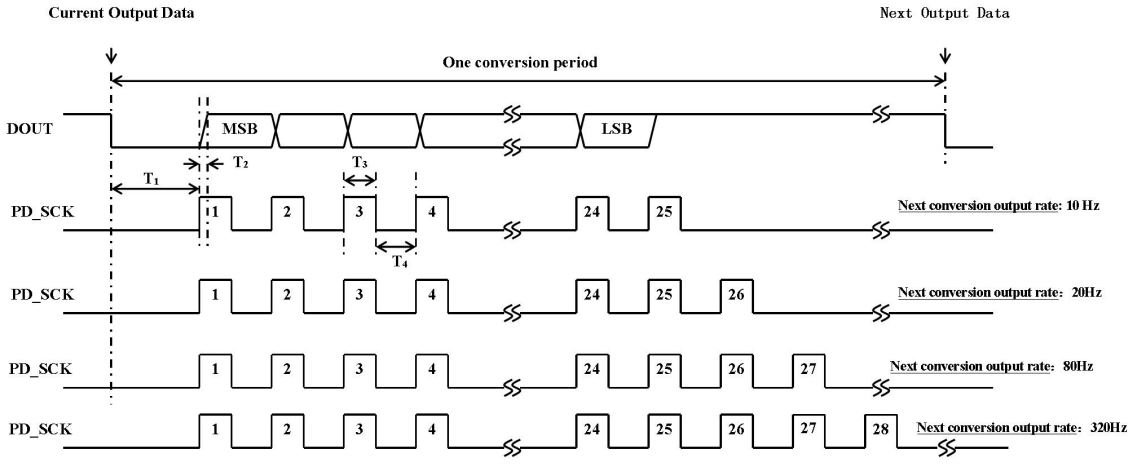


Fig.2 Output data rate selection by PD_SCK pulse number

Symbol	Note	MIN	TYP	MAX	Unit
T_1	DOUT falling edge to PD_SCK rising edge	0.1			μs
T_2	PD_SCK rising edge to DOUT data ready			0.1	μs
T_3	PD_SCK high time	0.2	1	50	μs
T_4	PD_SCK low time	0.2	1		μs

Reset and Power-Down Modes

When chip is powered up, on-chip power on rest circuitry will reset the chip.

Pin PD_SCK input is used to power down the HX71708. When PD_SCK Input is low, chip is in normal working mode.

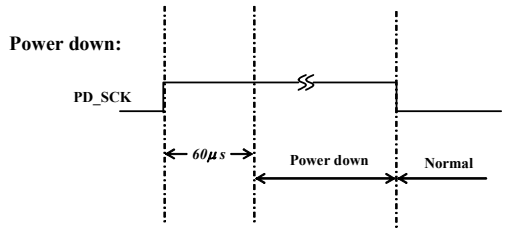


Fig.3 Power down control

When PD_SCK pin changes from low to high and stays high for longer than 80μs, HX71708 enters power down mode (Fig.3).

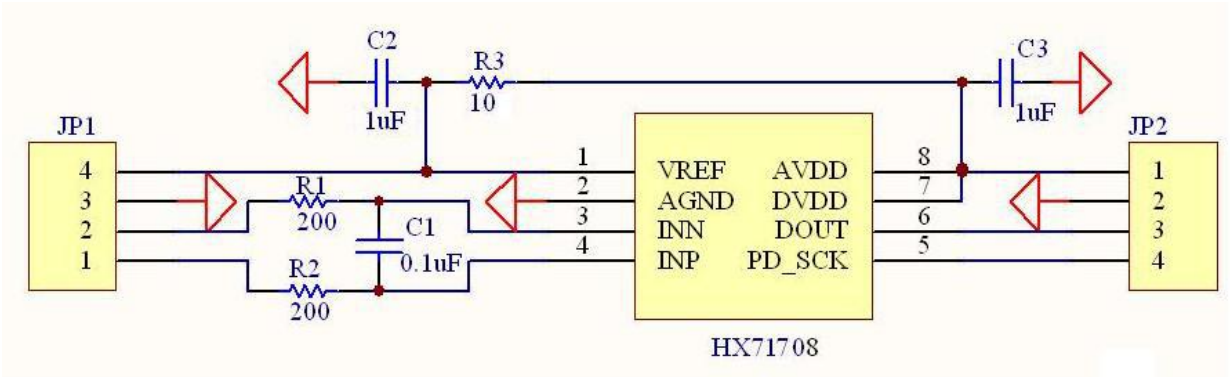
There are 2 power down modes. When PD_SCK input pulses is between 25~29, and PD_SCK is pulled high for more than 80uS, only A/D converter is powered down. Current consumption will be less than 100uA.

If PD_SCK input pulses is 30 and PD_SCK is pulled high for more than 80uS, all will be powered down. Current consumption will be less than 1uA.

When PD_SCK returns to low, chip will return back to the setup conditions the same as before power down and enter normal operation mode.

If PD_SCK pulse number is changed during the current conversion period, power down should be executed after current conversion period is completed. This is to ensure that the change is saved. When chip returns back to normal operation from power down, it will return to the set up conditions of the last change.

Reference Schematic

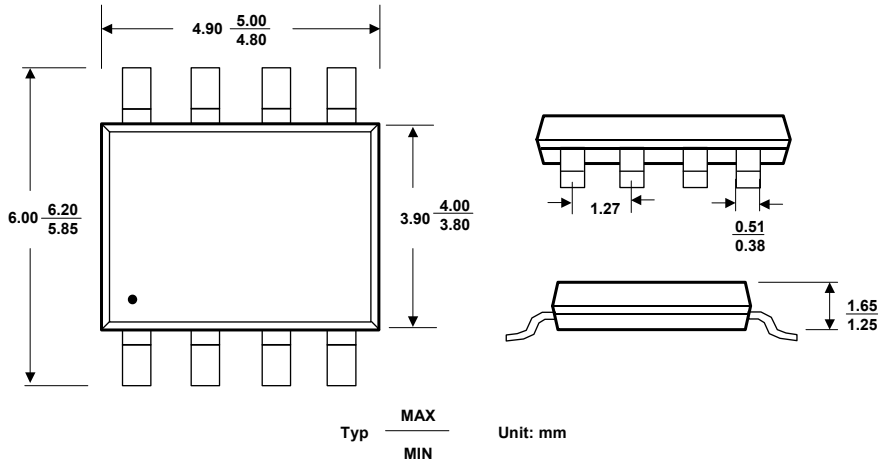


Reference Driver (C)

```
ulong  HX71708_Read(void)
{
       uchar  i;
       ulong  bcd=0;         // 24 bits

       PD_SCK = 0;
       while (DOUT==1);
       _nop_();              // More than 1uS delay
       _nop_();
       _nop_();
       for (i=0;i<24;i++)
       {
              PD_SCK = 1;    // high time must be less than 50uS
              PD_SCK = 0;
              bcd = bcd<<1;
              if (DOUT==1)  bcd++;
       }
       PD_SCK = 1;
       PD_SCK = 0;
       return bcd;
}
```

Package Dimensions



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