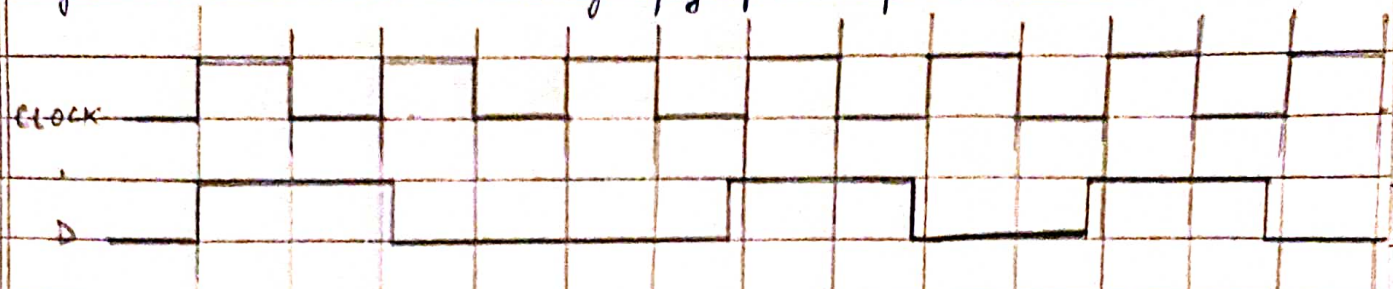
# ASSIGNMENT-2

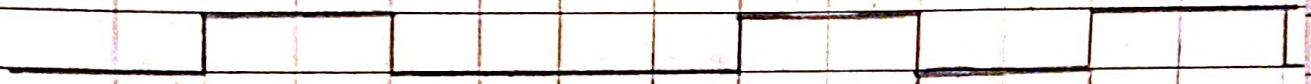
1. Following is a data signal and a clock signal input of some D-latch or D-flip-flop component.




Draw the result signals of :-

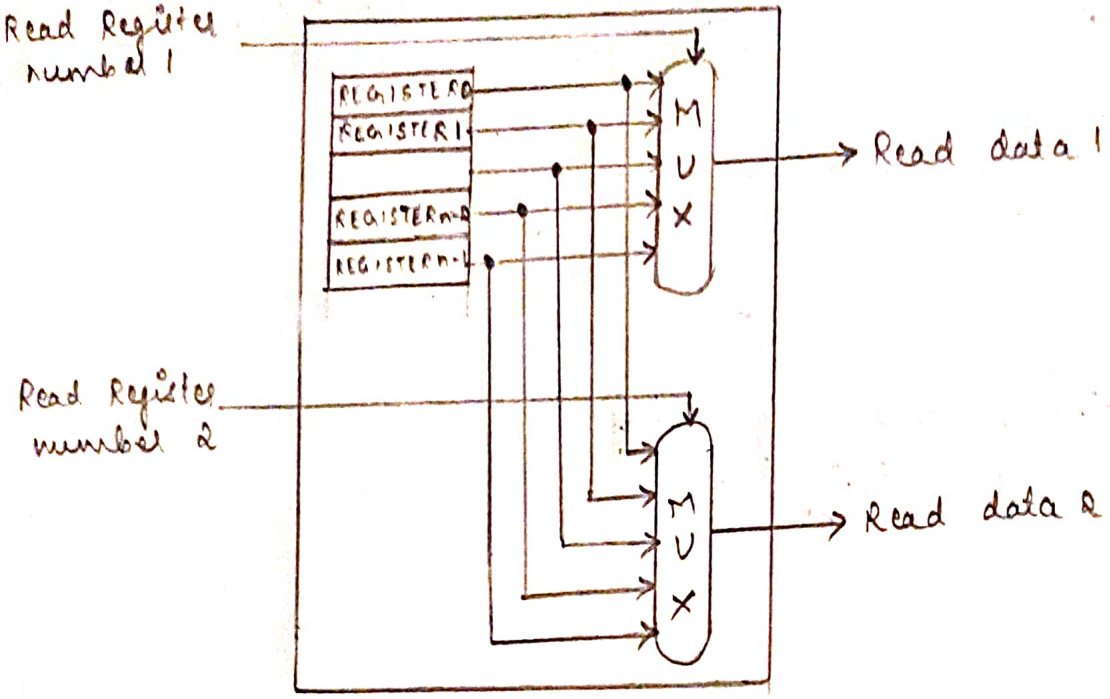
a) rising-edged-triggered

b) falling-edged-triggered



c) level-triggered

2. Since RISC-V instructions very likely need to read two from registers, so register files need to have two read input to select from two registers. Following is a diagram of a 32-bit register with 2 read inputs.




What is the width of red line and green line respectively?

→ Red Line = 1 bit ⇒ It is a selection line.

Green line = 32 bits ⇒ Each register is 32 bits.

3. Redesign the register file in Question 2 using D-flip-flop. The new register file will have two 2-bit registers and 1 read input.

→