Assignment #2

COEN210
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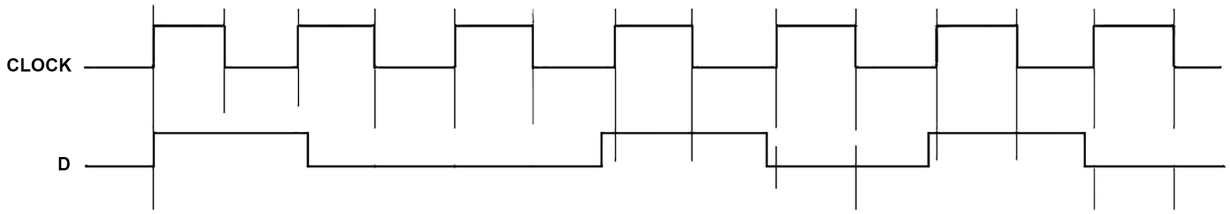
Question 1

Following is a data signal and a clock signal input of some D-latch or D-flip-flop component.

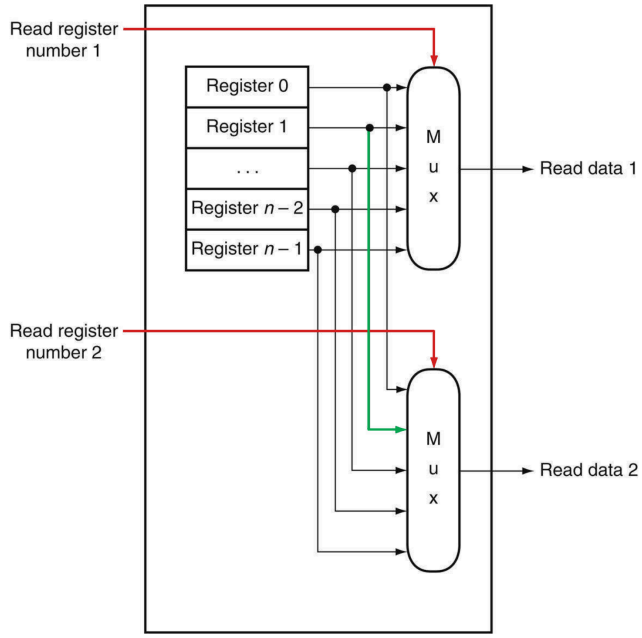


Draw the result signals of:

a. rising-edge-triggered
b. falling-edge-triggered
c. level-triggered.

Question 2

Since RISC-V instructions very likely need to read two from registers, so register file need to have two read input to select from two registers. Following is a diagram of n 32-bit registers with 2 data read inputs.



What is the width of red line and green line respectively?

Question 3

Redesign the register file in Question 2 using D flip-flops. The new register file will have two 2-bit registers and 1 read input.