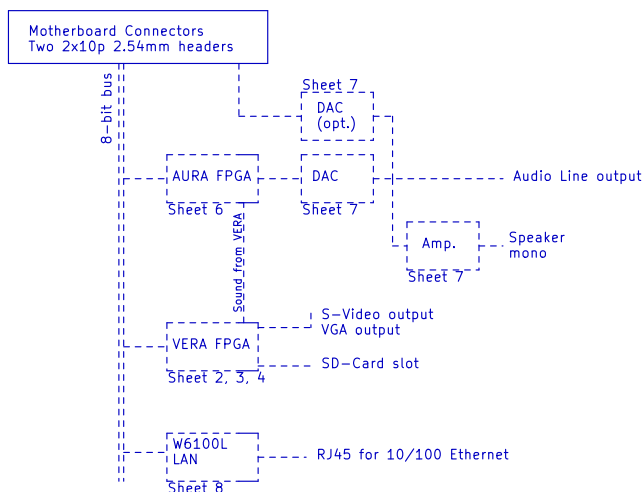


OpenX65 Video/Audio & Ethernet Board ("V/A-B0")

Block Diagram:



- FID101 Fiducial
- FID102 Fiducial
- FID103 Fiducial
- H101 MountingHole
- H102 MountingHole
- H103 MountingHole
- H104 MountingHole

This schematic contains portions of work done by Frank van den Hoe for the project VERA: <https://github.com/fvdhoef/vera-module>

Revision History:

Rev. / Date	Description
rev01 / 28.4.2023	Initial design, PCB 100x100mm 2-layers. VERA with VGA and S-Video outputs. AURA with line-out and amp/speaker, 2 DAC. LAN by W6100L

Sheets:

Video VERA FPGA



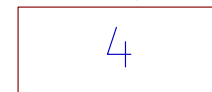
Soubor: vabo-sheet-02.kicad_sch

Video Outputs



Soubor: vabo-sheet-03.kicad_sch

VERA SPI-Flash, SDC



Soubor: vabo-sheet-04.kicad_sch

Motherboard Connectors



Soubor: vabo-sheet-05.kicad_sch

Audio AURA FPGA



Soubor: vabo-sheet-06.kicad_sch

Audio DAC, Output



Soubor: vabo-sheet-07.kicad_sch

Ethernet



Soubor: vabo-sheet-08.kicad_sch

Block Diagram

FOR X65.EU DESIGNED BY JSYKORA.INFO

Sheet: /

File: openX65-vabo.kicad_sch

Title: OpenX65 – Video/Audio & Ethernet Board

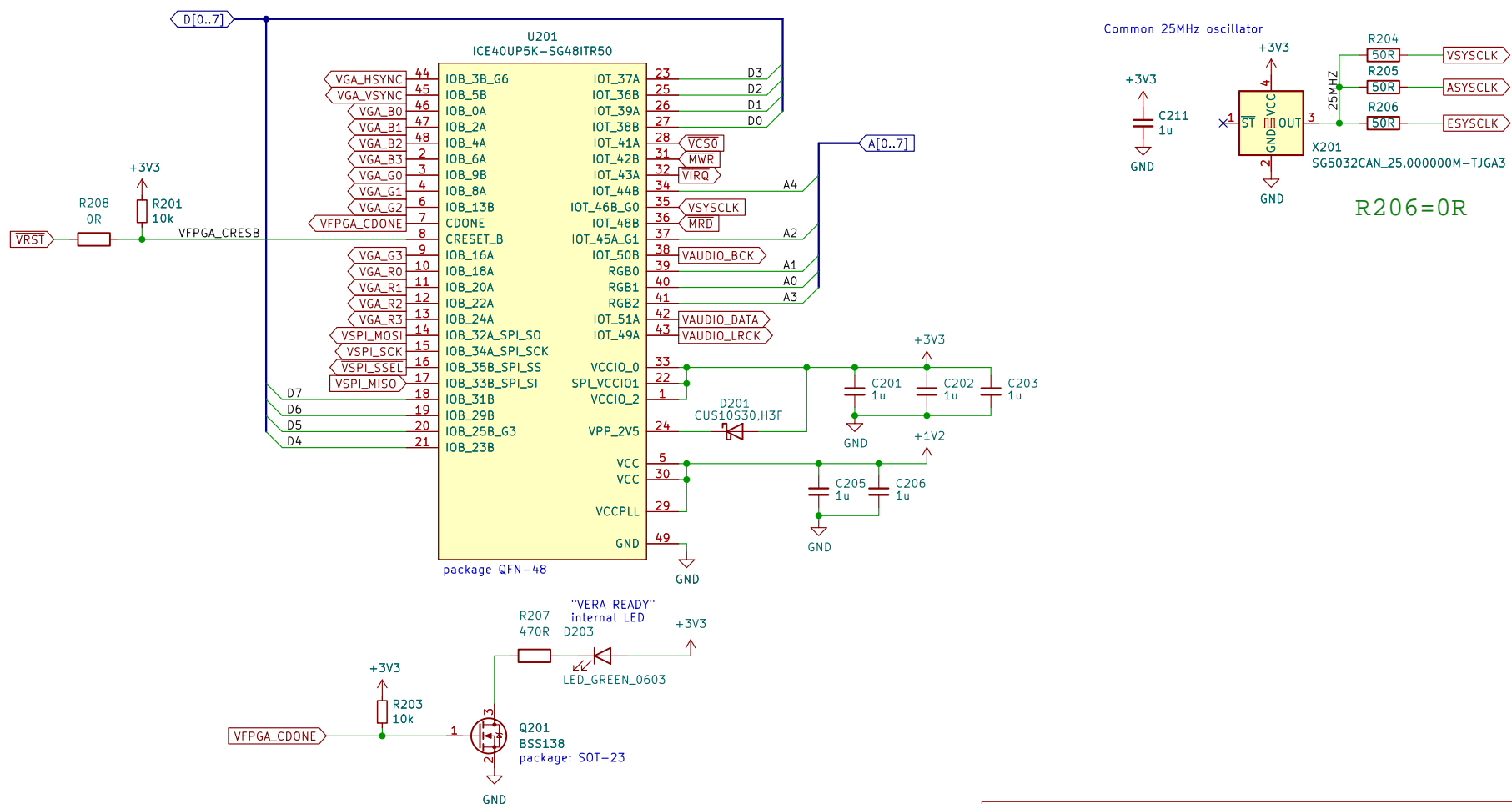
Size: A4 Date: 2023-04-28

KiCad E.D.A. kicad 6.0.11-3.fc36

Rev: rev01

Id: 1/8

"VERA" FPGA – Video Embedded Retro Adapter



This schematic contains portions of work done by Frank van den Hoe for the project VERA: <https://github.com/fvdhoe/vera-module>

VERA FPGA design by Frank van den Hoe
FOR X65.EU DESIGNED BY JSYKORA.INFO

Sheet: /Video VERA FPGA/
File: vabo-sheet-02.kicad_sch

Title: OpenX65 – Video/Audio & Ethernet Board

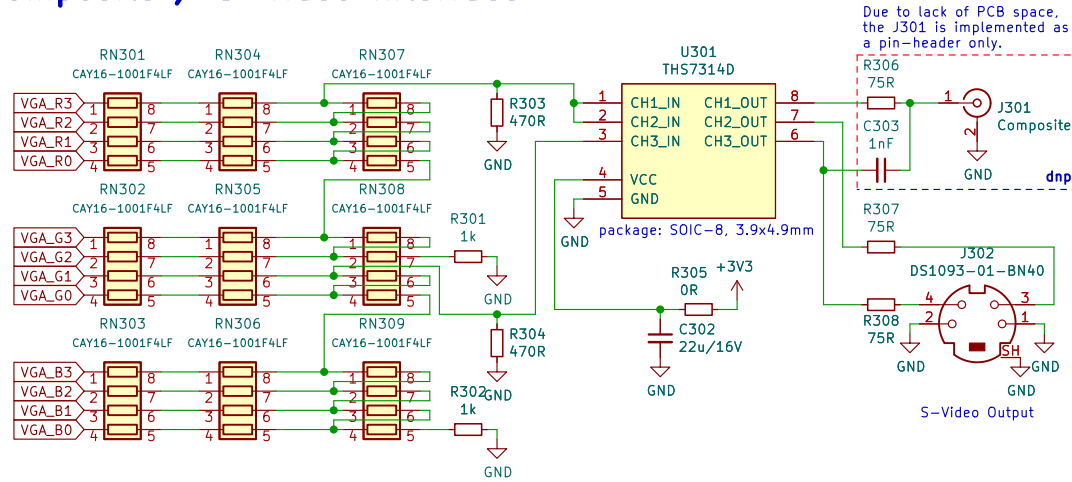
Size: A4 Date: 2023-04-28

KiCad E.D.A. kicad 6.0.11-3.fc36

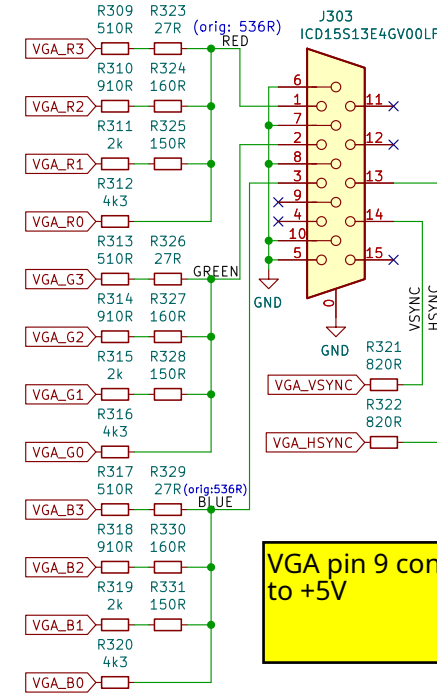
Rev: rev01

Id: 2/8

Composite / S-video interface



VGA interface



This schematic contains portions of work done by Frank van den Hoe for the project VERA: <https://github.com/fvdhoef/vera-module>

Video outputs from VERA
FOR X65.EU DESIGNED BY JSYKORA.INFO

Sheet: /Video Outputs/
File: vabo-sheet-03.kicad_sch

Title: OpenX65 – Video/Audio & Ethernet Board

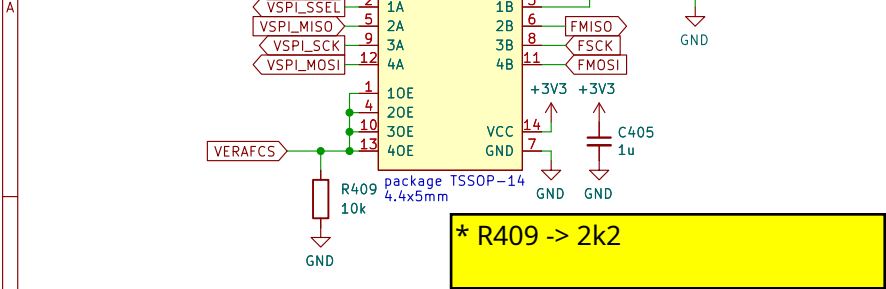
Size: A4 Date: 2023-04-28

KiCad E.D.A. kicad 6.0.11-3.fc36

Rev: rev01

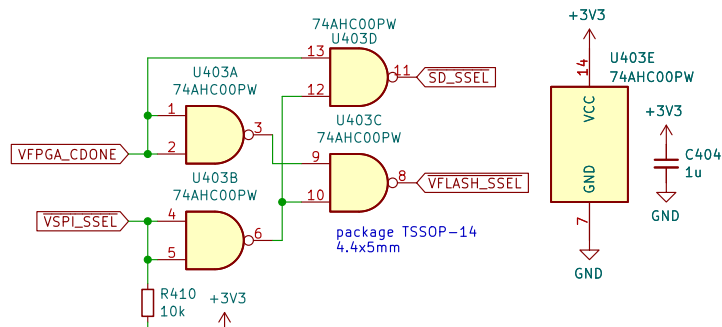
Id: 3/8

1	2	3	4	5	6
---	---	---	---	---	---



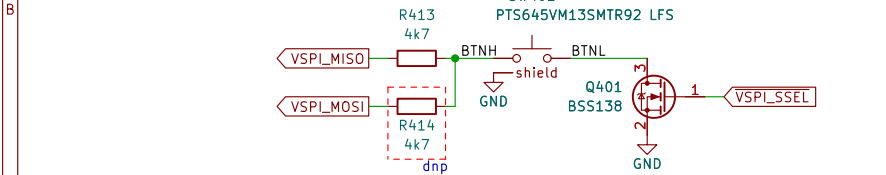
* R409 -> 2k2

VERA SPI pins multiplexing

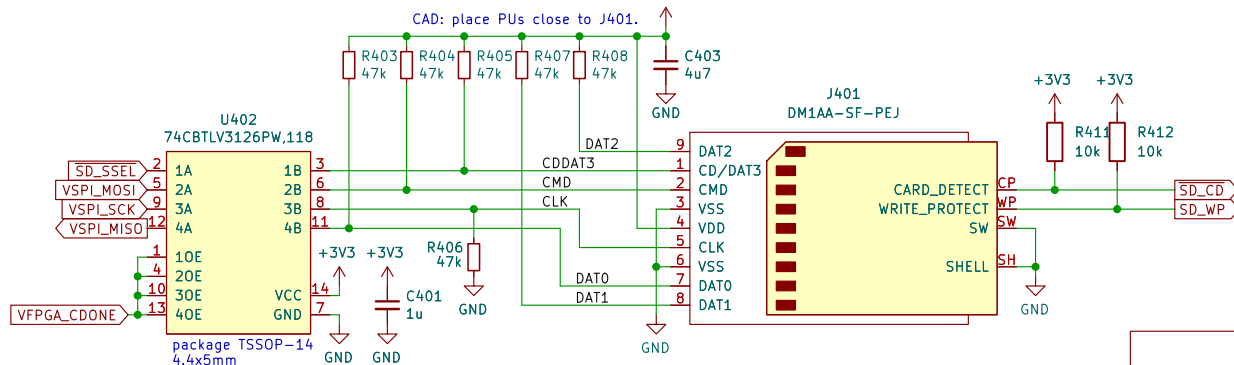


Inputs		Outputs		Description
VFPGA_CDONE	VSPI_SSEL	SD_SSEL	VFLASH_SSEL	
0	0	1	0	FPGA configuring from the SPI-Flash, or FTDI/ICD accessing.
0	1	1	1	FPGA empty/in-reset
1	0	0	1	FPGA loaded; User Design r/w to SDC
1	1	1	1	FPGA loaded; idle

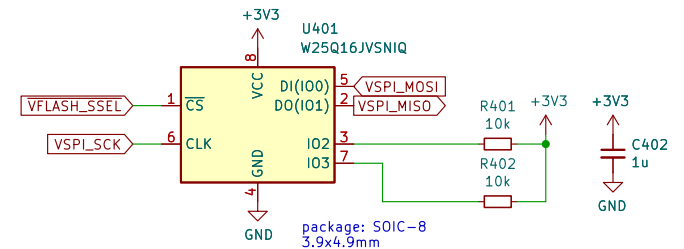
B	R413	PTS645VM13SMTR92 LFS	1	1	1	1	FPGA loaded; idle	B
---	------	----------------------	---	---	---	---	-------------------	---



J401	75V	75V	GND	3.9x4.9mm
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SPI flash for VERA Bitstream



* add PD to VSPI_SCK
(strictly not necessary - dnp)

This schematic contains portions of work done by Frank van den Hoe for the project VERA: <https://github.com/fvdhoef/vera-module>

VERA SPI multiplexing, SDC interface
FOR X65.EU DESIGNED BY JSYKORA.INFO

Sheet: /VERA SPI-Flash, SDC/
File: vabo-sheet-04.kicad_sch

Title: OpenX65 – Video/Audio & Ethernet Board

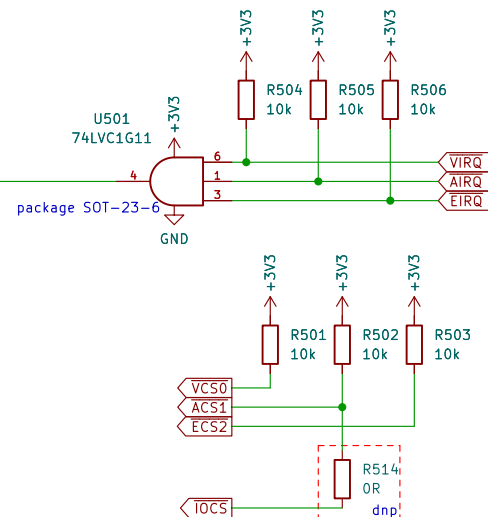
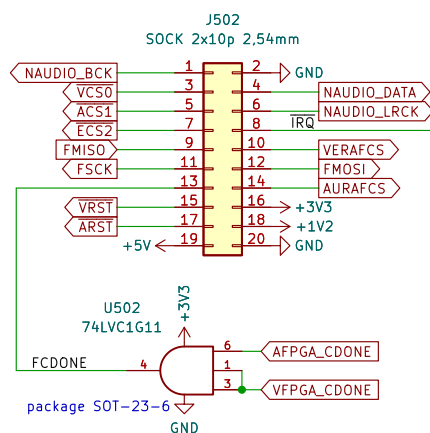
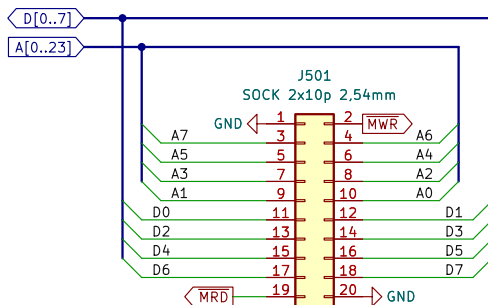
Size: A4	Date: 2023-04-28
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Rev: rev01

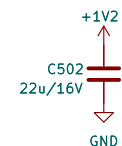
KiCad E.D.A.	kicad 6.0.11-3.fc36
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Id: 4/8

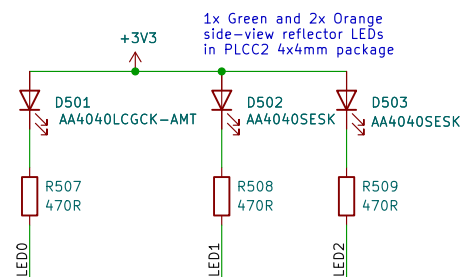
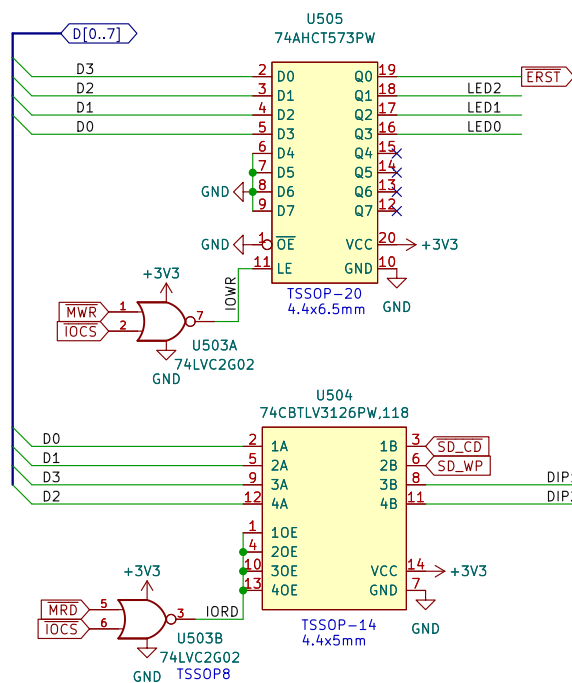
Connectors to the Motherboard



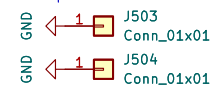
Mount R514 only if AURA
is mounted not
(bypass ACS directly to IOCS).



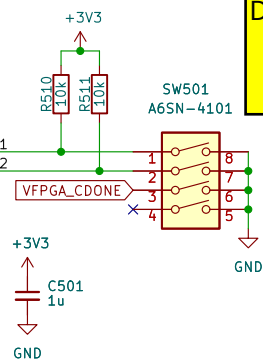
I/O: LEDs & DIP Switches



Ground pins for measurements



LED out works OK.
DIP in - does not?! reads always 0x00



Motherboard Connectors, simple I/O
FOR X65.EU DESIGNED BY JSYKORA.INFO

Sheet: /Motherboard Connector

File: vabo-sheet-05.kicad_sch

Title: OpenX65 – Video/Audio & Ethernet Board

Size: A4	Date: 2023-04-28
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Rev: rev01

Id: 5/8

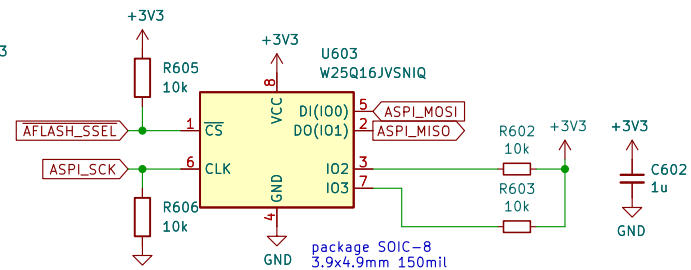
For X16 compatibility, AURA will implement the YM2151 FM-Synthesis (the chip is long out of production). One possible design is JT51 at <https://github.com/jotego/jt51> which requires about 2K gates (i.e. ICE5LP2K-SG48 – to be validated)



The schematic diagram shows the 74CBTLV3126PW118 component with the following connections:

- Pin 1:** Connected to AFLASH_SSEL.
- Pin 2:** Connected to ASPL_MOSI.
- Pin 3:** Connected to ASPL_SCK.
- Pin 4:** Connected to ASPL_MISO.
- Pin 5:** Connected to AFLASH_SSEL.
- Pin 6:** Connected to FMOSI.
- Pin 7:** Connected to FSCCK.
- Pin 8:** Connected to FMISO.
- Pin 9:** Connected to AFLASH_SSEL.
- Pin 10:** Connected to ASPL_MOSI.
- Pin 11:** Connected to ASPL_SCK.
- Pin 12:** Connected to ASPL_MISO.
- Pin 13:** Connected to AURAFCS.
- Pin 14:** Connected to +3V3.
- Pin 15:** Connected to +3V3.
- Pin 16:** Connected to GND.
- Pin 17:** Connected to GND.
- Pin 18:** Connected to GND.
- Pin 19:** Connected to GND.
- Pin 20:** Connected to GND.
- Pin 21:** Connected to GND.
- Pin 22:** Connected to GND.
- Pin 23:** Connected to GND.
- Pin 24:** Connected to GND.
- Pin 25:** Connected to GND.
- Pin 26:** Connected to GND.
- Pin 27:** Connected to GND.
- Pin 28:** Connected to GND.
- Pin 29:** Connected to GND.
- Pin 30:** Connected to GND.
- Pin 31:** Connected to GND.
- Pin 32:** Connected to GND.
- Pin 33:** Connected to GND.
- Pin 34:** Connected to GND.
- Pin 35:** Connected to GND.
- Pin 36:** Connected to GND.
- Pin 37:** Connected to GND.
- Pin 38:** Connected to GND.
- Pin 39:** Connected to GND.
- Pin 40:** Connected to GND.
- Pin 41:** Connected to GND.
- Pin 42:** Connected to GND.
- Pin 43:** Connected to GND.
- Pin 44:** Connected to GND.
- Pin 45:** Connected to GND.
- Pin 46:** Connected to GND.
- Pin 47:** Connected to GND.
- Pin 48:** Connected to GND.
- Pin 49:** Connected to GND.
- Pin 50:** Connected to GND.
- Pin 51:** Connected to GND.
- Pin 52:** Connected to GND.
- Pin 53:** Connected to GND.
- Pin 54:** Connected to GND.
- Pin 55:** Connected to GND.
- Pin 56:** Connected to GND.
- Pin 57:** Connected to GND.
- Pin 58:** Connected to GND.
- Pin 59:** Connected to GND.
- Pin 60:** Connected to GND.
- Pin 61:** Connected to GND.
- Pin 62:** Connected to GND.
- Pin 63:** Connected to GND.
- Pin 64:** Connected to GND.
- Pin 65:** Connected to GND.
- Pin 66:** Connected to GND.
- Pin 67:** Connected to GND.
- Pin 68:** Connected to GND.
- Pin 69:** Connected to GND.
- Pin 70:** Connected to GND.
- Pin 71:** Connected to GND.
- Pin 72:** Connected to GND.
- Pin 73:** Connected to GND.
- Pin 74:** Connected to GND.
- Pin 75:** Connected to GND.
- Pin 76:** Connected to GND.
- Pin 77:** Connected to GND.
- Pin 78:** Connected to GND.
- Pin 79:** Connected to GND.
- Pin 80:** Connected to GND.
- Pin 81:** Connected to GND.
- Pin 82:** Connected to GND.
- Pin 83:** Connected to GND.
- Pin 84:** Connected to GND.
- Pin 85:** Connected to GND.
- Pin 86:** Connected to GND.
- Pin 87:** Connected to GND.
- Pin 88:** Connected to GND.
- Pin 89:** Connected to GND.
- Pin 90:** Connected to GND.
- Pin 91:** Connected to GND.
- Pin 92:** Connected to GND.
- Pin 93:** Connected to GND.
- Pin 94:** Connected to GND.
- Pin 95:** Connected to GND.
- Pin 96:** Connected to GND.
- Pin 97:** Connected to GND.
- Pin 98:** Connected to GND.
- Pin 99:** Connected to GND.
- Pin 100:** Connected to GND.

R601 -> 2k2



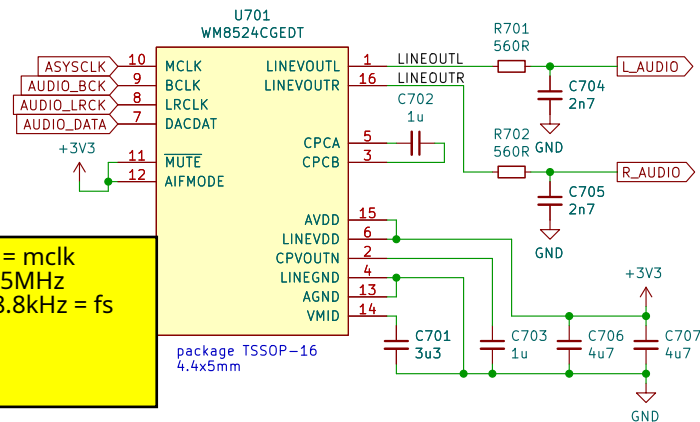
Sheet: /Audio AURA FPGA/
File: vabo-sheet-06.kicad_sch

Size: A4	Date: 2023-04-28
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KiCad E.D.A.	kiCad 6.0.11-3.fc36
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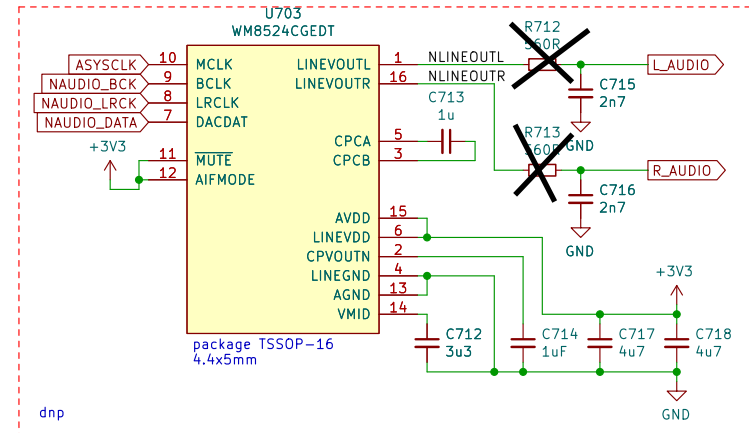
Rev: rev01
Id: 6/8

Audio DAC (PCM/PSG in VERA, FM in AURA)

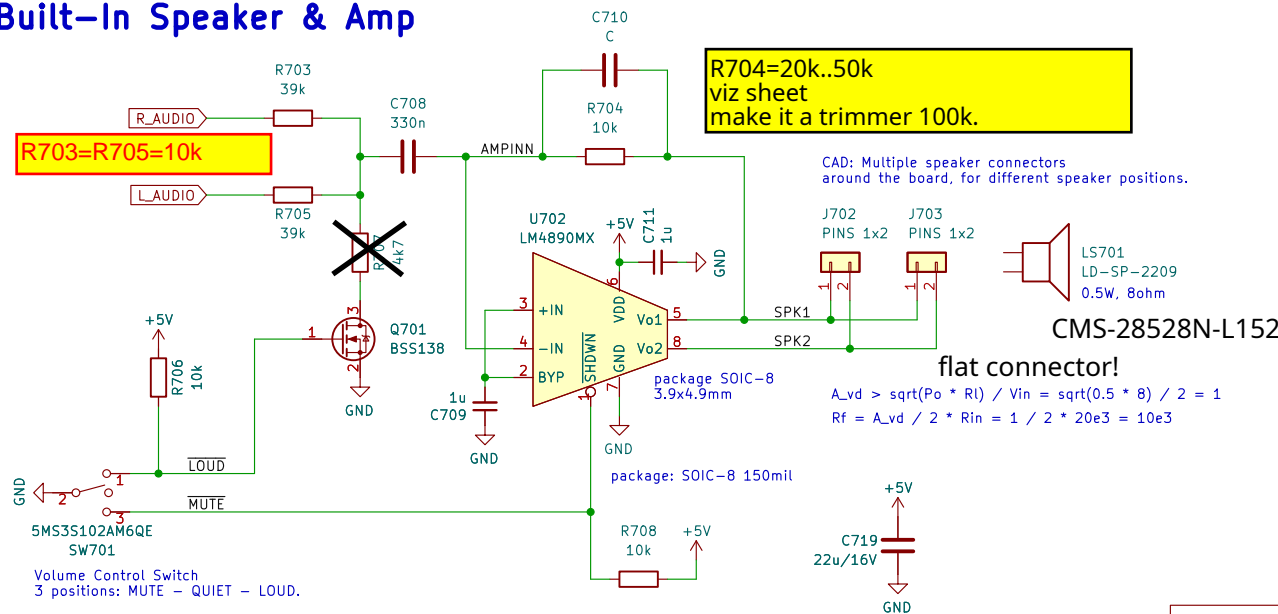


ASYCLK=25MHz = mclk
AUDIO_BCLK=12.5MHz
AUDIO_LRCLK=48.8kHz = fs
=> mclk = 512*fs

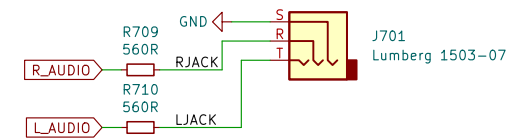
Audio DAC (Sound from NORA) – optional.



Built-In Speaker & Amp



3.5mm jack – AUDIO LINE output



This schematic contains portions of work done by Frank van den Hoe for the project VERA: <https://github.com/fvdhoef/vera-module>

Audio DAC, Speaker Amplifier, and Line Output
FOR X65.EU DESIGNED BY JSYKORA.INFO

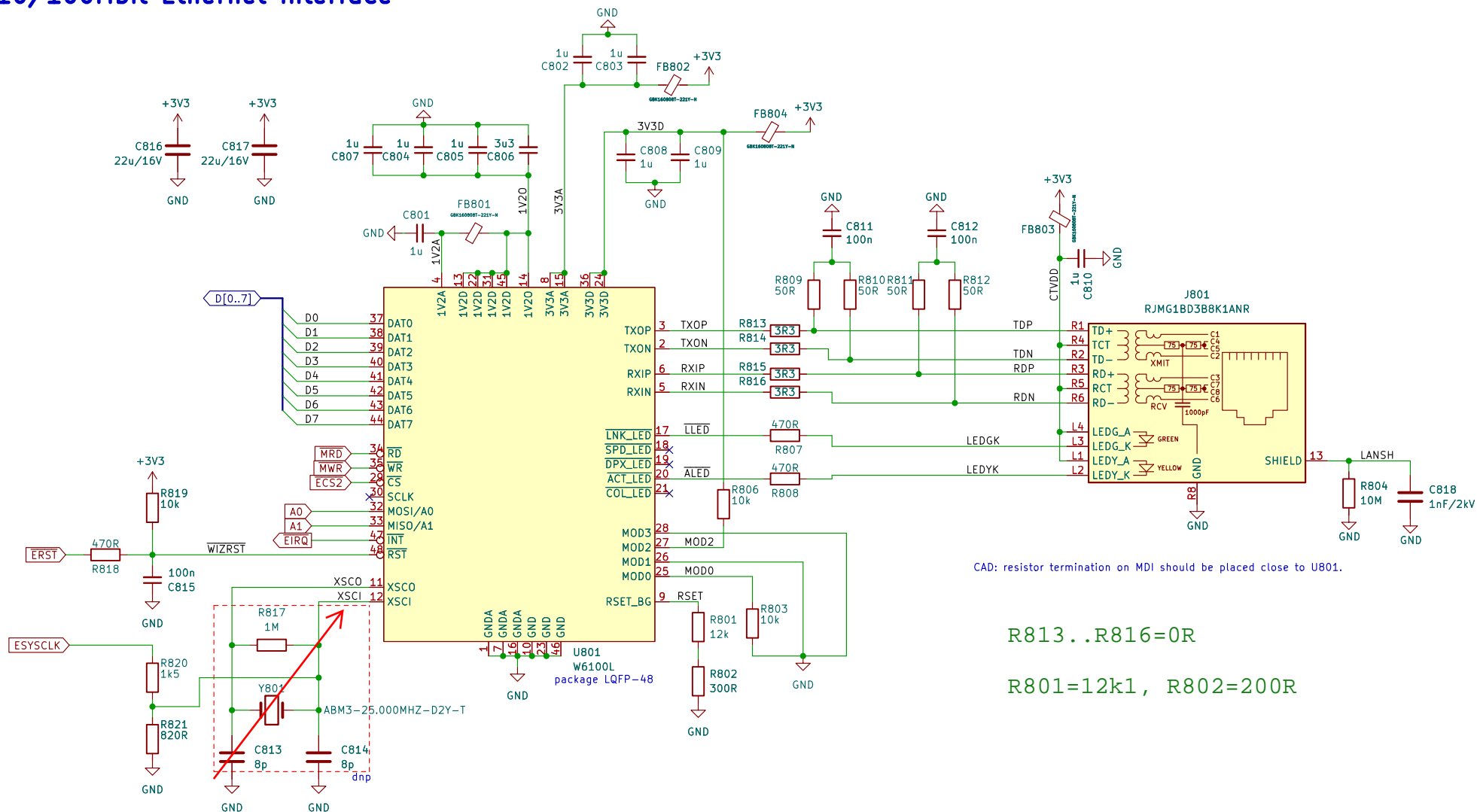
Sheet: /Audio DAC, Output/
File: vabo-sheet-07.kicad_sch

Title: OpenX65 – Video/Audio & Ethernet Board

Size: A4 Date: 2023-04-28
KiCad E.D.A. kicad 6.0.11-3.fc36

Rev: rev01
Id: 7/8

10/100Mbit Ethernet Interface



CAD: resistor termination on MDI should be placed close to U801.

R813..R816=0R

R801=12k1, R802=200R

XSCI requires 25MHz @ 1.2V levels, rise/fall time <8ns

R820=330R
R821=200R
R206=0R
=> rise/fall=5.2ns, top=1.14V

Ethernet LAN Interface (Wiznet)
FOR X65.EU DESIGNED BY JSYKORA.INFO

Sheet: /Ethernet/
File: vabo-sheet-08.kicad_sch

Title: OpenX65 - Video/Audio & Ethernet Board

Size: A4 Date: 2023-04-28

KiCad E.D.A. kicad 6.0.11-3.fc36

Rev: rev01

Id: 8/8