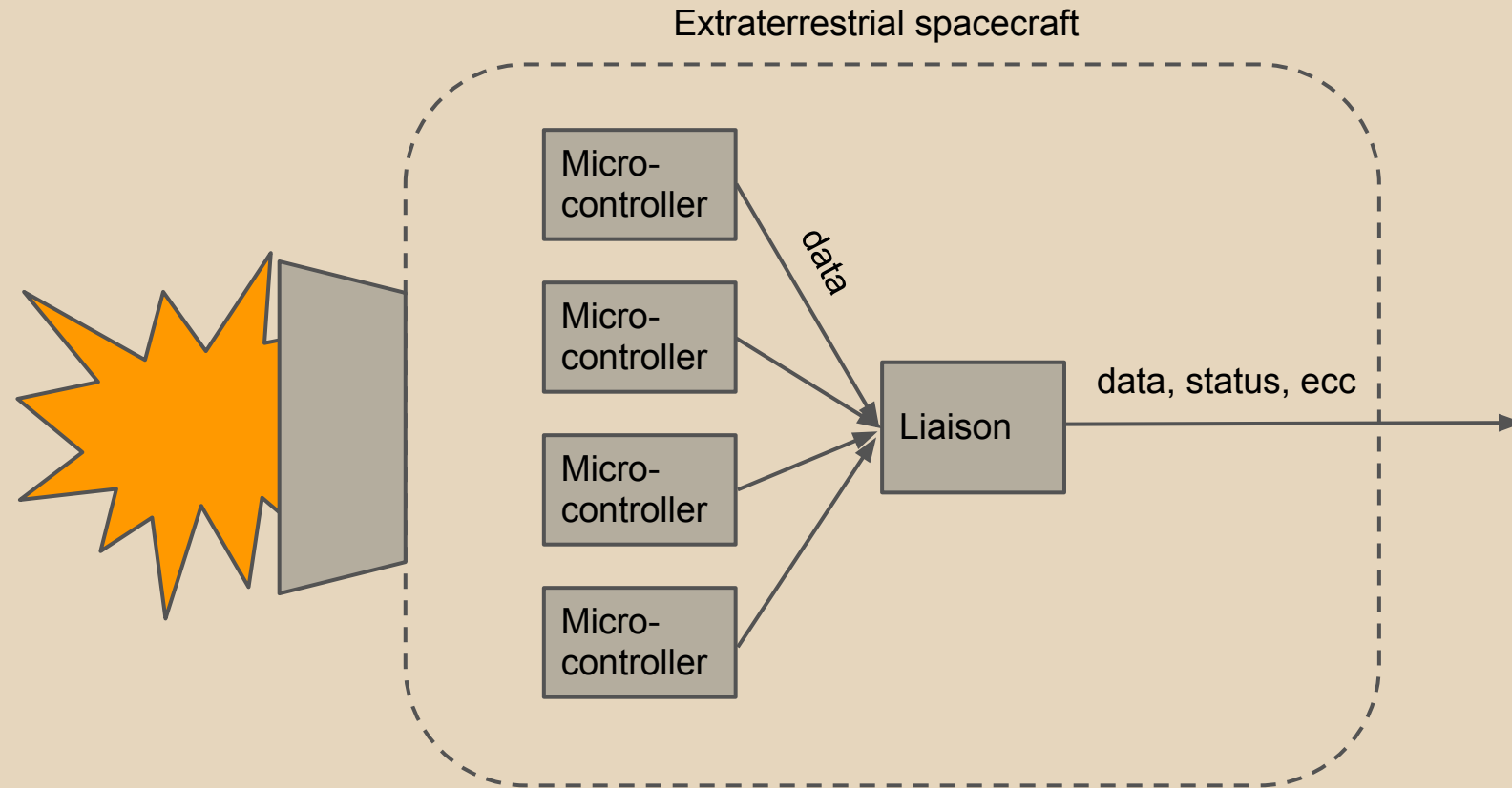# Presentation of Liaison

Voting system for extraterrestrial space craft
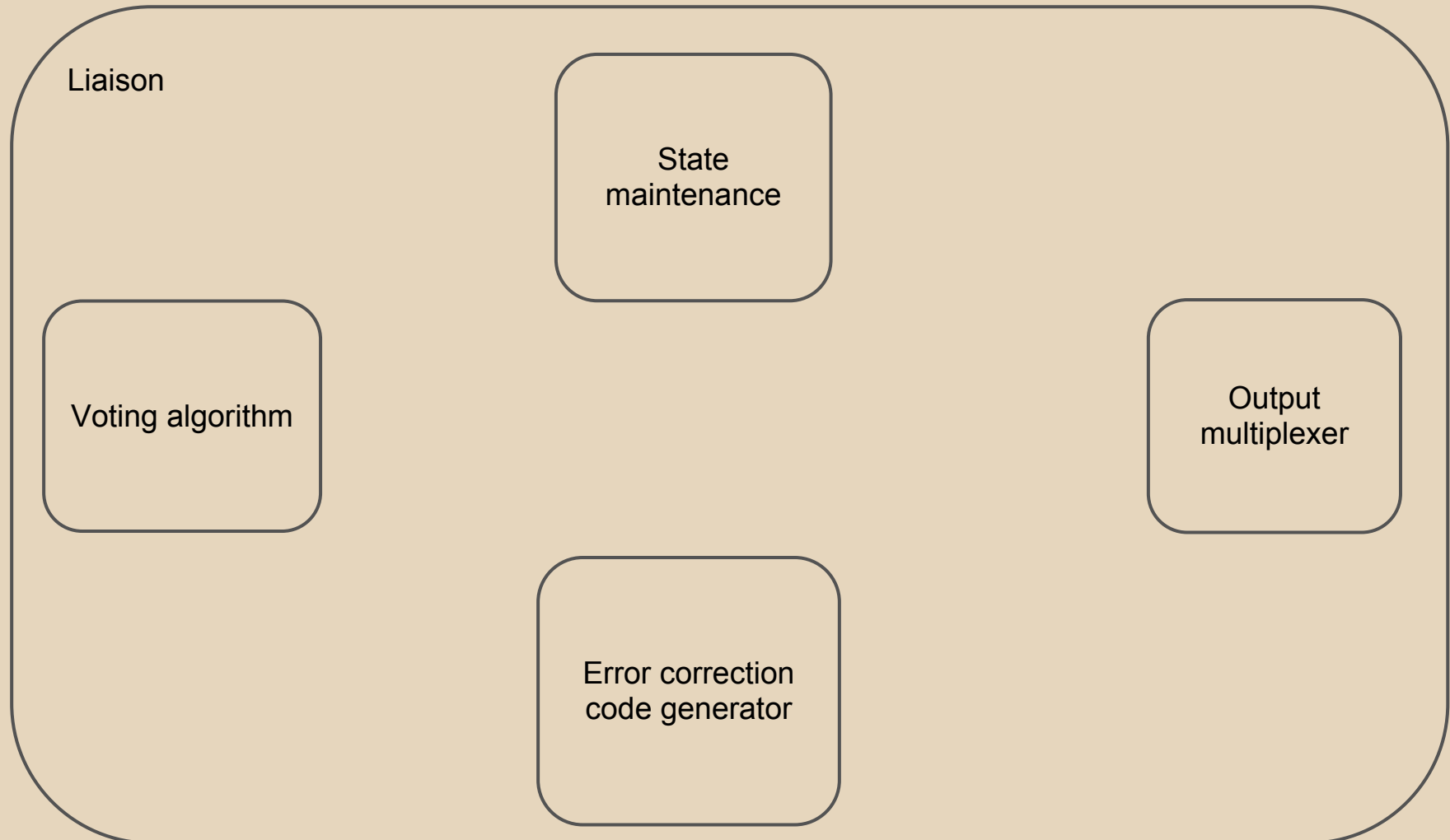
Presentation Outline

- What does our system do?
- How does it do it?
  - Block diagram
  - Algorithms
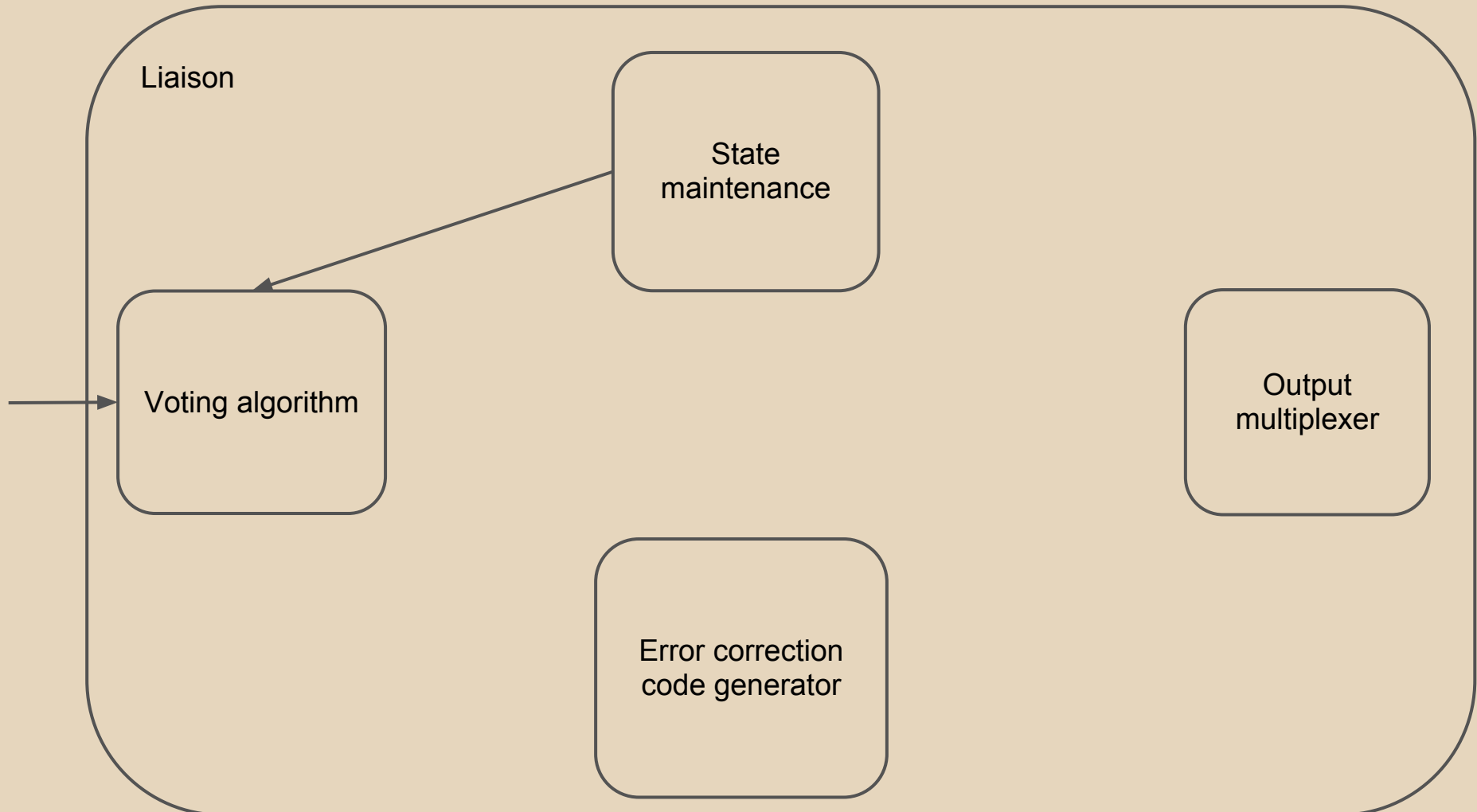- System performance
  - Area
  - Timing

System Overview

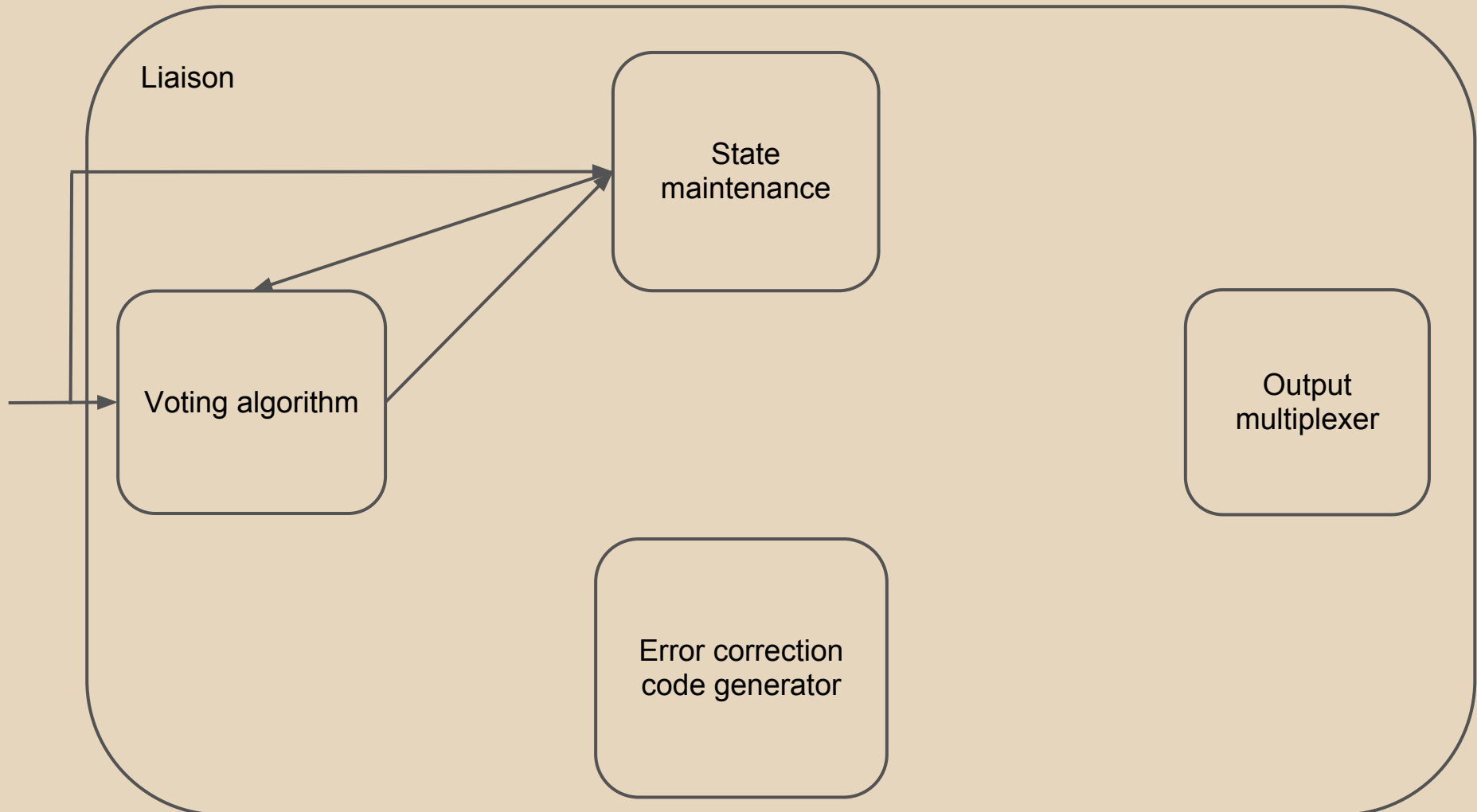# Block Diagram

Liaison

State maintenance

Voting algorithm

Output multiplexer

Error correction code generator

Block Diagram

Block Diagram

Liaison

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Block Diagram

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Output multiplexer
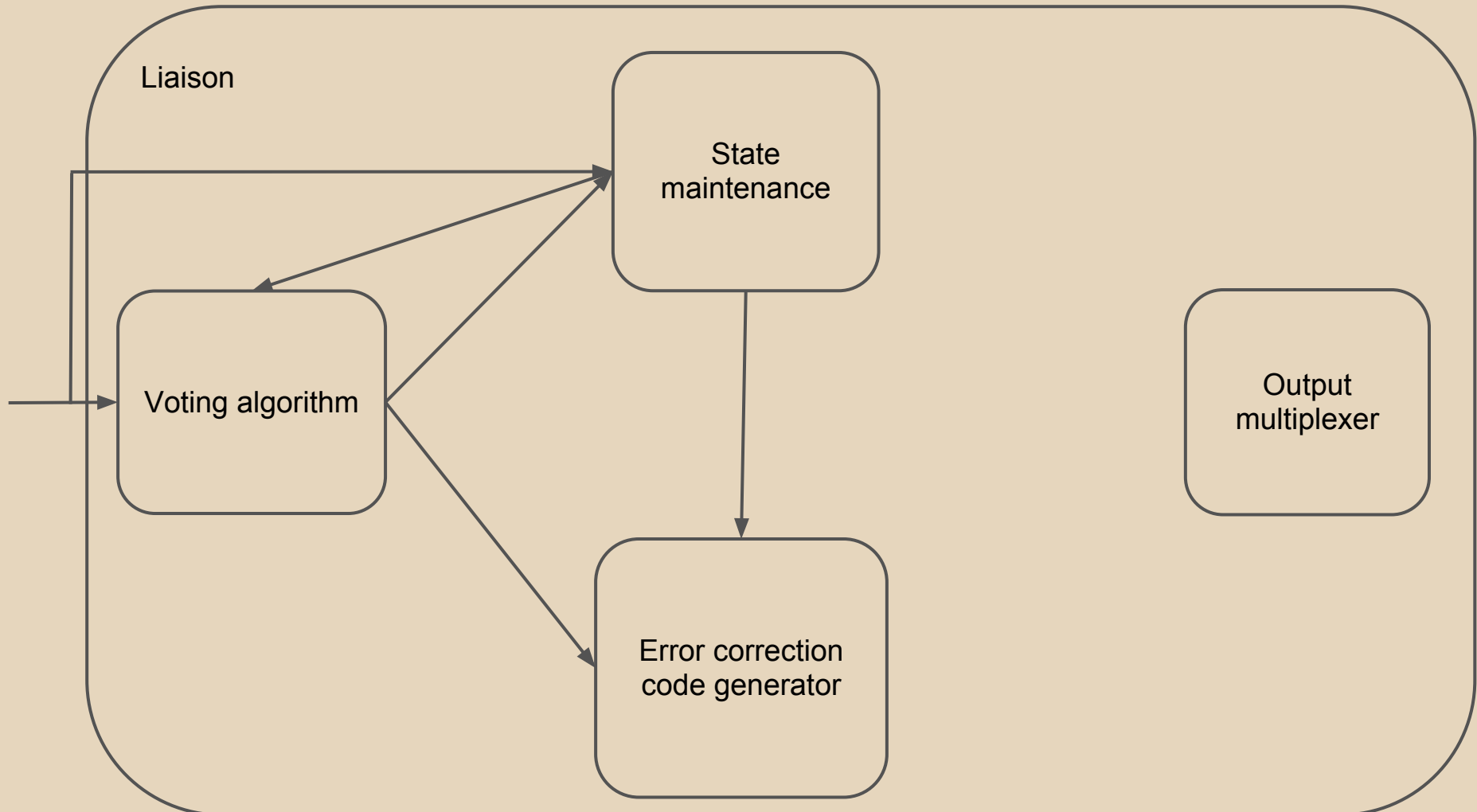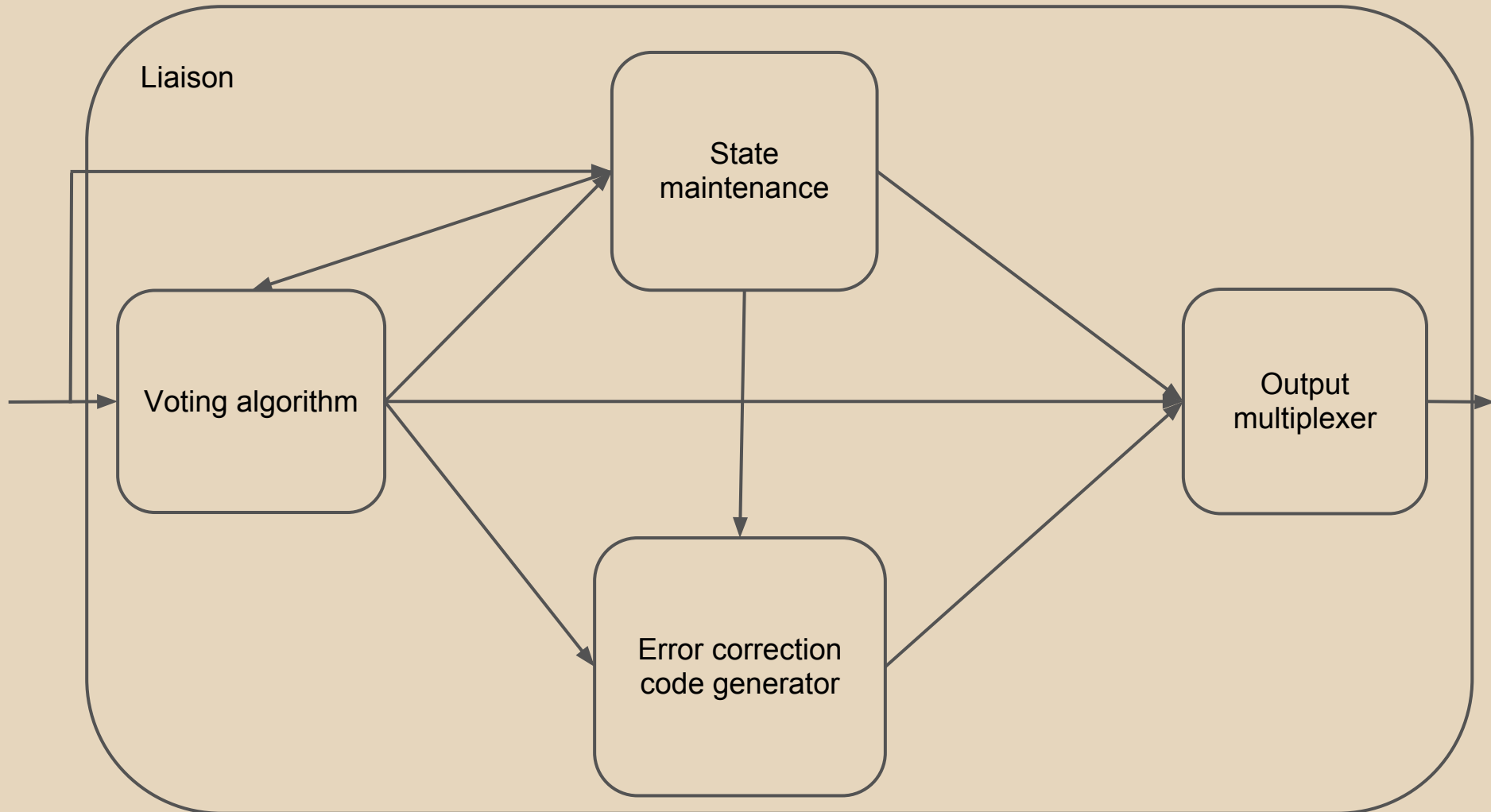
Block Diagram

Voting Algorithm

- MCUs are designated by A,B,C and D, and they are tagged if the system detects a false value

- The MCUs are assigned in groups of (A,B) and (C,D)

- Each group have a "local vote", where the first is chosen if it works, else the second is chosen if it works, else '0' is voted.

Voting Algorithm

- If both A and B works and agree on output, it is always safe to select result from (A,B)

- Else if C and D agree, it is safe to select the result from (C,D)
  - (A,B) is not safe, thus counts as one vote.
  - (C,D) counts as 2,1 or 0 votes, according to state.
    - This means majority, decisive vote or broken

- Else if C and D does not agree, the answers from (A,B) and (C,D) are ORed together, since neither of the groups represent the majority

State Maintenance

- The internal state is represented by three state elements
  - Output stage
  - Error tags
  - Intermediate parity bits calculation

- The output stage is a one-hot 16-flip-flop shift register

- The error tags are set when a MCU gives different result than voted output

- The parity bits are calculated using current output combined with the output stage

Error Correction
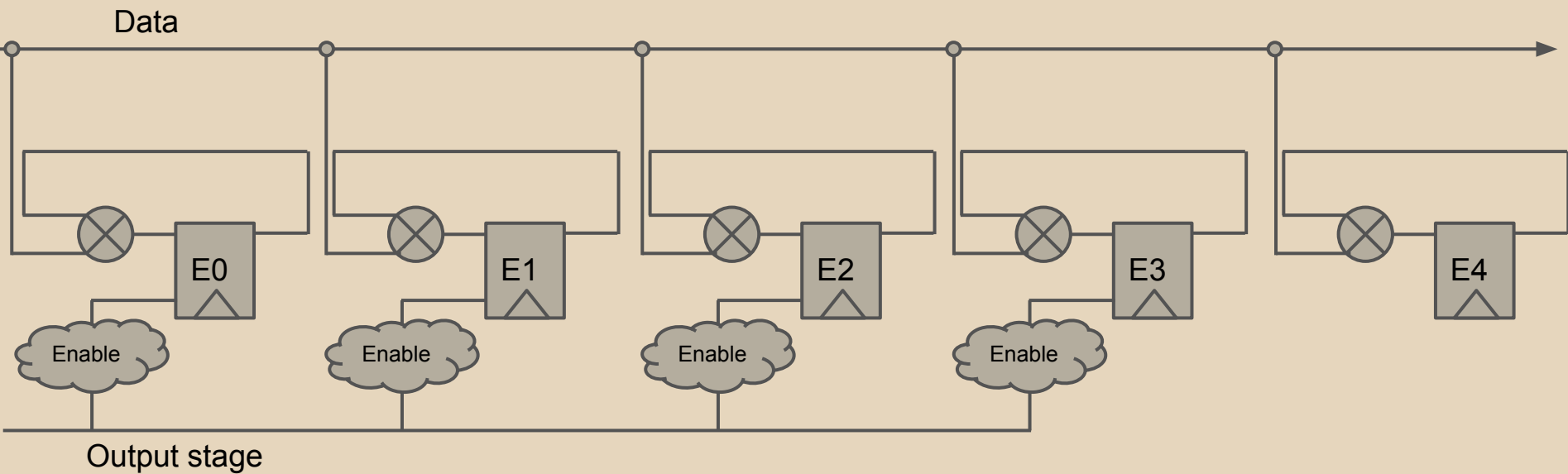
Data

Output stage

Output Multiplexer

- Selects what bit is sent
  - Voted data
  - System status
  - ECC

- Selected output is defined by current output stage

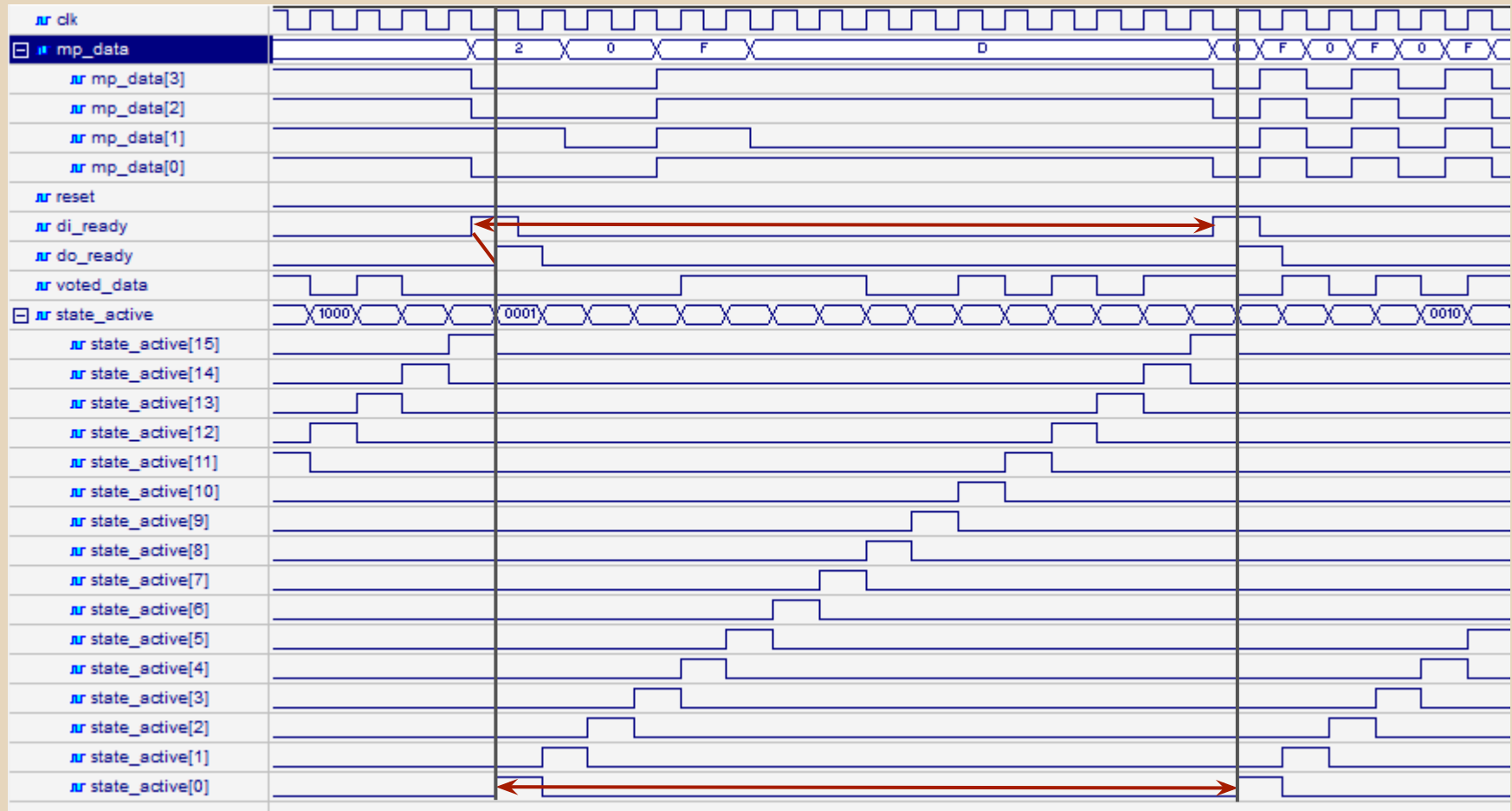- When ECC bit 4 is sent, it is XORed with the other ECC-bits

Area

- The circuit is realizable with 32 LUTs
  - Xilinx XST - 32 LUTs with area optimization
  - Synplify Pro - 37 LUTs with disabled sequential opt.

- Voting: 6 LUTs

- State maintenance w/o ECC: 4 LUTs

- ECC: 11 LUTs

- Output Multiplexing: 8 LUTs

- Status calculation: 3 LUTs

Verification

- Test bench
  - 7 tests for ordinary flow
  - 24 distinct corner cases
  - 16836 tests for all permutations fail states
    - All permutations of fail states
      - All 256 possible inputs (all MCUs agree)
        - Assures that each input is correct for any state.

- Test-driven development
  - Wrote a lot of tests, improved design until both LUT count was minimal and all tests were good

Timing

Questions?