Embedded Systems

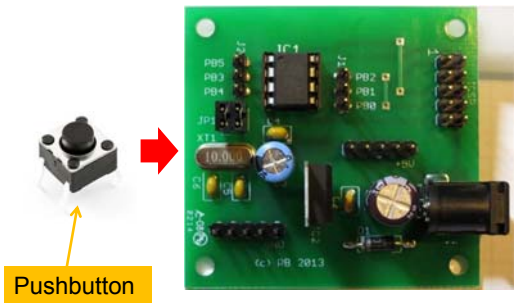
Lab 2

http://user.engineering.uiowa.edu/~rbeichel/lectures/es_s19/lab2/index.html

Note: each group will get one power shift register IC and one 7-segment display module from one of the TAs.

Lab 2 ("Hexadecimal Up/Down Counter") – Hardware and Software Considerations

- The user can control the counter by using one pushbutton
  →see website for a detailed description of required functionality and datasheets



TPIC6C595

LTS-4801JR

Pushbutton Switch

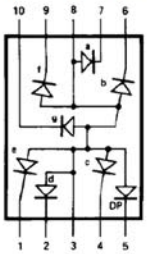
Power Logic 8-bit Shift Register (open drain NMOS FETs)

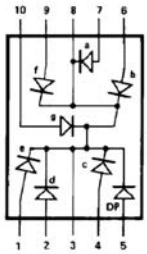
7-Segment LED Display

Consider I/O line constraints! → use internal RC oscillator!

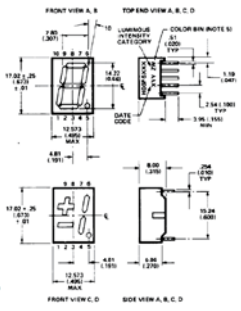
Seven-Segment & Other LED Displays

Internal Circuit Diagram





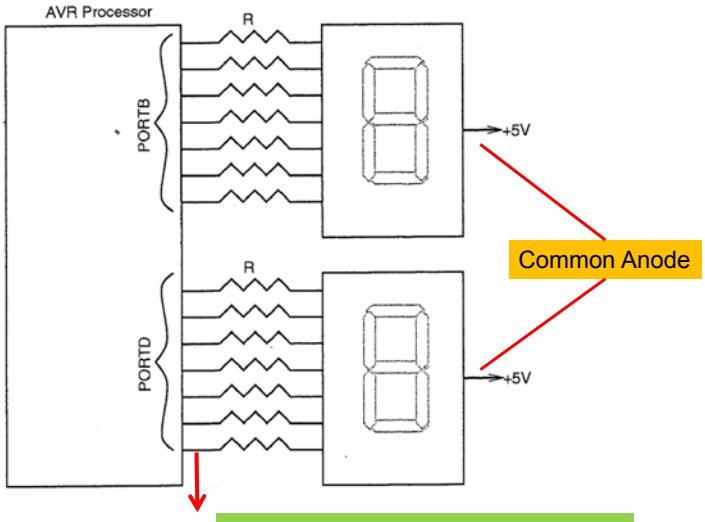
Package Dimensions



Common Anode

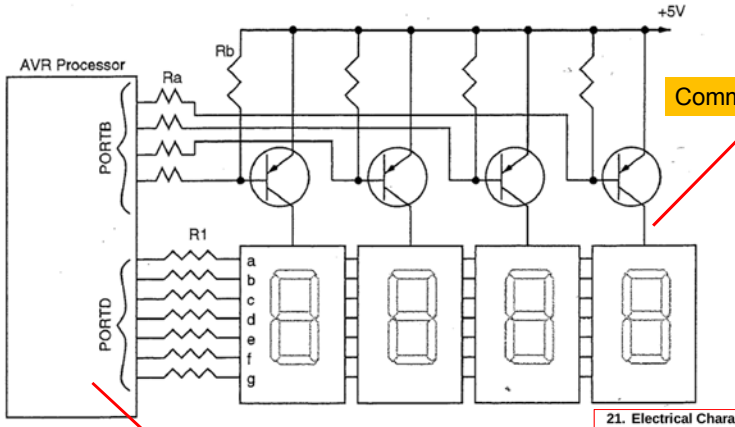
Common Cathode

Simple Seven-Segment LED Display Interface



Pull line low to activate LED segment

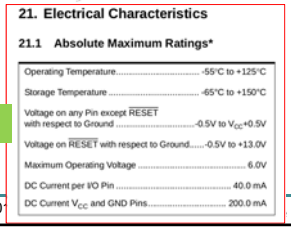
Multiplexed Seven Segment LED Display Interface



Common Anode

Consider current sink/source limitations!

ATtiny45 datasheet:



21. Electrical Characteristics

21.1 Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on any Pin except RESET with respect to Ground	-0.5V to V_{CC}+0.5V
Voltage on RESET with respect to Ground	-0.5V to +13.0V
Maximum Operating Voltage	6.0V
DC Current per I/O Pin	40.0 mA
DC Current V_{CC} and GND Pins	200.0 mA

Large Seven Segment LED Display

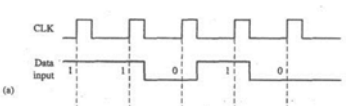
"Wall Clock"

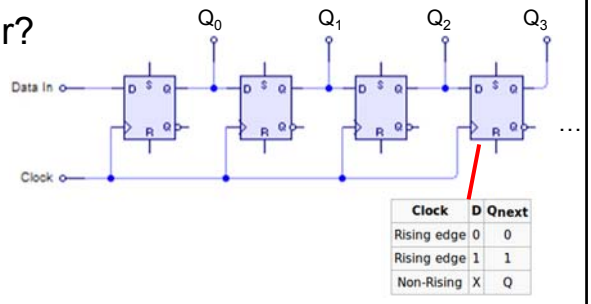
I/O Expansion

- Need more I/O lines/pins?
  → **(a)** use a different µC or **(b)** expand I/O using *shift registers*

What is a shift register?

D Flip-Flops are cascaded
Q to D and the clocks paralleled
to form a shift register





Clock	D	Qnext
Rising edge	0	0
Rising edge	1	1
Non-Rising	X	Q

Basic types of shift registers:

- **Serial-in/serial-out**
- **Parallel-in/serial-out** — Expand Input Lines
- **Serial-in/parallel-out** — Expand Output Lines
- **Ring**
- **…**

(b)

I/O Expansion using Shift Registers

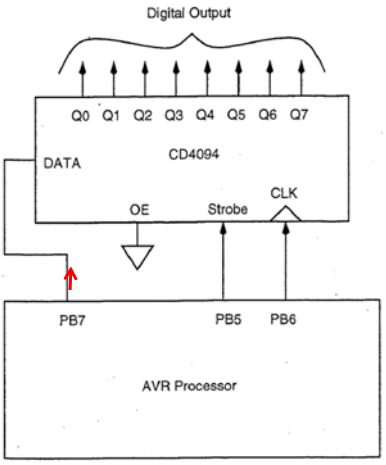


Figure 6.7 Eight-bit digital output port using a serial-in parallel-out shift register.

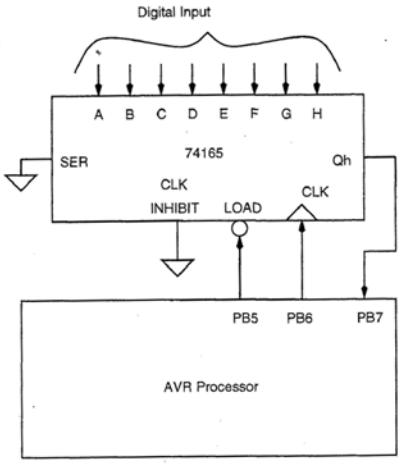
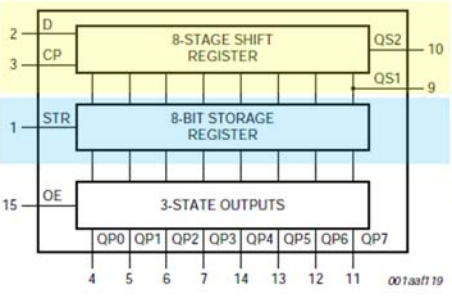
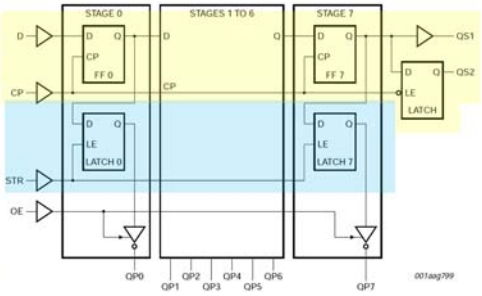


Figure 6.6 Eight-bit digital input port using a parallel-in serial-out shift register.

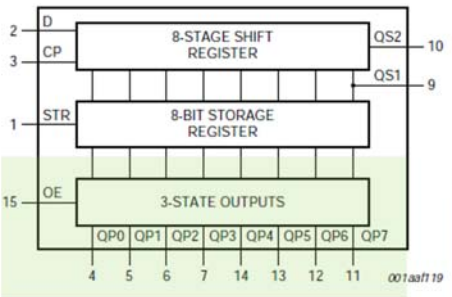
74HC4094

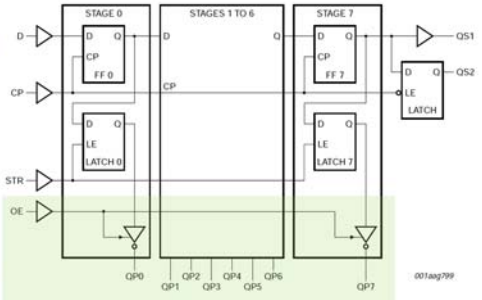




- The 74HC4094 is an 8-bit serial-in/serial- or parallel-out shift register with a storage register and 3-state outputs.
- Both the shift and storage **register** have separate clocks.
- The device features a serial input (D) and serial outputs to enable cascading.
- Data is shifted on the LOW-to-HIGH transitions of the CP input.
- The data in the shift register is transferred to the storage register when the STR input is HIGH.

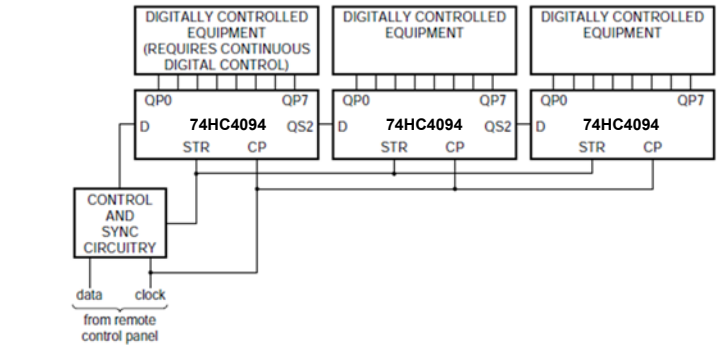
74HC4094





- Data in the storage register appears at the outputs whenever the output enable input (OE) is HIGH.
- A LOW on OE causes the outputs to assume a high-impedance OFF-state.
- Operation of the OE input does not affect the state of the registers.

74HC4094



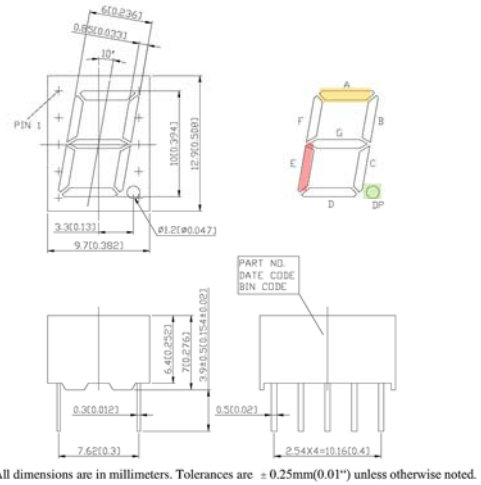
Remote control holding register

- The device features a serial input (D) and two serial outputs to enable cascading.

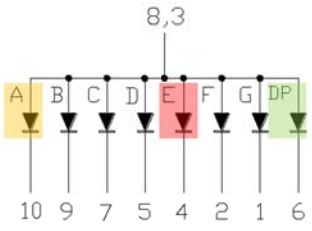
Seven Segment LED Display - LTS-4801JR

INTERNAL CIRCUIT DIAGRAM

PACKAGE DIMENSIONS



NOTES: All dimensions are in millimeters. Tolerances are ± 0.25mm(0.01") unless otherwise noted.



PIN CONNECTION

No	CONNECTION
1	CATHODE G
2	CATHODE F
3	COMMON ANODE
4	CATHODE E
5	CATHODE D
6	CATHODE D.P.
7	CATHODE C
8	COMMON ANODE
9	CATHODE B
10	CATHODE A

NOTE: PIN 3 & 8 ARE INTERNALLY CONNECTED.

LTS-4801JR

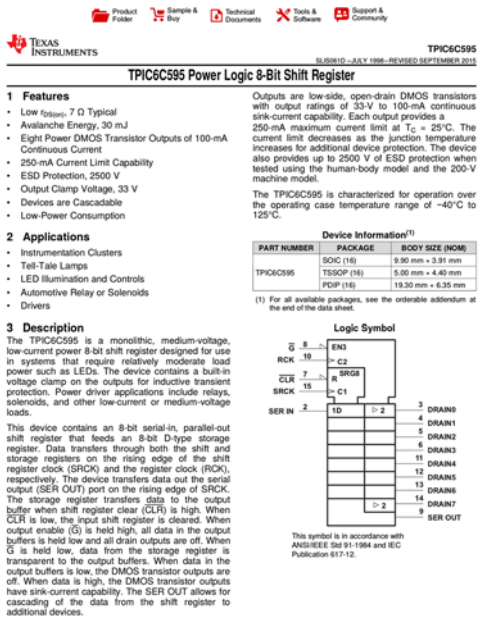
ABSOLUTE MAXIMUM RATING AT Ta=25°C

PARAMETER	MAXIMUM RATING	UNIT
Power Dissipation Per Segment	70	mW
Peak Forward Current Per Segment (1/10 Duty Cycle, 0.1ms Pulse Width)	90	mA
Continuous Forward Current Per Segment	25	mA
Derating Linear From 25°C Per Segment	0.33	mA/°C
Reverse Voltage Per Segment	5	V
Operating Temperature Range	-35°C to +85°C	
Storage Temperature Range	-35°C to +85°C	
Solder Temperature 1/16 inch Below Seating Plane for 3 Seconds at 260°C		

→ see datasheet for relation between I_F and V_F

TPIC6C595 – Datasheet

- **Can be found on class website**
- **Contains all relevant information for interfacing with the µC**
  - Voltage levels
  - Timing of signals
  - Pin function
  - Temperature range
  - Package (PDIP, SOIC, …)
  - Size
  - Ideas for application
  - …



Product Folder · Sample & Buy · Technical Documents · Tools & Software · Support & Community

TEXAS INSTRUMENTS — TPIC6C595

SLIS061D – JULY 1998 – REVISED SEPTEMBER 2015

TPIC6C595 Power Logic 8-Bit Shift Register

1 Features

- Low $r_{DS(on)}$, 7 Ω Typical
- Avalanche Energy, 30 mJ
- Eight Power DMOS Transistor Outputs of 100-mA Continuous Current
- 250-mA Current Limit Capability
- ESD Protection, 2500 V
- Output Clamp Voltage, 33 V
- Devices are Cascadable
- Low-Power Consumption

2 Applications

- Instrumentation Clusters
- Tell-Tale Lamps
- LED Illumination and Controls
- Automotive Relay or Solenoids
- Drivers

3 Description

The TPIC6C595 is a monolithic, medium-voltage, low-current power 8-bit shift register designed for use in systems that require relatively moderate load power such as LEDs. The device contains a built-in voltage clamp on the outputs for inductive transient protection. Power driver applications include relays, solenoids, and other low-current or medium-voltage loads.

This device contains an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. Data transfers through both the shift and storage registers on the rising edge of the shift register clock (SRCK) and the register clock (RCK), respectively. The device transfers data out the serial output (SER OUT) port on the rising edge of SRCK. The storage register transfers data to the output buffer when shift register clear ($\overline{CLR}$) is high. When $\overline{CLR}$ is low, the input shift register is cleared. When output enable ($\overline{G}$) is held high, all data in the output buffers is held low and all drain outputs are off. When $\overline{G}$ is held low, data from the storage register is transparent to the output buffers. When data in the output buffers is low, the DMOS transistor outputs are off. When data is high, the DMOS transistor outputs have sink-current capability. The SER OUT allows for cascading of the data from the shift register to additional devices.

Outputs are low-side, open-drain DMOS transistors with output ratings of 33-V to 100-mA continuous sink-current capability. Each output provides a 250-mA maximum current limit at T_C = 25°C. The current limit decreases as the junction temperature increases for additional device protection. The device also provides up to 2500 V of ESD protection when tested using the human-body model and the 200-V machine model.

The TPIC6C595 is characterized for operation over the operating case temperature range of −40°C to 125°C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPIC6C595	SOIC (16)	9.90 mm × 3.91 mm
	TSSOP (16)	5.00 mm × 4.40 mm
	PDIP (16)	19.30 mm × 6.35 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

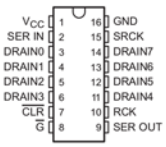
Logic Symbol

This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

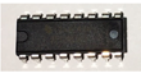
TPIC6C595 – Pin Functions

5 Pin Configuration and Functions

D, PW, or N Package
16-Pin SOIC, TSSOP, or PDIP
Top View



TPIC6C595



Pin Functions

PIN NAME	PIN NO.	I/O	DESCRIPTION
CLR	7	I	Shift register clear, active-low
DRAIN0	3	O	Open-drain output
DRAIN1	4	O	Open-drain output
DRAIN2	5	O	Open-drain output
DRAIN3	6	O	Open-drain output
DRAIN4	11	O	Open-drain output
DRAIN5	12	O	Open-drain output
DRAIN6	13	O	Open-drain output
DRAIN7	14	O	Open-drain output
G	8	I	Output enable, active-low
GND	16	—	Power ground
RCK	10	I	Register clock
SER IN	2	I	Serial data input
SER OUT	9	O	Serial data output
SRCK	15	I	Shift register clock
V_{CC}	1	I	Power supply

TPIC6C595 – Circuit Diagram & Connection to µC

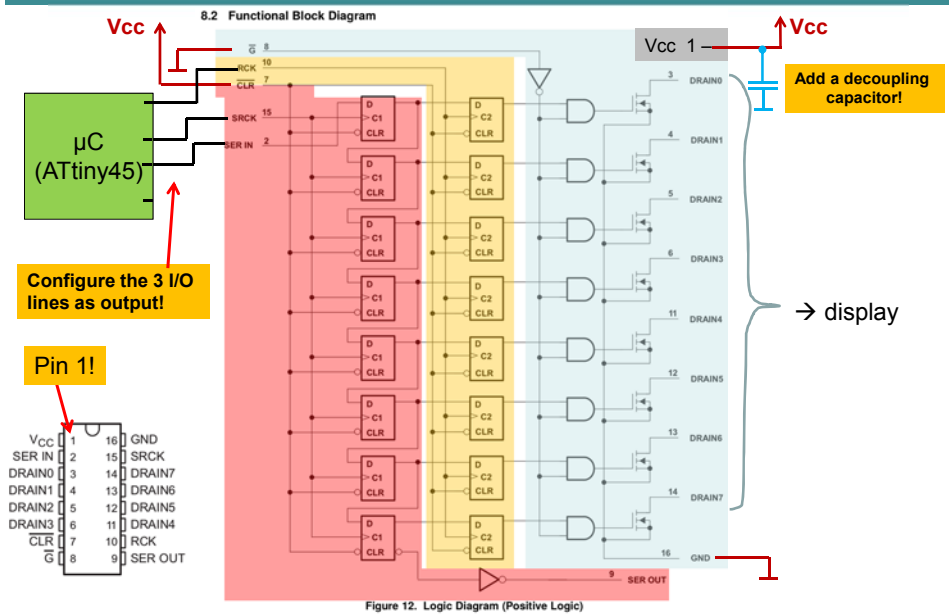
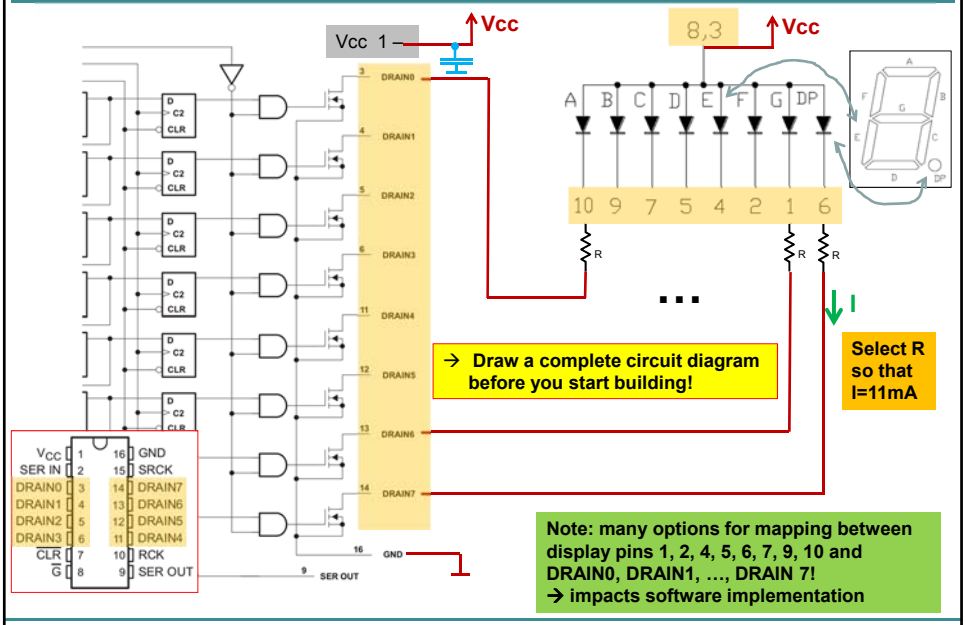


Figure 12. Logic Diagram (Positive Logic)

TPIC6C595 – Connection to 7-Segment LED Display



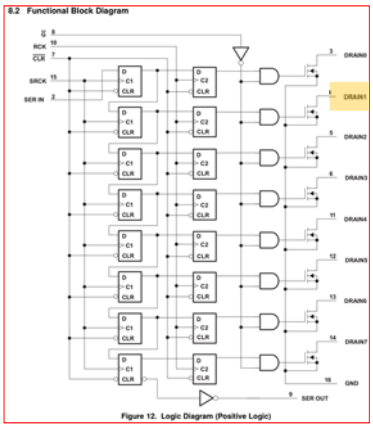
→ **Draw a complete circuit diagram before you start building!**

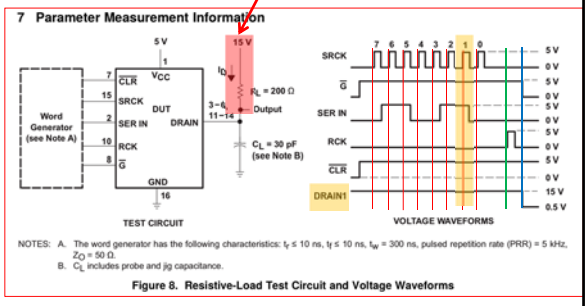
Select R so that I=11mA

Note: many options for mapping between display pins 1, 2, 4, 5, 6, 7, 9, 10 and DRAIN0, DRAIN1, …, DRAIN 7!
→ impacts software implementation

TPIC6C595 – Timing of Input Signals (General)

Needs a pull-up resistor or load to V+ for measuring the signal on DRAIN1!





Note: in this case V+ > Vcc
(→ open drain output)

TPIC6C595 – Timing of Input Signals (Our Use Case)

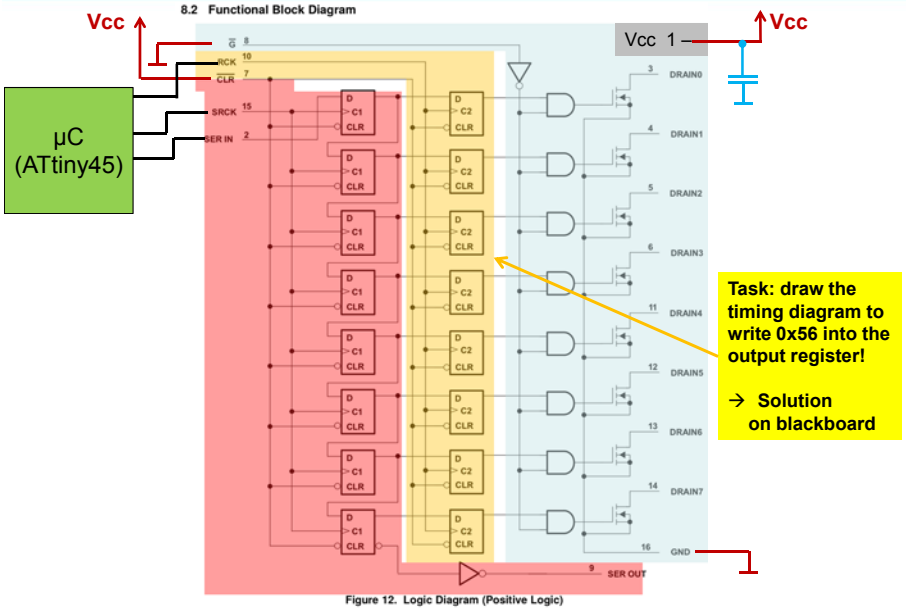


Figure 12. Logic Diagram (Positive Logic)

TPIC6C595 – Absolute Maximum Ratings

→Values of voltage, current, temperature, power dissipation etc., which should not be exceeded at any time → otherwise deterioration/destruction of the IC may take place

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
V_{CC}	Logic supply voltage (2)	–0.3	7	V
V_I	Logic input voltage	–0.3	7	V
V_{DS}	Power DMOS drain-to-source voltage (3)	–0.3	33	V
	Continuous source-to-drain diode anode current	0	250	mA
	Pulsed source-to-drain diode anode current (4)	0	500	mA
I_D	Pulsed drain current, each output, all outputs on, T_C = 25°C (4)	0	250	mA
I_D	Continuous drain current, each output, all outputs on, T_C = 25°C (4)	0	100	mA
I_{DM}	Peak drain current single output, T_C = 25°C (4)	0	250	mA
E_{AS}	Single-pulse avalanche energy (see Figure 11)	0	30	mJ
I_{AS}	Avalanche current (5)	0	200	mA
	Continuous total dissipation	See *Thermal Information*		
T_J	Operating virtual junction temperature	–40	150	°C
T_C	Operating case temperature	–40	125	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to GND.
(3) Each power DMOS source is internally connected to GND.
(4) Pulse duration ≤ 100 µs and duty cycle ≤ 2%.
(5) DRAIN supply voltage = 15 V, starting junction temperature (T_{JS}) = 25°C, L = 1.5 H, I_{AS} = 200 mA (see Figure 11).

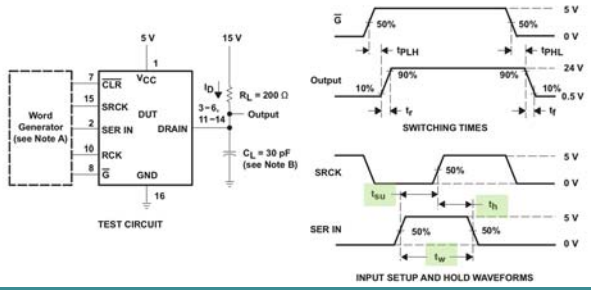
TPIC6C595 – Operating Conditions

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Logic supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	0.85 V_{CC}		V
V_{IL}	Low-level input voltage		0.15 V_{CC}	V
	Pulsed drain output current, T_C = 25°C, V_{CC} = 5 V, all outputs on (1) (2) (see Figure 7)		250	mA
t_{su}	Setup time, SER IN high before SRCKM ↑ (see Figure 9)	20		ns
t_h	Hold time, SER IN high after SRCKM ↑, (see Figure 9)	20		ns
t_w	Pulse duration (see Figure 9)	40		ns
T_C	Operating case temperature	–40	125	°C

(1) Pulse duration ≤ 100 µs and duty cycle ≤ 2%.
(2) Technique should limit $T_J - T_C$ to 10°C maximum.



AVR Subroutine for Displaying a Digit

- A (long) sequence of SBI and CBI instructions could be used to display a number on the 7-seg. display
- → Better approach: generate a general useable display subroutine

```
; put code here to configure I/O lines
; connected to TPIC6C595 as output
...

; start main program

...

; display a digit
ldi R16, 0x70 ; load pattern to display
rcall display ; call display subroutine

...
```

```
display:
   ; backup used registers on stack
   push R16
   push R17
   in R17, SREG
   push R17

   ldi R17, 8 ; loop --> test all 8 bits
loop:
   rol R16 ; rotate left trough Carry
   BRCS set_ser_in_1 ; branch if Carry set
   ; put code here to set SER_IN to 0
   ...
   rjmp end
set_ser_in_1:
   ; put code here to set SER_IN to 1
   ...
end:
    ; put code here to generate SRCK pulse
    ...

    dec R17
    brne loop

    ; put code here to generate RCK pulse
    ...

    ; restore registers from stack
    pop R17
    out SREG, R17
    pop R17
    pop R16

    ret
```

Example

Consider the following AVR program:

```
ldi R16, 0x00
out SREG, R16
ldi R16, 0xC3
rol R16
```

a) What will be the content of R16?

b) Which bits in SREG will be set to 1?

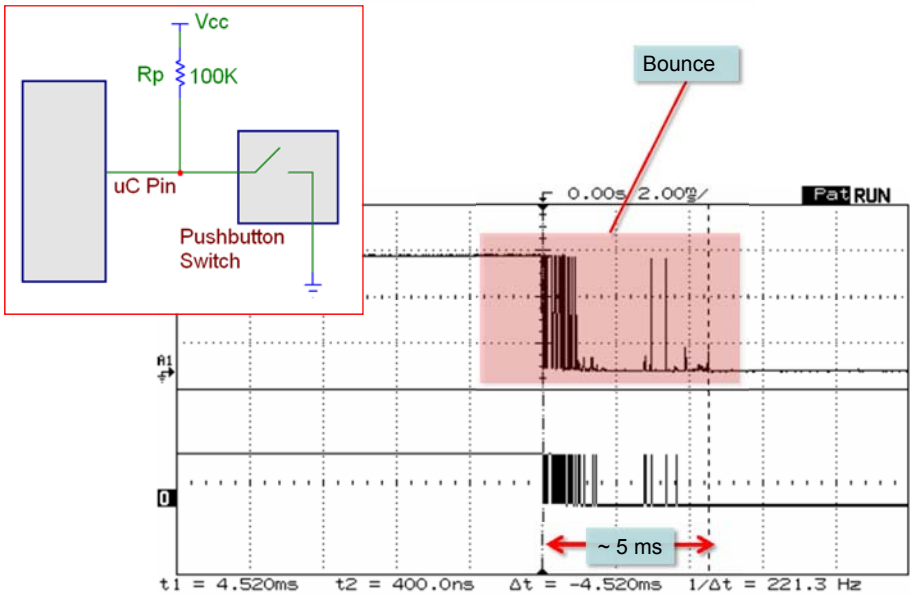
SREG – AVR Status Register

The AVR Status Register – SREG – is defined as:

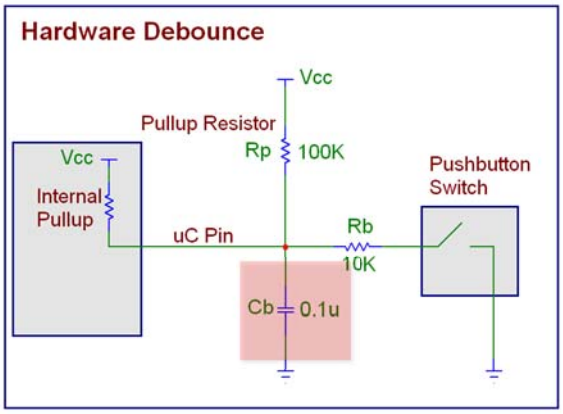
Bit	7	6	5	4	3	2	1	0	
0x3F	I	T	H	S	V	N	Z	C	SREG
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

→ **Solution on blackboard …**

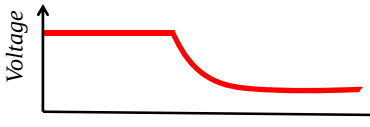
Switch Bounce and Debouncing



Switch Bounce and Debouncing



When the switch closes, the capacitor discharges through Rb



Question: what is the fall time?

Make sure you can calculate this.

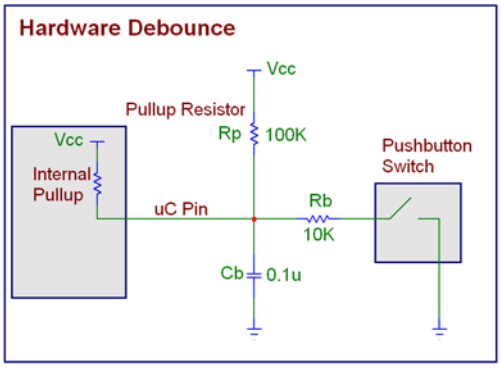
Software Debounce

One idea. Sample *n* times at regular intervals, say 10 ms apart. Count how many times the switch is zero. If this is larger than the number of times the switch is high, consider the switch pressed.

```
char isPressed(void)
{
  char ones=0, zeroes=0, i;

  for(i=0;i<=10-1;i++){
    if(PINA&0x01){ // read pin == 1
      ones++;
    } else {       // read pin == 0
      zeroes++;
    }
  _delay_ms(10);
  }
  return (ones > zeroes);
}
```

Testing Status of an I/O PIN




```
...
cbi  DDRB,0
cbi  DDRB,1
...
SBIS PINB,0
...
```

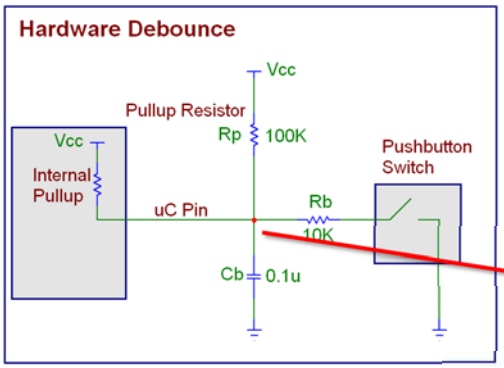
This instruction tests a single bit in an I/O register and skips the next instruction if the bit is set.

For input use **PINB**,not **PORTB**

```
...
cbi  DDRB,0
cbi  DDRB,1
...
SBIC PINB,0
...
```

Branch instruction:
SBIC (**S**kip next instruction if **B**it in **I**/O is **C**lear)

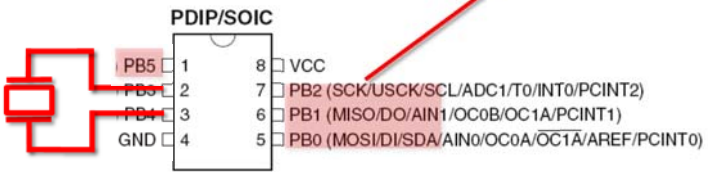
Which PIN to Use?



There are 5 PINs available for use as switch input: PB0, PB1, PB2, PB3 and PB4.

Which one should you use?

These are used by the programmer when it downloads code, so adding a debounce capacitor may interfere. You may have to experiment which PIN works best as an input pin.



… EOL