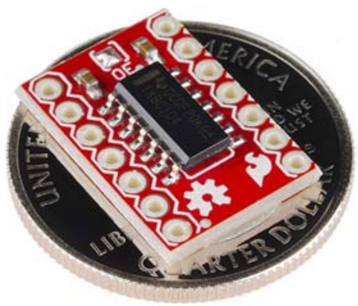
Embedded Systems

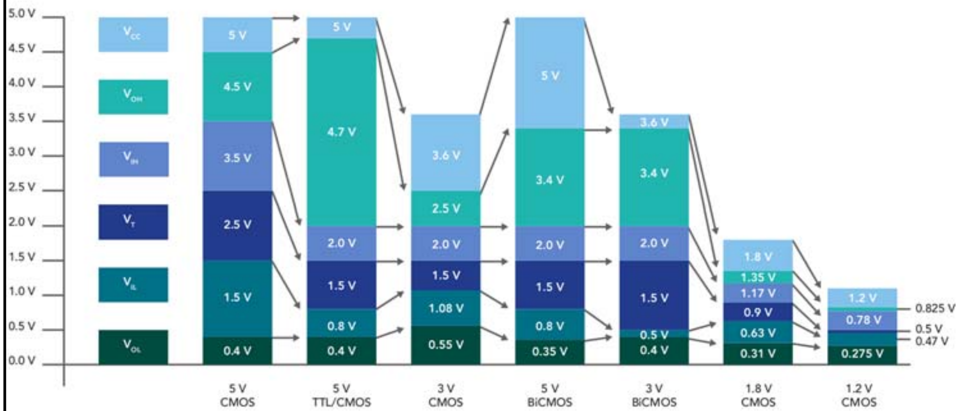
Interfacing 5V and sub-5V ICs



Low (<5V) Supply Voltage ICs

- **Driving factors:**
  - Ever increasing need for processing speed →reduction in size of transistors
  - Up-integration at cheaper cost → smaller geometries.
  - Reduction in power consumption (less heat, smaller battery size, …)
- **Reduced transistor size → reduction in the transistor breakdown voltage →reduction in supply voltage**
- **3.3V, 1.8V, or even 0.8V ICs**

Sub-5V CMOS



Mixed Voltage Systems

- **Ideal case: same supply voltage level for whole system (e.g., 3.3V)**
- **However, transition from 5V to sub-5V (e.g., 3.3V) systems is gradually → mixed design**
- **Issues to consider:**
  - **Translating analog signals across the 3.3V/5V or 5V/3.3V barrier (motivation on whiteboard!)**
  - **Potential logic level translation**
  - **Powering the 3.3V systems**

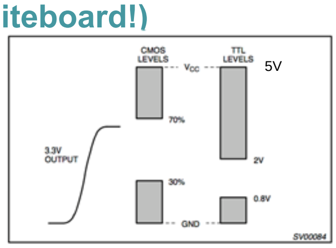


Figure 1. Switching Levels

Note that we assume a 3.3V supply for sub-5V system. However, most techniques work equally well for other supply voltages with the appropriate modifications.

Powering 3.3V Systems from 5V

- **The sub-5V system needs its own regulated power supply**
- **Several options including:**

Figure 2-1: Zener Supply

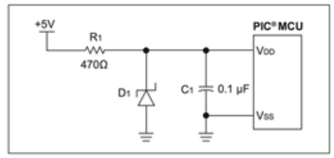
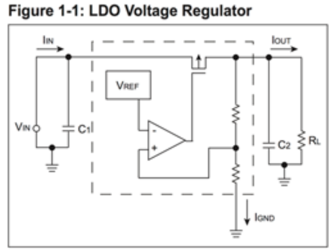


Figure 1-1: LDO Voltage Regulator



Example – Power Supply Comparison

Method	VREG	IQ	Eff.	Size	Cost	Transient Response
Zener Shun Reg.	10% Typ	5 mA	60%	Sm	Low	Poor
Series Linear Reg.	0.4% Typ	1 µA to 100 µA	60%	Sm	Med	Excellent
Switching Buck Reg.	0.4% Typ	30 µA to 2 mA	93%	Med to Lrg	High	Good

3.3V Output → 5V Input

- **Direct Connect:**
- **Works only if the following 2 requirements are met:**
  - **The V_{OH} of the 3.3V output is greater than the V_{IH} of the 5V input**
  - **The V_{OL} of the 3.3V output is less than the V_{IL} of the 5V input**
- **Example: interfacing a 3.3V LVCMOS output to a 5V TTL input**

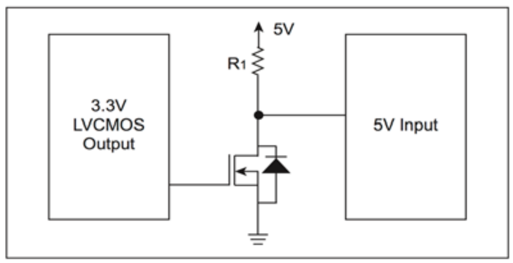
Input/Output Thresholds

	VOH min	VOL max	VIH min	VIL max
5V TTL	2.4V	0.5V	2.0V	0.8V
3.3V LVTTL	2.4V	0.4V	2.0V	0.8V
5V CMOS	4.7V (Vcc-0.3V)	0.5V	3.5V (0.7xVcc)	1.5V (0.3xVcc)
3.3V LVCMOS	3.0V (Vcc-0.3V)	0.5V	2.3V (0.7xVcc)	1.0V (0.3xVcc)

3.3V Output → 5V Input

- **MOSFET Translator:**
- **Works as an inverter!**
- **When selecting the value for R1, there are two parameters that need to be considered:**
  - the switching speed of the input and
  - the current consumption through R1

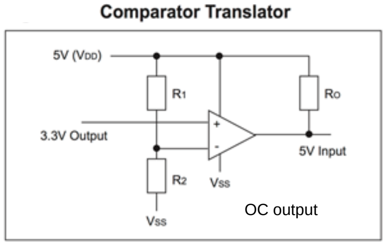
MOSFET Translator



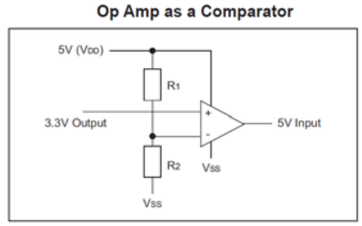
3.3V Output → 5V Input

- **Voltage Comparator:**
- **The basic operation of the comparator is as follows:**
  - When the voltage at the non-inverting (+) input is greater than that at the non-inverting (-) input, the output of the comparator is in a high state.
  - When the voltage at the inverting (-) input is greater than that at the non-inverting (+) input, the output of the comparator swings to Vss (low).
- **Allows to preserve polarity**

Comparator Translator



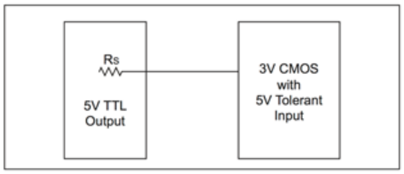
Op Amp as a Comparator



5V Output → 3.3V Input

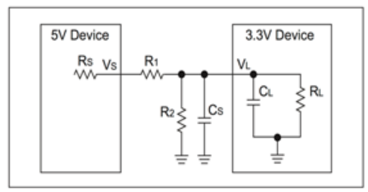
- **Typically, a direct connection is problematic in most cases (→ example on whiteboard)**
- **Some devices have 5V tolerant inputs:**

Figure 9-1: 5V Tolerant Input



- **Resistor divider:**
- There is a trade-off between:
  - power dissipation
  - and transition times

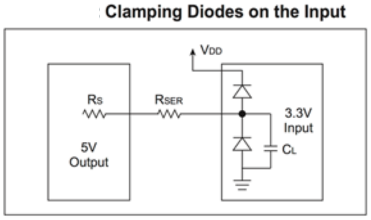
Resistive Interface Equivalent Circuit



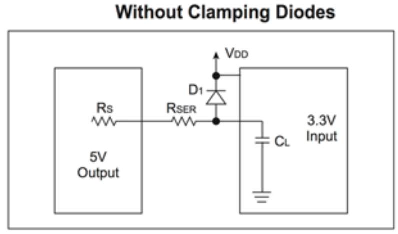
5V Output → 3.3V Input

- **More options:**

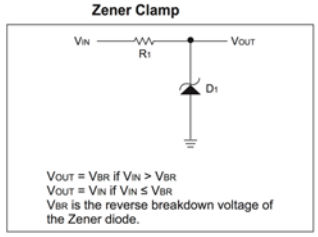
Clamping Diodes on the Input



Without Clamping Diodes

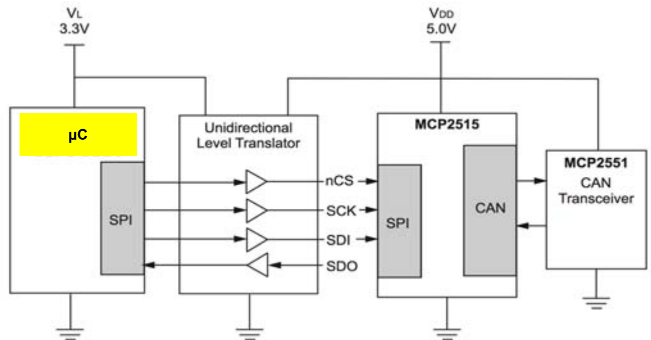


Zener Clamp



5V ← → 3.3V Conversion for SPI

- Communication between devices (e.g., MCU to peripheral) is most often done by either SPI or I2C.
- For SPI, it may be appropriate to use unidirectional level translators:



Note that translators for 3.3V to 5V and 5V to 3.3V are needed!

CMOS Voltage Level Shifter – Unidirectional

intersil

CD40109BMS

December 1992

CMOS Quad Low-to-High Voltage Level Shifter

Features

- High Voltage Type (20V Rating)
- Independence of Power Supply Sequence Considerations
  - VCC can Exceed VDD
  - Input Signals can Exceed Both VCC and VDD
- Up and Down Level Shifting Capability
- Three-State Outputs with Separate Enable Controls
- 100% Tested for Quiescent Current at 20V
- 5V, 10V and 15V Parametric Ratings
- Maximum Input Current of 1μA at 18V Over Full Package Temperature Range; 100nA at 18V and +25°C
- Noise Margin (Over Full Package/Temperature Range)
  - 1V at VCC = 5V, VDD = 10V
  - 2V at VCC = 10V, VDD = 15V
- Standardized Symmetrical Output Characteristics
- Meets All Requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications

- High or Low Level Shifting with Three-State Outputs for Unidirectional or Bidirectional Bussing
- Isolation of Logic Subsystems Using Separate Power Supplies from Supply Sequencing, Supply Loss and Supply Regulation Considerations

Description

CD40109BMS contains four low-to-high voltage level shifting circuits. Each circuit will shift a low voltage digital logic input signal (A, B, C, D) with logical 1 = VCC and logical 0 = VSS to a higher voltage output signal (E, F, G, H) with logical 1 = VDD and logical 0 = VSS.

The CD40109BMS, unlike other low-to-high level shifting circuits, does not require the presence of the high voltage supply (VDD) before the application of either the low voltage supply (VCC) or the input signals. There are no restrictions on the sequence of application of VDD, VCC, or the input signals. In addition, with one exception there are no restrictions on the relative magnitudes of the supply voltages or input signals within the device maximum ratings, provided that the input signal swings between VSS and at least 0.7VCC; VCC may exceed VDD, and input signals may exceed VCC and VDD. When operated in the mode VCC > VDD, the CD40109BMS will operate as a high-to-low level shifter.

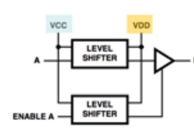
The CD40109BMS also features individual three-state output capability. A low level on any of the separately enabled three-state output controls produces a high impedance state in the corresponding output.

The CD40109BMS is supplied in these 16-lead outline packages:

Braze Seal DIP	H4T
Frit Seal DIP	H1E
Ceramic Flatpack	H6W

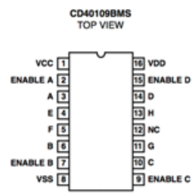
Functional Diagram

1 OF 4 UNITS



CMOS Voltage Level Shifter – Unidirectional

Pinout



Logic Diagram

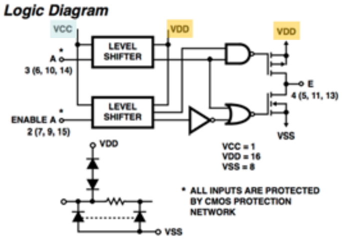


FIGURE 1. 1 OF 4 UNITS

TRUTH TABLE

INPUTS		OUTPUTS
A, B, C, D	ENABLE A, B, C, D	E, F, G, H
0	1	0
1	1	1
X	0	Z

Logic 0 = Low(VSS)
X = Don't care
Z = High impedance
Logic 1 = VCC at Inputs and VDD at Outputs

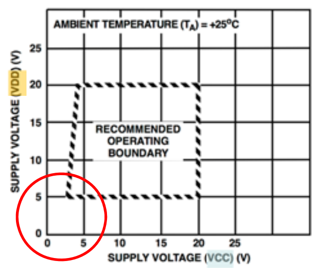
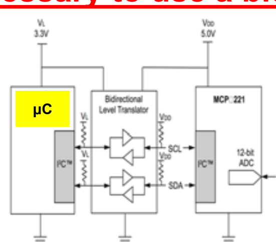


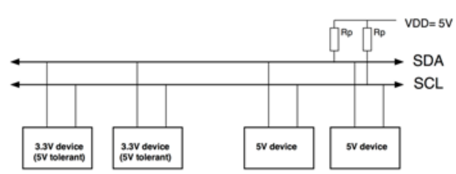
FIGURE 10. HIGH LEVEL SUPPLY VOLTAGE vs LOW LEVEL SUPPLY VOLTAGE

5V ← → 3.3V Conversion for I2C

- **Communication between devices (e.g., MCU to peripheral) is most often done by either SPI or I2C.**
- **For I2C, it is necessary to use a bidirectional solution:**

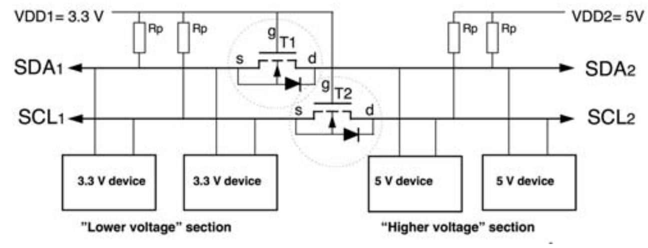


- **Some I2C ICs are 5V tolerant:**



5V ← → 3.3V Conversion for I2C

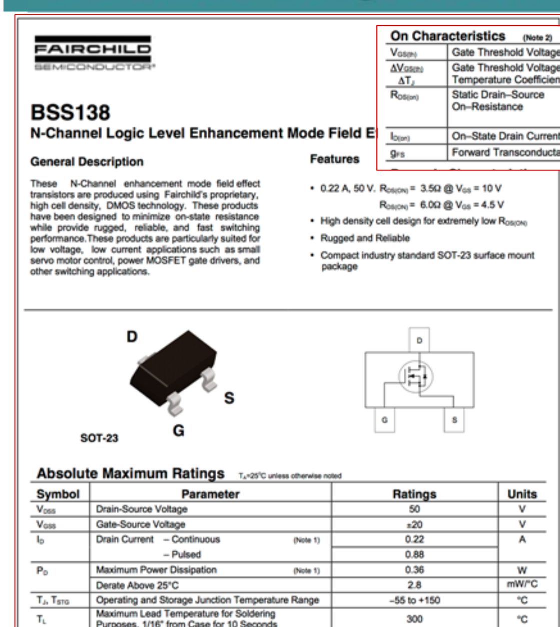
- **One option is to use suitable n-channel MOSFETs:**



- **Explanation on whiteboard!**
- **This approach can also be used for other applications than I2C (e.g., SPI, …)!**
- **MOSFET must have $V_{GS(th)}$ < VDD1 < VDD2**

TYPE	$V_{GS(th)}$	$R_{DS(on)}$	C_{iss}	Package
BSN10	min. 0.4V max. 1.8V	25 Ohm (typ)	15 pF	TO-92
BSN20	min. 0.4V max. 1.8V	25 Ohm (typ)	15 pF	SOT23
BSS83	min. 0.1V max. 2.0V	70 Ohm (typ)	1.5 pF (typ)	SOT143
BSS88	min. 0.4V max. 1.2V	15 Ohm	50 pF (typ)	TO-92

Bidirectional Voltage Level Converter with MOSFET



FAIRCHILD SEMICONDUCTOR®

BSS138

N-Channel Logic Level Enhancement Mode Field E

General Description

These N-Channel enhancement mode field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. These products have been designed to minimize on-state resistance while provide rugged, reliable, and fast switching performance.These products are particularly suited for low voltage, low current applications such as small servo motor control, power MOSFET gate drivers, and other switching applications.

Features

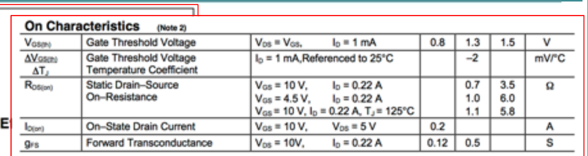
- 0.22 A, 50 V. $R_{DS(ON)}$ = 3.5Ω @ V_{GS} = 10 V
  $R_{DS(ON)}$ = 6.0Ω @ V_{GS} = 4.5 V
- High density cell design for extremely low $R_{DS(ON)}$
- Rugged and Reliable
- Compact industry standard SOT-23 surface mount package

D S G SOT-23

D G S

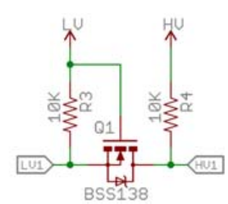
Absolute Maximum Ratings T_A=25°C unless otherwise noted

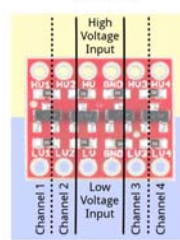
Symbol	Parameter	Ratings	Units
V_{DSS}	Drain-Source Voltage	50	V
V_{GSS}	Gate-Source Voltage	±20	V
I_D	Drain Current – Continuous (Note 1)	0.22	A
	– Pulsed	0.88	
P_D	Maximum Power Dissipation (Note 1)	0.36	W
	Derate Above 25°C	2.8	mW/°C
T_J, T_{STG}	Operating and Storage Junction Temperature Range	–55 to +150	°C
T_L	Maximum Lead Temperature for Soldering Purposes, 1/16" from Case for 10 Seconds	300	°C



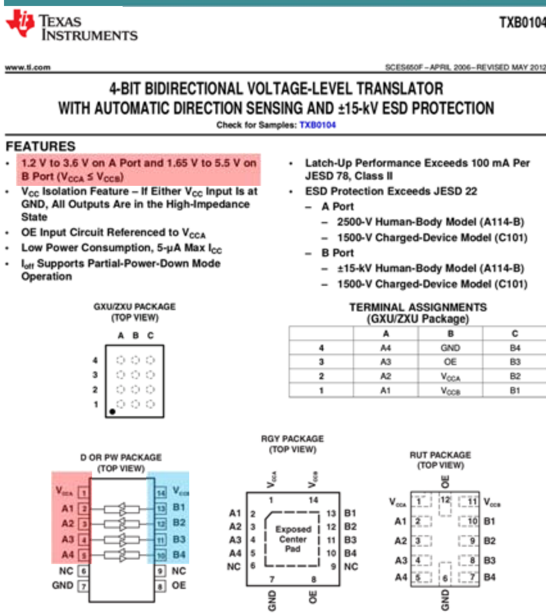
On Characteristics (Note 2)

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, I_D = 1 mA	0.8	1.3	1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	I_D = 1 mA,Referenced to 25°C		–2		mV/°C
$R_{DS(on)}$	Static Drain–Source On–Resistance	V_{GS} = 10 V, I_D = 0.22 A V_{GS} = 4.5 V, I_D = 0.22 A V_{GS} = 10 V, I_D = 0.22 A, T_J = 125°C		0.7 1.0 1.1	3.5 6.0 5.8	Ω
$I_{D(on)}$	On–State Drain Current	V_{GS} = 10 V, V_{DS} = 5 V	0.2			A
g_{FS}	Forward Transconductance	V_{DS} = 10V, I_D = 0.22 A	0.12	0.5		S





Bidirectional Voltage Level Converter IC


TEXAS INSTRUMENTS TXB0104

www.ti.com SCES650F – APRIL 2006 – REVISED MAY 2012

4-BIT BIDIRECTIONAL VOLTAGE-LEVEL TRANSLATOR
WITH AUTOMATIC DIRECTION SENSING AND ±15-kV ESD PROTECTION

Check for Samples: TXB0104

FEATURES

- 1.2 V to 3.6 V on A Port and 1.65 V to 5.5 V on B Port ($V_{CCA} \le V_{CCB}$)
- V_{CC} Isolation Feature – If Either V_{CC} Input Is at GND, All Outputs Are in the High-Impedance State
- OE Input Circuit Referenced to V_{CCA}
- Low Power Consumption, 5-µA Max I_{CC}
- I_{off} Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - A Port
    - 2500-V Human-Body Model (A114-B)
    - 1500-V Charged-Device Model (C101)
  - B Port
    - ±15-kV Human-Body Model (A114-B)
    - 1500-V Charged-Device Model (C101)

GXU/ZXU PACKAGE (TOP VIEW)

TERMINAL ASSIGNMENTS (GXU/ZXU Package)

	A	B	C
4	A4	GND	B4
3	A3	OE	B3
2	A2	V_{CCA}	B2
1	A1	V_{CCB}	B1

D OR PW PACKAGE (TOP VIEW)

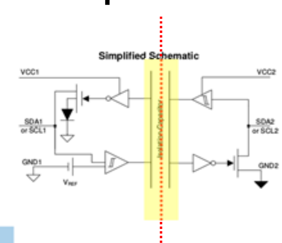
RGY PACKAGE (TOP VIEW)

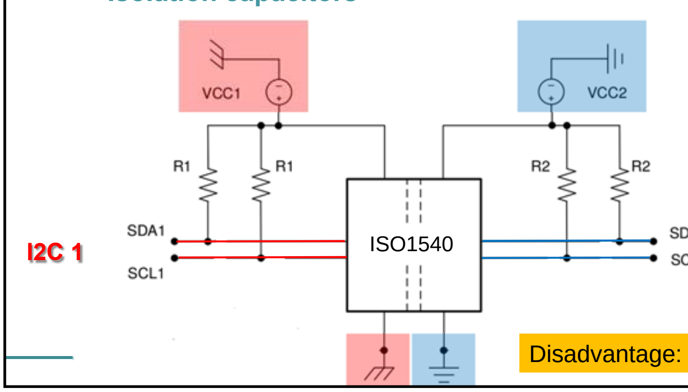
RUT PACKAGE (TOP VIEW)

~$1.30

Bidirectional I2C Isolators

- Enables isolated, bidirectional, and I2C-compatible communication between devices
- Also enables I2C level shifting
- Can be implemented with:
  - Optocouplers
  - Isolation capacitors





V_{CC1} range: 3 - 5.5 V
V_{CC2} range: 3 - 5.5 V

Disadvantage: expensive (~$5)

Discussion – Mixed Voltage Design

Email: "We are planning on using the Atmega88 development board to verify communication with an accelerometer and test our code.

The accelerometer we plan on using is powered with a 3.3v supply. To communicate between the micro-controller and the sensor we want to operate the micro-controller on 3.3V to make this issue easier to handle. However, the way we want to verify that our accelerometer is doing what we wish is through a RS232 serial output.

The MAX232 IC is supplied from 5V and if we wanted to use the ATmega88 development board's 3.3V regulator we would need to replace that component to a MAX3232 in order to use the RS232 serial output. The ESC shop does not sell this component, and it might be too late in the game to order this through Digit-Key because we wouldn't receive the component until late this week and we want to start developing software now.

Do you have and suggestions for us on how to communicate with micro-controller and how we can go about verifying that the accelerometer is working the way we want?"

… EOL