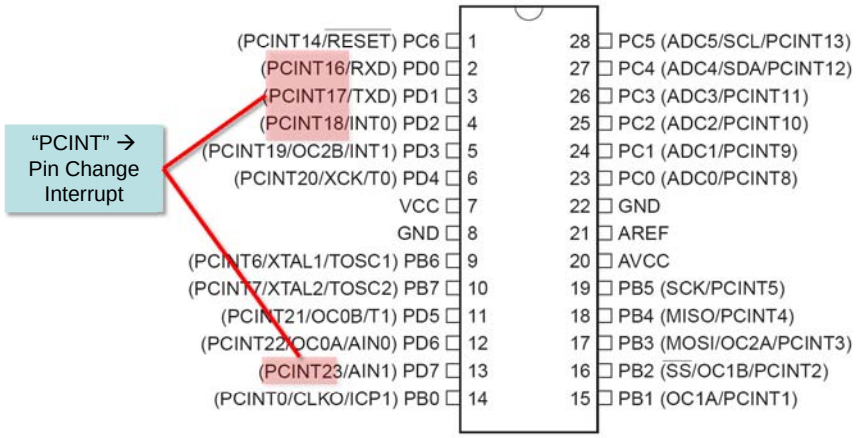
Embedded Systems

Lecture 11 Interrupts

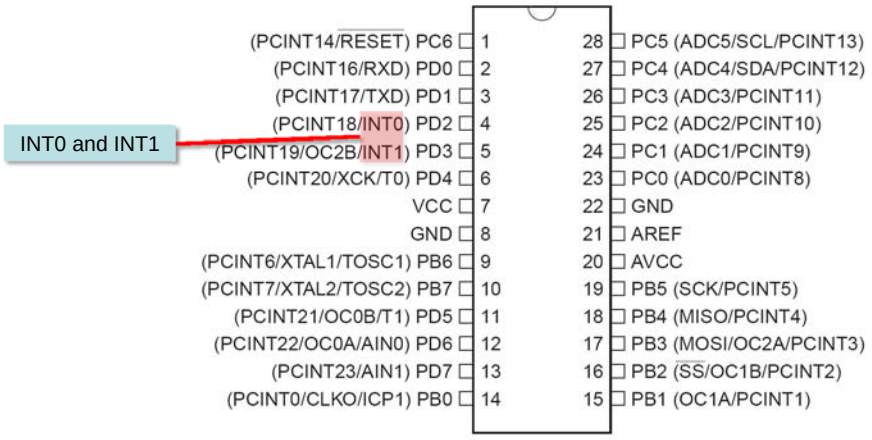
Interrupts

- One way to think of interrupts is that they are hardware-generated function calls
- Internal Hardware
  - When timer rolls over, then call a routine that blinks an LED
  - When built-in A/D converter is done converting, call a routine that manipulates the result
- External Hardware
  - When the voltage level on a I/O pin changes, call a routine that turns a motor
  - When the USART (Universal Synchronous Asynchronous Receiver Transmitter) receives a bit, call a routine that stores the bit, etc.
- The routines that are called when an interrupt occurs are called ***Interrupt Service Routine*s (ISRs)**

External Interrupts on ATmega88PA



External Interrupts on ATmega88PA



INT0 and INT1 interrupts can be triggered by a falling or rising edge or a low level. This is set up in the External Interrupt Control Register A – EICRA. When the INT0 or INT1 interrupts are enabled and are configured as level triggered, the interrupts will trigger as long as the pin is held low. Some interrupts are detected asynchronously. This implies that this interrupt can also be used for waking the part from sleep modes other than Idle mode.

External Interrupts on ATmega88PA

10.1 Sleep Modes

Figure 9-1 on page 26 presents the different clock systems in the ATmega48A/PA/88A/PA/168A/PA/328/P, and their distribution. The figure is helpful in selecting an appropriate sleep mode. Table 10-1 shows the different sleep modes, their wake up sources BOD disable ability.(1)

Note: 1. BOD disable is only available for ATmega48PA/88PA/168PA/328P.

Table 10-1. Active Clock Domains and Wake-up Sources in the Different Sleep Modes.

	Active Clock Domains					Oscillators		Wake-up Sources							
Sleep Mode	clk_{CPU}	clk_{FLASH}	clk_{IO}	clk_{ADC}	clk_{ASY}	Main Clock Source Enabled	Timer Oscillator Enabled	INT1, INT0 and Pin Change	TWI Address Match	Timer2	SPM/EEPROM Ready	ADC	WDT	Other I/O	Software BOD Disable
Idle			X	X	X	X	X(2)	X	X	X	X	X	X	X	
ADC Noise Reduction				X	X	X	X(2)	X(3)	X	X(2)	X	X	X		
Power-down								X(3)	X				X		X
Power-save					X		X(2)	X(3)	X	X			X		X
Standby(1)						X		X(3)	X				X		X
Extended Standby					X(2)	X	X(2)	X(3)	X	X			X		X

Notes: 1. Only recommended with external crystal or resonator selected as clock source.
2. If Timer/Counter2 is running in asynchronous mode.
3. For INT1 and INT0, only level interrupt.

Table 11-2. Reset and Interrupt Vectors in ATmega88PA

Vector No.	Program Address(2)	Source	Interrupt Definition
1	0x000(1)	RESET	External Pin, Power-on Reset, Brown-out Reset and Watchdog System Reset
2	0x001	INT0	External Interrupt Request 0
3	0x002	INT1	External Interrupt Request 1
4	0x003	PCINT0	Pin Change Interrupt Request 0
5	0x004	PCINT1	Pin Change Interrupt Request 1
6	0x005	PCINT2	Pin Change Interrupt Request 2
7	0x006	WDT	Watchdog Time-out Interrupt
8	0x007	TIMER2 COMPA	Timer/Counter2 Compare Match A
9	0x008	TIMER2 COMPB	Timer/Counter2 Compare Match B
10	0x009	TIMER2 OVF	Timer/Counter2 Overflow
11	0x00A	TIMER1 CAPT	Timer/Counter1 Capture Event
12	0x00B	TIMER1 COMPA	Timer/Counter1 Compare Match A
13	0x00C	TIMER1 COMPB	Timer/Coutner1 Compare Match B
14	0x00D	TIMER1 OVF	Timer/Counter1 Overflow

15	0x00E	TIMER0 COMPA	Timer/Counter0 Compare Match A
16	0x00F	TIMER0 COMPB	Timer/Counter0 Compare Match B
17	0x010	TIMER0 OVF	Timer/Counter0 Overflow
18	0x011	SPI, STC	SPI Serial Transfer Complete
19	0x012	USART, RX	USART Rx Complete
20	0x013	USART, UDRE	USART, Data Register Empty
21	0x014	USART, TX	USART, Tx Complete
22	0x015	ADC	ADC Conversion Complete
23	0x016	EE READY	EEPROM Ready
24	0x017	ANALOG COMP	Analog Comparator
25	0x018	TWI	2-wire Serial Interface
26	0x019	SPM READY	Store Program Memory Ready

Interrupt - Priority

The interrupts have priority in accordance with their Interrupt Vector position.
→ The lower the Interrupt Vector address, the higher the priority.

Table 11-2. Reset and Interrupt Vectors in ATmega88PA

Vector No.	Program Address(2)	Source	Interrupt Definition
1	0x000(1)	RESET	External Pin, Power-on Reset, Brown-out Reset and Watchdog System Reset
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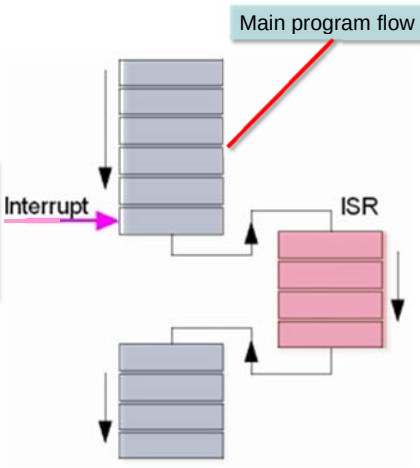
4	0x003	PCINT0	Pin Change Interrupt Request 0
5	0x004	PCINT1	Pin Change Interrupt Request 1
6	0x005	PCINT2	Pin Change Interrupt Request 2
7	0x006	WDT	Watchdog Time-out Interrupt
8	0x007	TIMER2 COMPA	Timer/Counter2 Compare Match A
9	0x008	TIMER2 COMPB	Timer/Counter2 Compare Match B
10	0x009	TIMER2 OVF	Timer/Counter2 Overflow
11	0x00A	TIMER1 CAPT	Timer/Counter1 Capture Event
12	0x00B	TIMER1 COMPA	Timer/Counter1 Compare Match A
13	0x00C	TIMER1 COMPB	Timer/Coutner1 Compare Match B
14	0x00D	TIMER1 OVF	Timer/Counter1 Overflow
15	0x00E	TIMER0 COMPA	Timer/Counter0 Compare Match A
16	0x00F	TIMER0 COMPB	Timer/Counter0 Compare Match B
17	0x010	TIMER0 OVF	Timer/Counter0 Overflow
18	0x011	SPI, STC	SPI Serial Transfer Complete
19	0x012	USART, RX	USART Rx Complete
20	0x013	USART, UDRE	USART, Data Register Empty
21	0x014	USART, TX	USART, Tx Complete
22	0x015	ADC	ADC Conversion Complete
23	0x016	EE READY	EEPROM Ready
24	0x017	ANALOG COMP	Analog Comparator
25	0x018	TWI	2-wire Serial Interface
26	0x019	SPM READY	Store Program Memory Ready

Interrupts Concepts



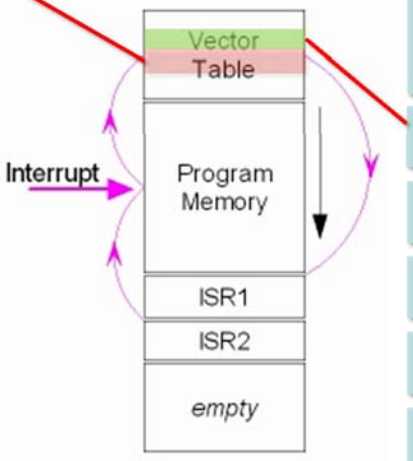
Generally, ISR should be fast – do one simple task as fast as possible.

ISRs should do their work transparently to the main program flow

See www.avrtutor.com/tutorial/interrupt/interrupts.php

Interrupts Concepts

One-instruction slot for INT1



Starting at program address 0x0000, there are predefined locations where different ISR start executing

For example, INT0's ISR starts execution at 0x0001

And the ISR for INT1 starts execution at 0x0002

Note: there is room for **only one** instruction for every ISR.

Thus, there should be an **rjmp** to the rest of the ISR code

Hence the name: ***vector tabl***e, or sometimes ***jump table.***

See www.avrtutor.com/tutorial/interrupt/interrupts.php

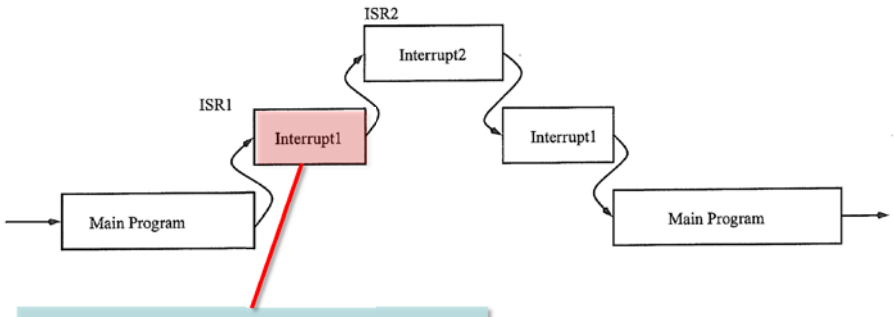
Nested Interrupts

When an ISR is invoked, the interrupts are turned off globally, i.e., there is an implied **cli.**

The **reti** instruction turn on interrupts globally.

Thus, normally, an ISR will not be interrupted by other ISRs.

However:



If this ISR enables interrupts (**sei** instruction), then other ISRs can interrupt it.

Writing an ISR

Writing an ISR is similar to writing a normal function: create a label, save registers (including SREG!) as needed, perform the task at hand (toggle bits, etc.).

When done, clean up and return.

When an event triggers the ISR, the return address is pushed onto the stack, the **PC** is loaded with the ISR address and execution continues.

ISRs should end with the RETI instruction. This pops the return address off the stack and load the PC, and execution continues with the next instruction

Example:

```
            ...
extint:     push    r0      ; Save r0 on the Stack
            ...
            pop     r0      ; Restore r0
            reti            ; Return and enable interrupts
```

RETI – Return from Interrupt

Returns from interrupt. The return address is loaded from the STACK and the Global Interrupt Flag is set.

Note that the Status Register (SREG) is not automatically stored when entering an interrupt routine, and it is not restored when returning from an interrupt routine. This must be handled by the application program. The Stack Pointer uses a pre-increment scheme during RETI.

Example:

```
            ...
extint:     push    r0      ; Save r0 on the Stack
            ...
            pop     r0      ; Restore r0
            reti            ; Return and enable interrupts
```


ISR Activation

Assume that the AVR had been configured so that Timer 0 ISR is activated when Timer 0 rolls over

Assume the main program is running and the counter is incrementing.

Main Program

```
…
                …
                sei  ; Enable interrupts
                …
0x0102          ldi   r30,LOW(2*msg)
0x0103          ldi   r31,HIGH(2*msg)
            L20:
0x0105          lpm   r2,Z+
0x0106          tst   r2
0x0107          breq  done
…               …
0x011A          rjmp  L20
            done:
…               …
```

PC = 0x0105

Timer 0 Overflow ISR

```
tim0_ovf:
0x0122 sbi PINC,1
0x0123 reti
```

Stack

Note: for simplicity the ISR does not show all the required house-keeping: saving SREG etc.

ISR Activation

Assume that the AVR had been configured so that Timer 0 ISR is activated when Timer 0 rolls over

Assume the main program is running and the counter is incrementing.

Main Program

```
…
                …
                sei  ; Enable interrupts
                …
0x0102          ldi   r30,LOW(2*msg)
0x0103          ldi   r31,HIGH(2*msg)
             L20:
0x0105          lpm   r2,Z+
0x0106          tst   r2
0x0107          breq  done
…               …
0x011A          rjmp  L20
             done:
…               …
```

Timer 0 Overflow ISR

```
tim0_ovf:
0x0122 sbi PINC,1
0x0123 reti
```

Stack

PC = 0x0106

Note: for simplicity the ISR does not show all the required house-keeping: saving SREG etc.

ISR Activation

Assume that the AVR had been configured so that Timer 0 ISR is activated when Timer 0 rolls over

Assume the main program is running and the counter is incrementing.

Main Program

```
…
                …
                sei  ; Enable interrupts
                …
0x0102          ldi   r30,LOW(2*msg)
0x0103          ldi   r31,HIGH(2*msg)
             L20:
0x0105          lpm   r2,Z+
0x0106          tst   r2
0x0107          breq  done
…               …
0x011A          rjmp  L20
             done:
…               …
```

Timer 0 Overflow ISR

```
tim0_ovf:
0x0122 sbi PINC,1
0x0123 reti
```

Stack

PC = 0x0106

Timer 0 Roll Over

Note: for simplicity the ISR does not show all the required house-keeping: saving SREG etc.

ISR Activation

Assume that the AVR had been configured so that Timer 0 ISR is activated when Timer 0 rolls over

Assume the main program is running and the counter is incrementing.

Main Program

```
…
                …
                sei  ; Enable interrupts
                …
0x0102          ldi   r30,LOW(2*msg)
0x0103          ldi   r31,HIGH(2*msg)
            L20:
0x0105          lpm   r2,Z+
0x0106          tst   r2
0x0107          breq  done
…               …
0x011A          rjmp  L20
            done:
…               …
```

Timer 0 Overflow ISR

```
tim0_ovf:
0x0122 sbi PINC,1
0x0123 reti
```

Stack

```
0x01
0x07
```

PC = 0x0106

Note: for simplicity the ISR does not show all the required house-keeping: saving SREG etc.

ISR Activation

Assume that the AVR had been configured so that Timer 0 ISR is activated when Timer 0 rolls over

Assume the main program is running and the counter is incrementing.

Main Program

```
…
                …
                sei  ; Enable interrupts
                …
0x0102          ldi   r30,LOW(2*msg)
0x0103          ldi   r31,HIGH(2*msg)
            L20:
0x0105          lpm   r2,Z+
0x0106          tst   r2
0x0107          breq  done
…               …
0x011A          rjmp  L20
            done:
…               …
```

Timer 0 Overflow ISR

```
tim0_ovf:
0x0122 sbi PINC,1
0x0123 reti
```

Stack

```
0x01
0x07
```

PC = 0x0122

Note: for simplicity the ISR does not show all the required house-keeping: saving SREG etc.

ISR Activation

Assume that the AVR had been configured so that Timer 0 ISR is activated when Timer 0 rolls over

Assume the main program is running and the counter is incrementing.

Main Program

```
…
                    …
                    sei  ; Enable interrupts
                    …
0x0102              ldi   r30,LOW(2*msg)
0x0103              ldi   r31,HIGH(2*msg)
                L20:
0x0105              lpm   r2,Z+
0x0106              tst   r2
0x0107              breq  done
…                   …
0x011A              rjmp  L20
                done:
…                   …
```

Timer 0 Overflow ISR

```
tim0_ovf:
0x0122 sbi PINC,1
0x0123 reti
```

Stack

```
0x01
0x07
```

PC = 0x0123

Note: for simplicity the ISR does not show all the required house-keeping: saving SREG etc.

ISR Activation

Assume that the AVR had been configured so that Timer 0 ISR is activated when Timer 0 rolls over

Assume the main program is running and the counter is incrementing.

Main Program

```
…
                    …
                    sei  ; Enable interrupts
                    …
0x0102              ldi   r30,LOW(2*msg)
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                L20:
0x0105              lpm   r2,Z+
0x0106              tst   r2
0x0107              breq  done
…                   …
0x011A              rjmp  L20
                done:
…                   …
```

Timer 0 Overflow ISR

```
tim0_ovf:
0x0122 sbi PINC,1
0x0123 reti
```

Stack

PC = 0x0107

Note: for simplicity the ISR does not show all the required house-keeping: saving SREG etc.

ISR Activation

Assume that the AVR had been configured so that Timer 0 ISR is activated when Timer 0 rolls over

Assume the main program is running and the counter is incrementing.

Main Program

```
…
                …
                sei  ; Enable interrupts
                …
0x0102          ldi   r30,LOW(2*msg)
0x0103          ldi   r31,HIGH(2*msg)
             L20:
0x0105          lpm   r2,Z+
0x0106          tst   r2
0x0107          breq  done
…               …
0x011A          rjmp  L20
             done:
…               …
```

Timer 0 Overflow ISR

```
tim0_ovf:
0x0122 sbi PINC,1
0x0123 reti
```

Stack

PC = 0x0107

Note: for simplicity the ISR does not show all the required house-keeping: saving SREG etc.

Interrupt-Driven Programming

In some programs, the main program configures the controller and interrupts, and then enters the main loop that does nothing. The real work is done by the ISR(s) when it/they is/are triggered

```
Interrupt [EXT_INT0] void ext_int_isr(void)
{
   PORTC = PORTC ^ 0x01;   // Toggle LSB of PORT C
}

void main(void)
{
   DDRC = 0x01;   // Port C LSB is output
   EIMSK = 0x01;  // Enable INT0
   EICRA = 0x02;  // INT0 on falling edge
   #asm("sei");   // Enable interrupts
   while(1)
       ;          // Loop forever
}
```

Note: for simplicity the ISR does not show all the required house-keeping: saving **SREG** etc.

Important Considerations I

ISRs should return with an **RETI** and not **RET** instruction…

The **sei** and **cli** instructions globally enable/disable all interrupts by setting/clearing the Global Interrupt Flag (I) in **SREG** (Status Register).

Unless disabled by **cli**, interrupts can in principle occur any time, so one has to structure program to account for this.

Related to previous point – generally speaking, ISRs should save and restore resources they use → do their work as transparently as possible

Generally, ISR should be fast – do one simple task as fast as possible. Be careful about implied delays.

```
Interrupt [TMR0] void tmr0_int_isr(void)
{
    printf("%d",n);  // Print something
}
```

The ISR is one line, but the C printf function is hugely complex and quite long, so this ISR does NOT meet the fast criteria…

Important Considerations II

Once enabled, ISRs can occur at any time in the program. Programmers should structure the main program flow accordingly and plan for interrupts at any time.

Since ISRs can occur at any time in the program, the ISR should guard against side effects and save and restore registers they use.

Protect sections of code that must not be interrupted using **cli** and **sei**:

```
…
cli   ; Turn off all interrupts
      ; Code that should not be interrupted
      ; goes here
sei   ; Enable interrupts
…
```

Code that should not be interrupted is called a **critical section**.

What constitutes a critical section? This depends on the specific application. An embedded system may generate precise pulse (PWM for servo control) and have a button for user input. A critical section in this case may be a section of code where the PWM hardware or timers are reloaded, and one does not want to interrupt because a user presses the button to perform some non-critical task such as turning on the backlight on an LCD display.

Interrupt-Driven Programming

```
Interrupt [EXT_INT0] void ext_int_isr(void)
{
   // Get RPG State
}

Interrupt [EXT_INT1] void ext_int_isr(void)
{
   // Process push button
}

Interrupt [TMR0] void tmr0_int_isr(void)
{
   PORTC = PORTC ^ 0x01;   // Toggle LSB of PORT C
   TCNT0 = 125;            // reload timer
}

void main(void)
{
   DDRC = 0x01;   // Port C LSB is output
   EIMSK = 0x01;  // Enable INT0
   EICRA = 0x02;  // INT0 on falling edge
   #asm("sei");   // Enable interrupts
   while(1)
       ;          // Loop forever
}
```

Triggered when RPG changes the pin it is connected to.

Note: for simplicity the ISRs does not show all the required house-keeping: saving **SREG** etc.

Interrupt-Driven Programming

```
Interrupt [EXT_INT0] void ext_int_isr(void)
{
   // Get RPG State
}

Interrupt [EXT_INT1] void ext_int_isr(void)
{
   // Process push button
}

Interrupt [TMR0] void tmr0_int_isr(void)
{
   PORTC = PORTC ^ 0x01;   // Toggle LSB of PORT C
   TCNT0 = 125;            // reload timer
}

void main(void)
{
   DDRC = 0x01;   // Port C LSB is output
   EIMSK = 0x01;  // Enable INT0
   EICRA = 0x02;  // INT0 on falling edge
   #asm("sei");   // Enable interrupts
   while(1)
        ;          // Loop forever
}
```

Triggered when user presses button

Note: for simplicity the ISRs does not show all the required house-keeping: saving **SREG** etc.

Interrupt-Driven Programming

```
Interrupt [EXT_INT0] void ext_int_isr(void)
{
   // Get RPG State
}

Interrupt [EXT_INT1] void ext_int_isr(void)
{
   // Process push button
}

Interrupt [TMR0] void tmr0_int_isr(void)
{
   PORTC = PORTC ^ 0x01;   // Toggle LSB of PORT C
   TCNT0 = 125;            // reload timer
}

void main(void)
{
   DDRC = 0x01;   // Port C LSB is output
   EIMSK = 0x01;  // Enable INT0
   EICRA = 0x02;  // INT0 on falling edge
   #asm("sei");   // Enable interrupts
   while(1)
         ;          // Loop forever
}
```

Triggered when timer that generates square wave rolls over

Note: for simplicity the ISRs does not show all the required house-keeping: saving **SREG** etc.

Interrupt-Driven Programming

```
Interrupt [EXT_INT0] void ext_int_isr(void)
{
   // Get RPG State
}

Interrupt [EXT_INT1] void ext_int_isr(void)
{
   // Process push button
}

Interrupt [TMR0] void tmr0_int_isr(void)
{
   PORTC = PORTC ^ 0x01;   // Toggle LSB of PORT C
   TCNT0 = 125;            // reload timer
}

void main(void)
{
   DDRC = 0x01;   // Port C LSB is output
   EIMSK = 0x01;  // Enable INT0
   EICRA = 0x02;  // INT0 on falling edge
   #asm("sei");   // Enable interrupts
   while(1)
         ;          // Loop forever
}
```

Configure

Note: for simplicity the ISRs does not show all the required house-keeping: saving **SREG** etc.

Interrupt-Driven Programming

```
Interrupt [EXT_INT0] void ext_int_isr(void)
{
   // Get RPG State
}

Interrupt [EXT_INT1] void ext_int_isr(void)
{
   // Process push button
}

Interrupt [TMR0] void tmr0_int_isr(void)
{
   PORTC = PORTC ^ 0x01;   // Toggle LSB of PORT C
   TCNT0 = 125;            // reload timer
}

void main(void)
{
   DDRC = 0x01;   // Port C LSB is output
   EIMSK = 0x01;  // Enable INT0
   EICRA = 0x02;  // INT0 on falling edge
   #asm("sei");   // Enable interrupts
   while(1)
         ;          // Loop forever
}
```

Note: for simplicity the ISRs does not show all the required house-keeping: saving **SREG** etc.

Wait for interrupts

Example

Using a Timer Overflow Interrupt to Generate Square Waves

Assume we want to use timer 0 to generate a square wave on PC5, using interrupts.

* Set timer up to generate an interrupt when it overflows
* In the ISR toggle output pin PC5
* Reload the timer 0 with the required start value
* Set up ISR jump table/vector
* Global enable interrupts

```
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
;;
;;  Timer 0 Overflow interrupt ISR
;;
tim0_ovf:
   push  r25
   in    r25,sreg
   push  r25
   sbi   PINC,5      ; Toggle PORTC,5
   ldi   r25,201     ; Reload counter
   out   TCNT0,r25
   pop   r25
   out   sreg,r25
   pop   r25
   reti
```

Can name this anything, but it makes sense to use same naming conventions as in AVR documentation

Note: This ISRs does the required house-keeping: save **SREG** and **R25**

Assume we want to use timer 0 to generate a square wave on PC5, using interrupts.

* Set timer up to generate an interrupt when it overflows
* In the ISR toggle output pin PC5
* Reload the timer 0 with the required start value
* Set up ISR jump table/vector
* Global enable interrupts

```
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
;;
;;  Timer 0 Overflow interrupt ISR
;;
tim0_ovf:
   push  r25
   in    r25,sreg
   push  r25
   sbi   PINC,5      ; Toggle PORTC,5
   ldi   r25,201     ; Reload counter
   out   TCNT0,r25
   pop   r25
   out   sreg,r25
   pop   r25
   reti
```

Save **R25** and **SREG**

Note: This ISRs does the required house-keeping: save **SREG** and **R25**

Assume we want to use timer 0 to generate a square wave on PC5, using interrupts.

* Set timer up to generate an interrupt when it overflows
* In the ISR toggle output pin PC5
* Reload the timer 0 with the required start value
* Set up ISR jump table/vector
* Global enable interrupts

```
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
;;
;;  Timer 0 Overflow interrupt ISR
;;
tim0_ovf:
   push  r25
   in    r25,sreg
   push  r25
   sbi   PINC,5       ; Toggle PORTC,5
   ldi   r25,201      ; Reload counter
   out   TCNT0,r25
   pop   r25
   out   sreg,r25
   pop   r25
   reti
```

Note how we toggle PC5 by writing 1 to PINC,5

Note: This ISRs does the required house-keeping: save **SREG** and **R25**

Assume we want to use timer 0 to generate a square wave on PC5, using interrupts.

* Set timer up to generate an interrupt when it overflows
* In the ISR toggle output pin PC5
* Reload the timer 0 with the required start value
* Set up ISR jump table/vector
* Global enable interrupts

```
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
;;
;;  Timer 0 Overflow interrupt ISR
;;
tim0_ovf:
   push  r25
   in    r25,sreg
   push  r25
   sbi   PINC,5       ; Toggle PORTC,5
   ldi   r25,201      ; Reload counter
   out   TCNT0,r25
   pop   r25
   out   sreg,r25
   pop   r25
   reti
```

Reload counter.

Note: This ISRs does the required house-keeping: save SREG and r25

Assume we want to use timer 0 to generate a square wave on PC5, using interrupts.

* Set timer up to generate an interrupt when it overflows
* In the ISR toggle output pin PC5
* Reload the timer 0 with the required start value
* Set up ISR jump table/vector
* Global enable interrupts

```
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
;;
;;  Timer 0 Overflow interrupt ISR
;;
tim0_ovf:
   push  r25
   in    r25,sreg
   push  r25
   sbi   PINC,5      ; Toggle PORTC,5
   ldi   r25,201     ; Reload counter
   out   TCNT0,r25
   pop   r25
   out   sreg,r25
   pop   r25
   reti
```

Restore **SREG** and **R25**

Note: This ISRs does the required house-keeping: save **SREG** and **R25**

Assume we want to use timer 0 to generate a square wave on PC5, using interrupts.

* Set timer up to generate an interrupt when it overflows
* In the ISR toggle output pin PC5
* Reload the timer 0 with the required start value
* Set up ISR jump table/vector
* Global enable interrupts

```
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
;;
;;  Timer 0 Overflow interrupt ISR
;;
tim0_ovf:
   push  r25
   in    r25,sreg
   push  r25
   sbi   PINC,5      ; Toggle PORTC,5
   ldi   r25,201     ; Reload counter
   out   TCNT0,r25
   pop   r25
   out   sreg,r25
   pop   r25
   reti
```

Return with **reti**

Note: This ISRs **does the required house-keeping**: save **SREG** and **R25**

```
;; Shows how to use timer 0 overflow interrupt.

.include "m88padef.inc"
.cseg
.org 0x00          ; PC points here after power up,
   rjmp  reset     ;   hardware reset, WDT timeout

.org 0x010         ; PC points here on timer 0
   rjmp  tim0_ovf  ;   over flow interrupt

.org  0x1a         ; Just past the last ISR vector
reset:             ;  on ATmega88PA (see docs)

; Configure PC5 as output, used for LED.
   sbi   DDRC,5

; Enable overflow interrupt on 8-bit timer 0.
   lds   r24,TIMSK0
   ori   r24,0x01       ; Overflow interrupt enable
   sts   TIMSK0,r24

; Turn timer 0 on, use system clock, prescaled with
; 256 => increment at (8 MHz)/256
   ldi   r24,0x04
   out   TCCR0B,r24

; Enable interrupts and enter main loop.
   sei
main:
    rjmp  main
```

PC points here at reset. Jump to main loop


```
;; Shows how to use timer 0 overflow interrupt.

.include "m88padef.inc"
.cseg
.org 0x00          ; PC points here after power up,
   rjmp  reset     ;   hardware reset, WDT timeout

.org 0x010         ; PC points here on timer 0
   rjmp  tim0_ovf  ;   over flow interrupt

.org  0x1a         ; Just past the last ISR vector
reset:             ;  on ATmega88PA (see docs)

; Configure PC5 as output, used for LED.
   sbi   DDRC,5

; Enable overflow interrupt on 8-bit timer 0.
   lds   r24,TIMSK0
   ori   r24,0x01       ; Overflow interrupt enable
   sts   TIMSK0,r24

; Turn timer 0 on, use system clock, prescaled with
; 256 => increment at (8 MHz)/256
   ldi   r24,0x04
   out   TCCR0B,r24

; Enable interrupts and enter main loop.
   sei
main:
    rjmp  main
```

Timer 0's slot in the ISR vector table. Place an **rjmp** there to the rest of the ISR code

```
;; Shows how to use timer 0 overflow interrupt.

.include "m88padef.inc"
.cseg
.org 0x00         ; PC points here after power up,
   rjmp  reset    ;   hardware reset, WDT timeout

.org 0x010        ; PC points here on timer 0
   rjmp  tim0_ovf ;   over flow interrupt

.org  0x1a        ; Just past the last ISR vector
reset:            ;  on ATmega88PA (see docs)

; Configure PC5 as output, used for LED.
   sbi   DDRC,5

; Enable overflow interrupt on 8-bit timer 0.
   lds   r24,TIMSK0
   ori   r24,0x01       ; Overflow interrupt enable
   sts   TIMSK0,r24

; Turn timer 0 on, use system clock, prescaled with
; 256 => increment at (8 MHz)/256
   ldi   r24,0x04
   out   TCCR0B,r24

; Enable interrupts and enter main loop.
   sei
main:
    rjmp  main
```

0x1a is the address just beyond the last ISR vector on the ATmega88PA


```
;; Shows how to use timer 0 overflow interrupt.

.include "m88padef.inc"
.cseg
.org 0x00         ; PC points here after power up,
   rjmp  reset    ;   hardware reset, WDT timeout

.org 0x010        ; PC points here on timer 0
   rjmp  tim0_ovf ;   over flow interrupt

.org  0x1a        ; Just past the last ISR vector
reset:            ;  on ATmega88PA (see docs)

; Configure PC5 as output, used for LED.
   sbi   DDRC,5

; Enable overflow interrupt on 8-bit timer 0.
   lds   r24,TIMSK0
   ori   r24,0x01       ; Overflow interrupt enable
   sts   TIMSK0,r24

; Turn timer 0 on, use system clock, prescaled with
; 256 => increment at (8 MHz)/256
   ldi   r24,0x04
   out   TCCR0B,r24

; Enable interrupts and enter main loop.
   sei
main:
    rjmp  main
```

Start of program

```
;; Shows how to use timer 0 overflow interrupt.

.include "m88padef.inc"
.cseg
.org 0x00         ; PC points here after power up,
   rjmp  reset    ;   hardware reset, WDT timeout

.org 0x010        ; PC points here on timer 0
   rjmp  tim0_ovf ;   over flow interrupt

.org  0x1a        ; Just past the last ISR vector
reset:            ;  on ATmega88PA (see docs)

; Configure PC5 as output, used for LED.
   sbi   DDRC,5

; Enable overflow interrupt on 8-bit timer 0.
   lds   r24,TIMSK0
   ori   r24,0x01       ; Overflow interrupt enable
   sts   TIMSK0,r24

; Turn timer 0 on, use system clock, prescaled with
; 256 => increment at (8 MHz)/256
   ldi   r24,0x04
   out   TCCR0B,r24

; Enable interrupts and enter main loop.
   sei
main:
    rjmp  main
```

Note the use of **lds** and **sts** rather than **in/out**. This is because the address of **TMSK0** is outside the 0…63 address range that **in/out** can handle.


```
;; Shows how to use timer 0 overflow interrupt.

.include "m88padef.inc"
.cseg
.org 0x00         ; PC points here after power up,
   rjmp  reset    ;   hardware reset, WDT timeout

.org 0x010        ; PC points here on timer 0
   rjmp  tim0_ovf ;   over flow interrupt

.org  0x1a        ; Just past the last ISR vector
reset:            ;  on ATmega88PA (see docs)

; Configure PC5 as output, used for LED.
   sbi   DDRC,5

; Enable overflow interrupt on 8-bit timer 0.
   lds   r24,TIMSK0
   ori   r24,0x01       ; Overflow interrupt enable
   sts   TIMSK0,r24

; Turn timer 0 on, use system clock, prescaled with
; 256 => increment at (8 MHz)/256
   ldi   r24,0x04
   out   TCCR0B,r24

; Enable interrupts and enter main loop.
   sei
main:
    rjmp  main
```

Configure timer

```
;; Shows how to use timer 0 overflow interrupt.

.include "m88padef.inc"
.cseg
.org 0x00         ; PC points here after power up,
   rjmp  reset    ;   hardware reset, WDT timeout

.org 0x010        ; PC points here on timer 0
   rjmp  tim0_ovf ;   over flow interrupt

.org  0x1a        ; Just past the last ISR vector
reset:            ;  on ATmega88PA (see docs)

; Configure PC5 as output, used for LED.
   sbi   DDRC,5

; Enable overflow interrupt on 8-bit timer 0.
   lds   r24,TIMSK0
   ori   r24,0x01       ; Overflow interrupt enable
   sts   TIMSK0,r24

; Turn timer 0 on, use system clock, prescaled with
; 256 => increment at (8 MHz)/256
   ldi   r24,0x04
   out   TCCR0B,r24

; Enable interrupts and enter main loop.
   sei
main:
    rjmp  main
```

Turn on interrupts and enter main loop

EICRA – External Interrupt Control Register A

The External Interrupt Control Register A **EIRCA** contains control bits for interrupt sense control.

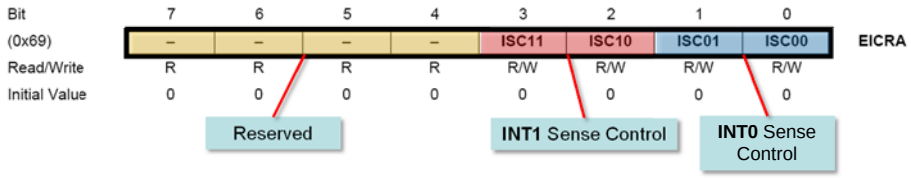


Table 12-1. Interrupt 1 Sense Control

ISC11	ISC10	Description
0	0	The low level of INT1 generates an interrupt request.
0	1	Any logical change on INT1 generates an interrupt request.
1	0	The falling edge of INT1 generates an interrupt request.
1	1	The rising edge of INT1 generates an interrupt request.

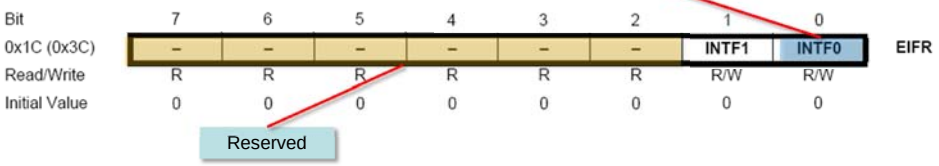
Table 12-2. Interrupt 0 Sense Control

ISC01	ISC00	Description
0	0	The low level of INT0 generates an interrupt request.
0	1	Any logical change on INT0 generates an interrupt request.
1	0	The falling edge of INT0 generates an interrupt request.
1	1	The rising edge of INT0 generates an interrupt request.

EIFR – External Interrupt Flag Register

When an edge or logic change on the **INT0** pin triggers an interrupt request, **INTF0** becomes set (one). If the **I**-bit in **SREG** and the **INT0** bit in **EIMSK** are set (one), the MCU will jump to the corresponding Interrupt Vector. The flag is cleared when the interrupt routine is executed.

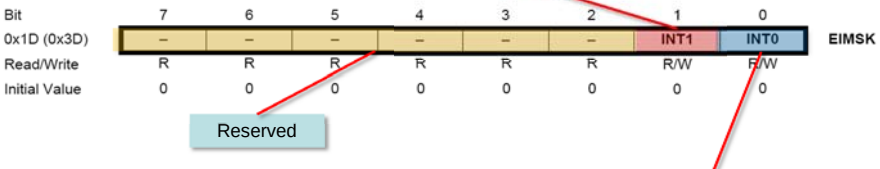
Alternatively, the flag can be cleared by writing a logical one to it.



Reserved

EIMSK – External Interrupt Mask Register

When the **INT1** bit is set (one) and the **I**-bit in the Status Register (**SREG**) is set (one), the external pin interrupt is enabled.



Reserved

When the **INT**0 bit is set (one) and the **I**-bit in the Status Register (**SREG**) is set (one), the external pin interrupt is enabled.

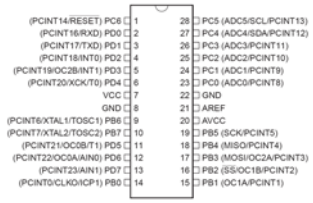
PIN Change Registers

ATmega88: Each I/O pin can trigger a PIN change interrupt.

→ Can be enabled individually by setting bits in PCMSK0, PCMSK1, and PCMSK2 registers to 1.

→ Note: also need to configure PCICR register in addition to globally enabling interrupts.

→ See section “External Interrupts” in datasheet …



PCMSK2 – Pin Change Mask Register 2

Bit	7	6	5	4	3	2	1	0	
(0x6D)	PCINT23	PCINT22	PCINT21	PCINT20	PCINT19	PCINT18	PCINT17	PCINT16	PCMSK2
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

PortD

PCMSK1 – Pin Change Mask Register 1

Bit	7	6	5	4	3	2	1	0	
(0x6C)	–	PCINT14	PCINT13	PCINT12	PCINT11	PCINT10	PCINT9	PCINT8	PCMSK1
Read/Write	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

PortC

PCMSK0 – Pin Change Mask Register 0

Bit	7	6	5	4	3	2	1	0	
(0x6B)	PCINT7	PCINT6	PCINT5	PCINT4	PCINT3	PCINT2	PCINT1	PCINT0	PCMSK0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

PortB

PIN Change Registers

PCICR – Pin Change Interrupt Control Register

Bit	7	6	5	4	3	2	1	0	
(0x68)	–	–	–	–	–	PCIE2	PCIE1	PCIE0	PCICR
Read/Write	R	R	R	R	R	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

PCIFR – Pin Change Interrupt Flag Register

Bit	7	6	5	4	3	2	1	0	
0x1B (0x3B)	–	–	–	–	–	PCIF2	PCIF1	PCIF0	PCIFR
Read/Write	R	R	R	R	R	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

PCMSK2 – Pin Change Mask Register 2

Bit	7	6	5	4	3	2	1	0	
(0x6D)	PCINT23	PCINT22	PCINT21	PCINT20	PCINT19	PCINT18	PCINT17	PCINT16	PCMSK2
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

PortD

PCMSK1 – Pin Change Mask Register 1

Bit	7	6	5	4	3	2	1	0	
(0x6C)	–	PCINT14	PCINT13	PCINT12	PCINT11	PCINT10	PCINT9	PCINT8	PCMSK1
Read/Write	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

PortC

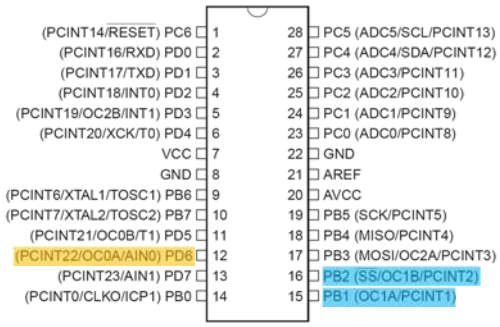
PCMSK0 – Pin Change Mask Register 0

Bit	7	6	5	4	3	2	1	0	
(0x6B)	PCINT7	PCINT6	PCINT5	PCINT4	PCINT3	PCINT2	PCINT1	PCINT0	PCMSK0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

PortB

Example - PIN Change Interrupts

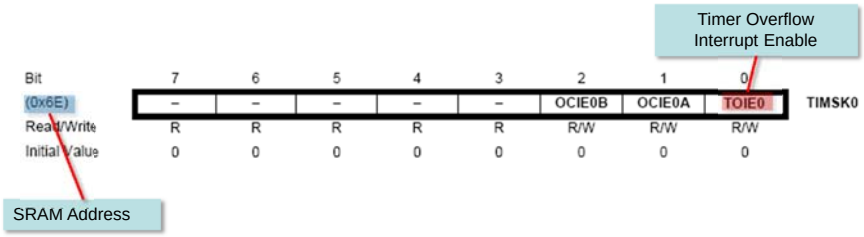
- **Q1: What configuration is need to enable PIN change interrupts on PD6, PB1, and PB2?**
- **Q2: What are the implications of using I/O lines PD6, PB1, and PB2 for PIN change interrupts?**



→ Solution on whiteboard!

Some I/O Locations are "Problematic"

The **IN/OUT** instructions access location in I/O space. However, some configuration are out of reach of the **IN/OUT** (0…63) range, so one has to use **LDS** and **STS** instructions:



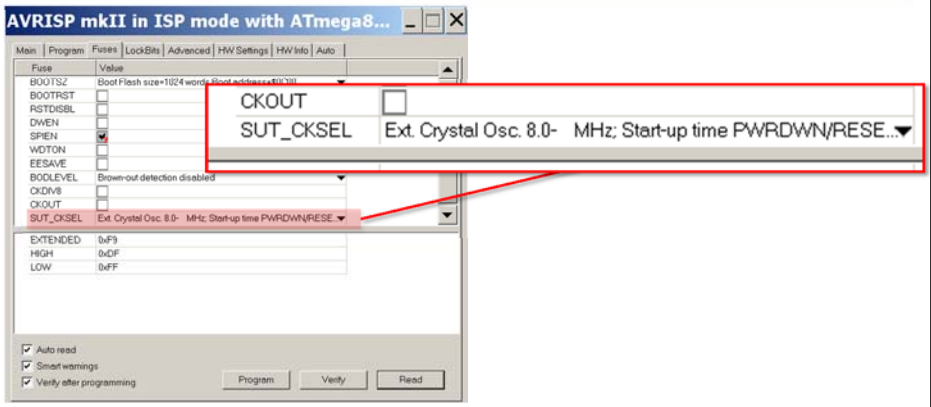

```
; Enable overflow interrupt on 8-bit timer 0.
; Use LDS and STS instructions, since IN/OUT can
; only access addresses in range 0...63, and TIMSK0
; on ATmega88 is at 0x6E.
   lds   r24,TIMSK0     ; Grab the 8-bit timer's interrupt mask
   ori   r24,0x01       ; Enable overflow interrupt
   sts   TIMSK0,r24     ; Update the interrupt mask
```

→ See file "m88PAdef.inc" on website

Waking Up Via External Interrupts

Note that if a **level triggered interrupt** is used for **wake-up from Power-down**, the required level must be held long enough for the MCU to complete the wake-up to trigger the level interrupt.
If the level disappears before the end of the Start-up Time, the MCU will still wake up, but no interrupt will be generated.

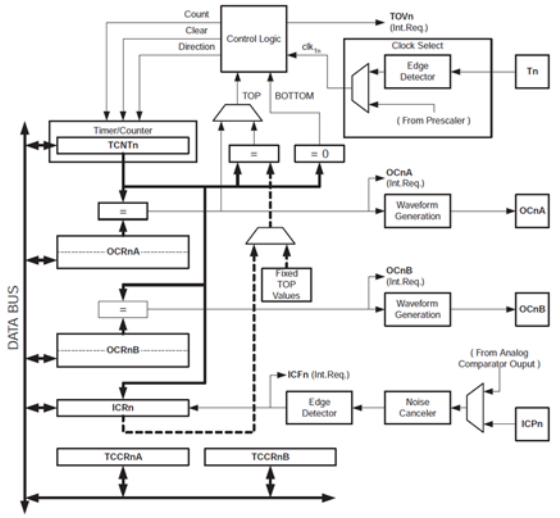
The start-up time is defined by the **SUT** and **CKSEL** Fuses



ATmega88PA – 16bit Timer/Counter

ATmega88PA – 16bit Timer/Counter

Figure 15-1. 16-bit Timer/Counter Block Diagram[1]



There are some similarities with the 8-bit version!

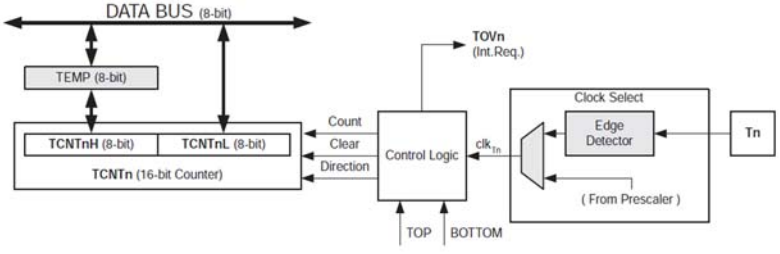
Assume that we want to use TCNT1 as a timer.

Note: 1. Refer to Figure 1-1 on page 2, Table 13-3 on page 82 and Table 13-9 on page 88 for Timer/Counter1 pin placement and description.

ATmega88PA – 16bit Timer/Counter: 16bit Registers

- **Reading/writing requires using the TEMP register!**
- **Sequence of access to TCNT1H and TCNT1L registers is important! (→ also for 16bit OCR1A and OCR1B registers)**
- **Loading: 1) Rr → TCNT1H 2) Rr → TCNT1L**
- **Reading: 1) Rd ← TCNT1L 2) Rd ← TCNT1H**
- See datasheet or lecture notes for details!

Figure 15-2. Counter Unit Block Diagram



ATmega88PA – 16bit Timer/Counter: Clock Source

Table 15-5. Clock Select Bit Description

CS12	CS11	CS10	Description
0	0	0	No clock source (Timer/Counter stopped).
0	0	1	$clk_{I/O}$/1 (No prescaling)
0	1	0	$clk_{I/O}$/8 (From prescaler)
0	1	1	$clk_{I/O}$/64 (From prescaler)
1	0	0	$clk_{I/O}$/256 (From prescaler)
1	0	1	$clk_{I/O}$/1024 (From prescaler)
1	1	0	External clock source on T1 pin. Clock on falling edge.
1	1	1	External clock source on T1 pin. Clock on rising edge.

If external pin modes are used for the Timer/Counter1, transitions on the T1 pin will clock the counter even if the pin is configured as an output. This feature allows software control of the counting.

Q: Criteria for selection?

ATmega88PA – 16bit Timer/Counter: Modes

Table 15-4. Waveform Generation Mode Bit Description[1]

Mode	WGM13	WGM12 (CTC1)	WGM11 (PWM11)	WGM10 (PWM10)	Timer/Counter Mode of Operation	TOP	Update of OCR1x at	TOV1 Flag Set on
0	0	0	0	0	Normal	0xFFFF	Immediate	MAX
1	0	0	0	1	PWM, Phase Correct, 8-bit	0x00FF	TOP	BOTTOM
2	0	0	1	0	PWM, Phase Correct, 9-bit	0x01FF	TOP	BOTTOM
3	0	0	1	1	PWM, Phase Correct, 10-bit	0x03FF	TOP	BOTTOM
4	0	1	0	0	CTC	OCR1A	Immediate	MAX
5	0	1	0	1	Fast PWM, 8-bit	0x00FF	BOTTOM	TOP
6	0	1	1	0	Fast PWM, 9-bit	0x01FF	BOTTOM	TOP
7	0	1	1	1	Fast PWM, 10-bit	0x03FF	BOTTOM	TOP
8	1	0	0	0	PWM, Phase and Frequency Correct	ICR1	BOTTOM	BOTTOM
9	1	0	0	1	PWM, Phase and Frequency Correct	OCR1A	BOTTOM	BOTTOM
10	1	0	1	0	PWM, Phase Correct	ICR1	TOP	BOTTOM
11	1	0	1	1	PWM, Phase Correct	OCR1A	TOP	BOTTOM
12	1	1	0	0	CTC	ICR1	Immediate	MAX
13	1	1	0	1	(Reserved)	–	–	–
14	1	1	1	0	Fast PWM	ICR1	BOTTOM	TOP
15	1	1	1	1	Fast PWM	OCR1A	BOTTOM	TOP

Note: 1. The CTC1 and PWM11:0 bit definition names are obsolete. Use the WGM12:0 definitions. However, the functionality and location of these bits are compatible with previous versions of the timer.

CTC ... Clear Timer on Compare Match

ATmega88PA – 16bit Timer/Counter

TIFR1 – Timer/Counter1 Interrupt Flag Register

Bit	7	6	5	4	3	2	1	0	
0x16 (0x36)	–	–	ICF1	–	–	OCF1B	OCF1A	TOV1	TIFR1
Read/Write	R	R	R/W	R	R	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

- **Bit 0 – TOV1: Timer/Counter1, Overflow Flag**

The setting of this flag is dependent of the WGM13:0 bits setting. In Normal and CTC modes, the TOV1 Flag is set when the timer overflows. Refer to Table 15-4 on page 136 for the TOV1 Flag behavior when using another WGM13:0 bit setting.

TOV1 is automatically cleared when the Timer/Counter1 Overflow Interrupt Vector is executed. Alternatively, TOV1 can be cleared by writing a logic one to its bit location.

CTC mode

TIMSK1 – Timer/Counter1 Interrupt Mask Register

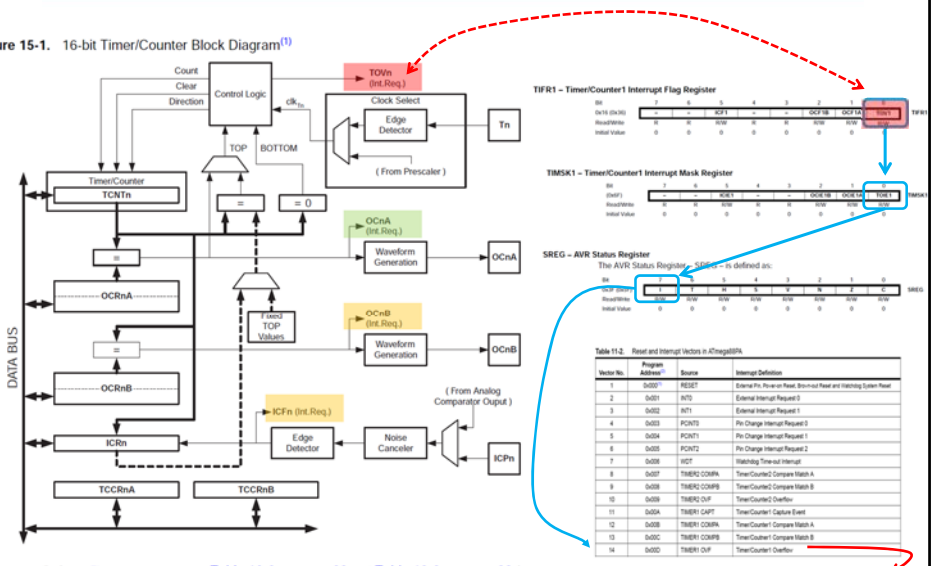
Bit	7	6	5	4	3	2	1	0	
(0x6F)	–	–	ICIE1	–	–	OCIE1B	OCIE1A	TOIE1	TIMSK1
Read/Write	R	R	R/W	R	R	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

- **Bit 0 – TOIE1: Timer/Counter1, Overflow Interrupt Enable**

When this bit is written to one, and the I-flag in the Status Register is set (interrupts globally enabled), the Timer/Counter1 Overflow interrupt is enabled. The corresponding Interrupt Vector (See "Interrupts" on page 57) is executed when the TOV1 Flag, located in TIFR1, is set.

ATmega88PA – 16bit Timer/Counter: Interrupts

Figure 15-1. 16-bit Timer/Counter Block Diagram[1]



Note: 1. Refer to Figure 1-1 on page 2, Table 13-3 on page 82 and Table 13-9 on page 88 for Timer/Counter1 pin placement and description.

0x00D rjmp TCNT1_ISR

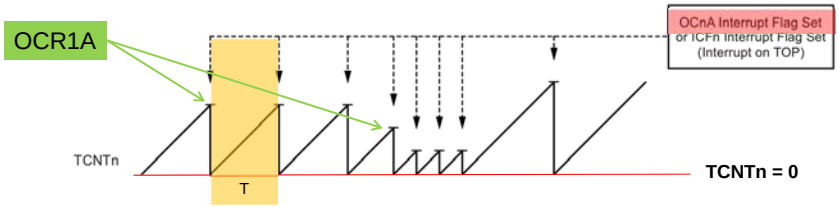
Example – Utilization of 16-bit TC1 of ATmega88 in CTC Mode

16.9.2 Clear Timer on Compare Match (CTC) Mode

In *Clear Timer on Compare* or CTC mode (WGM13:0 = 4 or 12), the OCR1A or ICR1 register are used to manipulate the counter resolution. In CTC mode the counter is cleared to zero when the counter value (TCNT1) matches either the OCR1A (WGM13:0 = 4) or the ICR1 (WGM13:0 = 12). The OCR1A or ICR1 define the top value for the counter, hence also its resolution. This mode allows greater control of the compare match output frequency. It also simplifies the operation of counting external events.

The timing diagram for the CTC mode is shown in Figure 16-6. The counter value (TCNT1) increases until a compare match occurs with either OCR1A or ICR1, and then counter (TCNT1) is cleared.

Figure 16-6. CTC Mode, Timing Diagram



$T = (1+OCRnA) * (f_{clk\_IO} / N)^{-1}$
N … prescaler factor (1, 8, 64, 256, or 1024)

Example: produce a 50 Hz square wave on PB1 (T_on=10ms; T_off=10ms)

Example – Utilization of 16-bit TC1 of ATmega88 in CTC Mode

```
.cseg
.org 0x0000
rjmp start

.org 0x000B;
rjmp TIMER1_COMPA

.org 0x001A ; Main program start
start:
sbi DDRB, 1; configure PB1 as output

;*****************************************************
; configure 16-bit TC1 of uC with 8MHz external clock
;*****************************************************
.set delayN = 10000-1; count for 10 ms;  see configuration below

ldi R16, high(delayN); IMPORTANT load HIGH before LOW !!!! ---> use TEMP register
sts OCR1AH, R16
ldi R16, low(delayN);
sts OCR1AL, R16

ldi R16, (1<<OCIE1A); Output Compare A Match Interrupt Enable
sts TIMSK1, R16
sei; global interrupt enable

ldi R16, 0x00; configure CTC mode with clk_io/8 and
sts TCCR1A, R16
ldi R16, (1<<WGM12)|(1<<CS11); start TC1
sts TCCR1B, R16
…
```

Example: produce a 50 Hz square wave on PB1 (T_on=10ms; T_off=10ms)

Example – Utilization of 16-bit TC1 of ATmega88 in CTC Mode

```
…
;****************************************************
loop:             ; main program; do nothing
    nop
    rjmp loop
;****************************************************

TIMER1_COMPA:  ; ISR for TC1
sbi PINB,1     ; toggle PB1 (note: we could do this in HW too!) --> 50 Hz signal
reti
```

→ Result: periodic (100 Hz → 10 ms) interrupt

… EOL