**VGA Transpose and Edge Detection**

Team 7

Zachary Boe, Benjamin Sullins, Gregory Walls, and Bryce Williams

*Abstract --* A simple design is presented for a VGA image transpose and edge detector circuit. The circuit will be designed in VHDL and implemented on a Basys3 Artix-7 FPGA Trainer Board. The design will consist of four stages. Figure 1 displays the four stages of the design.

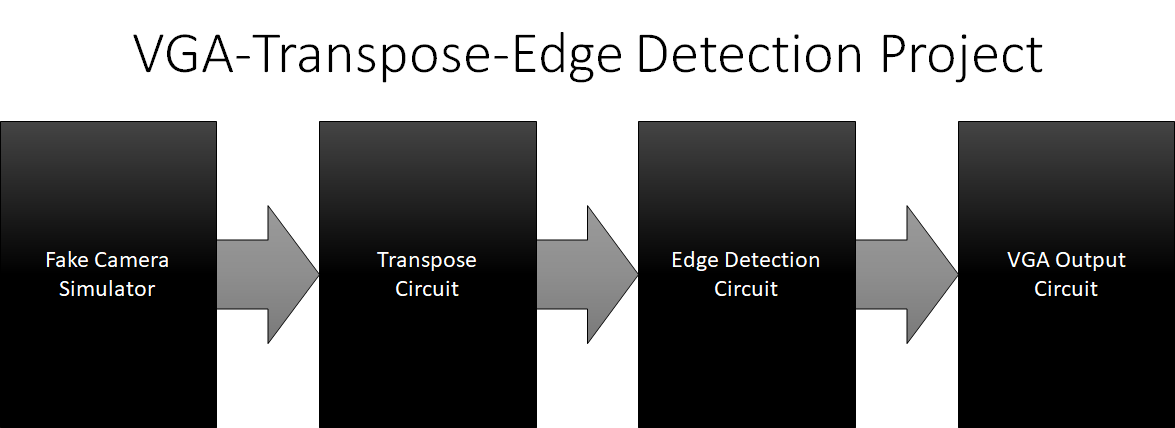


Figure 1: Design Overview

|  |  |
| --- | --- |
| **Deliverables** | |
| Fake Camera Simulator:   1. Synthetic Video    1. Horizontal Test Pattern    2. Vertical Test Pattern    3. Pre-Loaded Image    4. 320 x 240 - Monochrome 2. User Selectable Video Output Options    1. Switch/Button | Transpose Circuit:   1. User Selectable Transpose Output Options    1. Switch/Button 2. Video Options    1. Non-transposed    2. Transposed 3. Unaltered Original Video Timing |
| Edge Detection Circuit:   1. User Selectable Video Options    1. Unfiltered    2. Edge Detection Filtered 2. Sobel Filter    1. Horizontal and Vertical    2. 3x3 Kernel 3. Unaltered Original Video Timing | VGA Output Circuit:   1. VESA Standard Video Output 2. Upsampled Video Scaling    1. 320x240 to 640x480 |

The Fake Camera Simulator is the first stage of the design. It provides synthetic video frames, reflective of a real-life camera input, which propagates throughout the design’s logic. The available video selections will be a horizontal/vertical test patterns and a pre-loaded image found within an internal BRAM. The user will have the option of selecting between the video options through a switch/button. Figure 2 below shows a graphical layout of the proposed design.

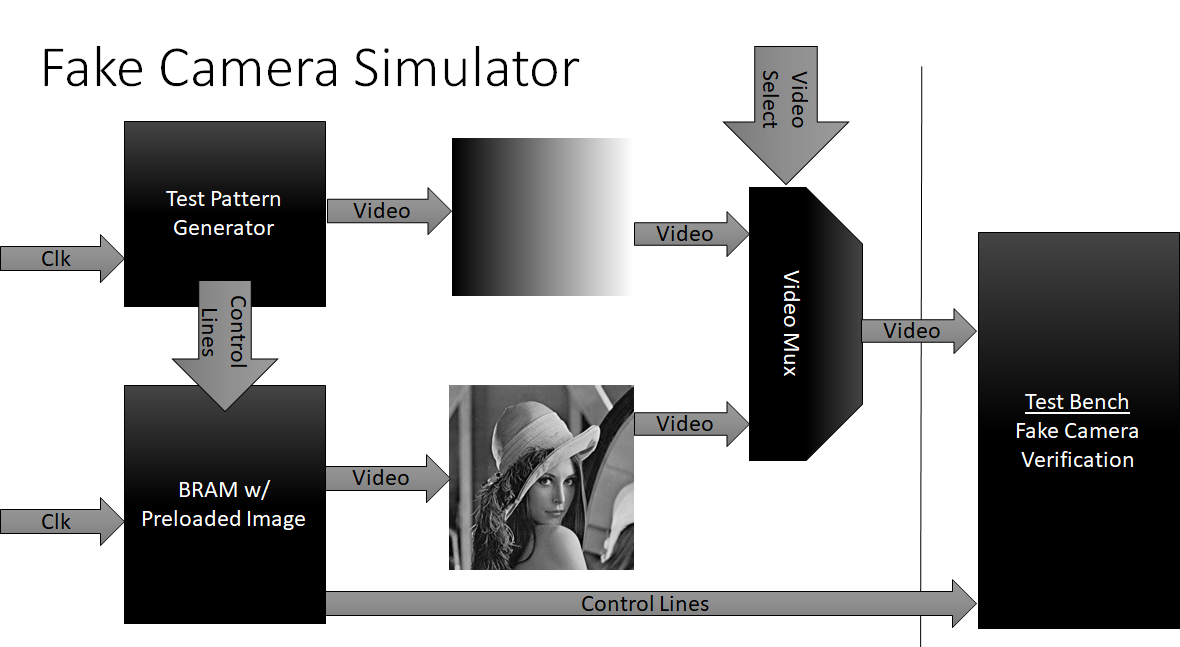


Figure 2: Fake Camera Simulator

The Transpose Circuit performs the action of transposing the input image. The module will buffer the image into a BRAM and read out a user-selectable video option. Options include non-transposed and transposed video and selections are made through a switch/button. The readout circuit will maintain the original video format and timing. Figure 3 shows a generic graphical layout of the design.

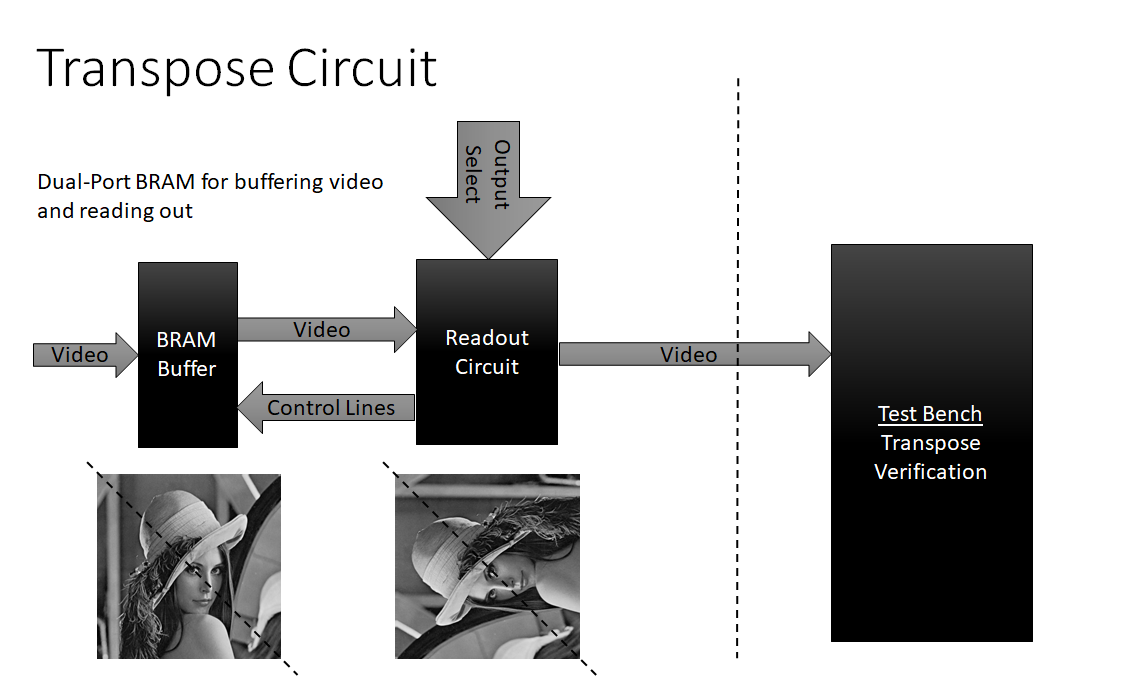


Figure 3: Transpose Circuit

The Edge Detection Circuit will implement a horizontal/vertical sobel filter used in edge detection algorithms. A switch/button will allow the user to select between unfiltered video and edge detected video. The edge detection circuit will utilize a set of BRAM line buffers for generating the kernel elements needed for the sobel filter. Figure 4 shows a generic overview of the implementation.

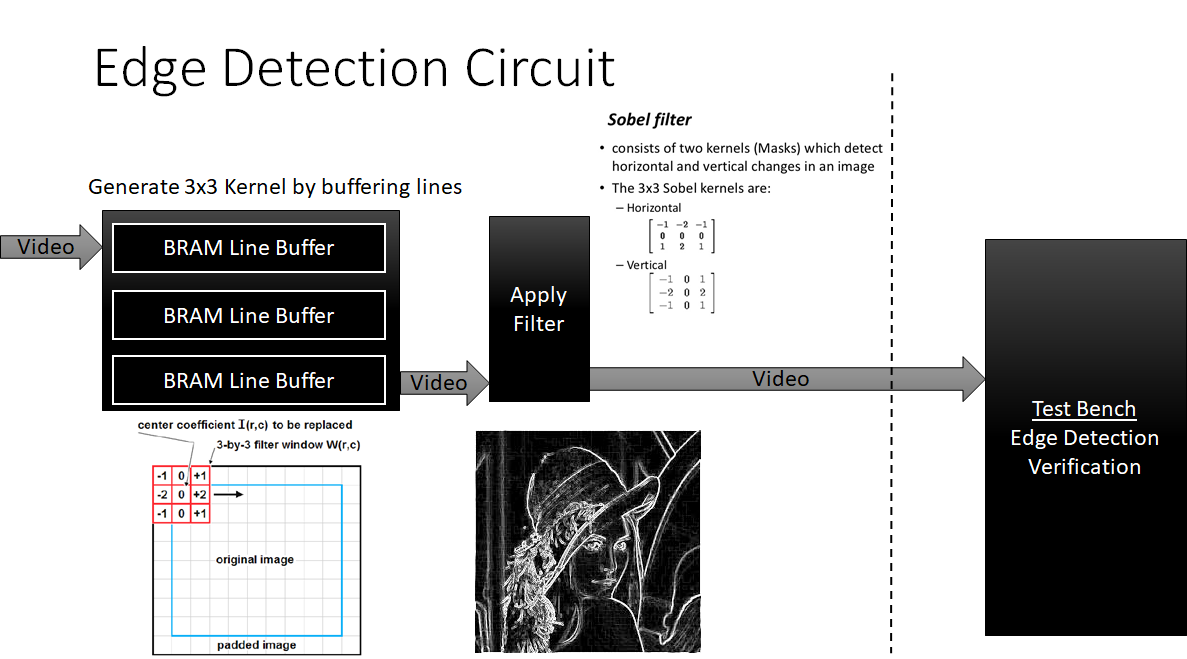


Figure 4: Edge Detection Circuit

Finally, a VGA output circuit will re-time the input video signals for output to a VGA display. The module will buffer the input video into a BRAM and be read out according to the VESA standard. Figure 5 shows a generic overview of the implementation.

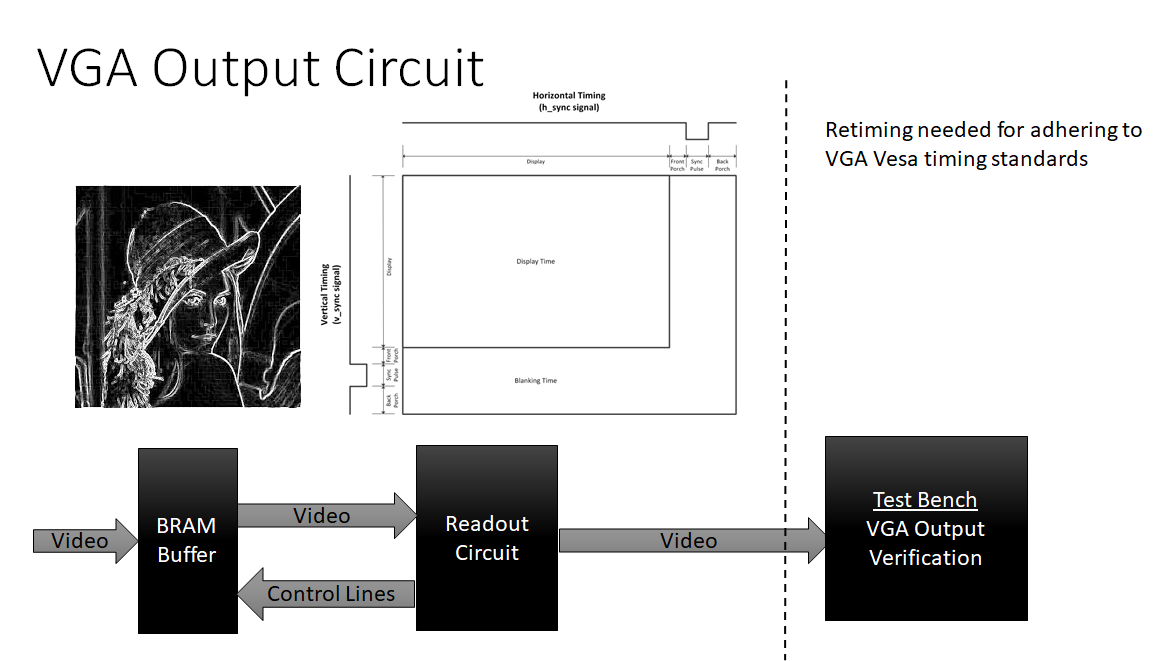


Figure 5: VGA Output Circuit