Revision	Date	Author	Comments
1A	2020-06-18	Tim S. timothystotts08@gmail.com	First publishable draft of the serial flash sector tester
2A	2020-06-19	Tim S. timothystotts08@gmail.com	Clerical updates to documentation and code.

Serial Flash Sector-Tester Experiment

Serial Flash Sector-Tester Experiment: Folder Structure

Example Homework Solutions with equivalent function of performing an erase/program/read cycle in 1/32 address steps of a 256 Mbit Serial Flash.

Project Folder	Project Description
SF3-Experiment-Single-Clock-VHDL (Vivado 2020.1)	A utility designed for a custom operation of a serial flash and displaying erase/program/read-back byte error count on both an LCD and a serial terminal. The design is completely in VHDL RTL and visual VHDL test-bench without a soft processor. Multiple clock domains exist; and each 7 MHz or faster domain is controlled by a MMCM, and each slower domain is controlled by a clock enable divider RTL dividing a MMCM clock by clock enable pulse instead of clock division. Clock dividers are only used for the generation of an output clock that outputs at a bus port on the FPGA.
SF3-Experiment-AXI (Vivado 2020.1 and Vitis 2020.1)	A utility designed for custom operation of a serial flash and displaying erase/program/read-back byte error count on both an LCD and a serial terminal. The design is completely in Microblaze AXI subsystem with standard Xilinx IP Integrator components, and C language program executing on the Microblaze soft processor.

For the SF3-Experiment-AXI project, the BSP of the bootloader and the BSP of the application require that the flash family parameter be set in the xilisf configuration on the BSP configure page. The default value is 1, but must be changed to 5 as the Arty-A7-100T board has a Spansion 128Mbit serial flash for booting the FPGA.

To successfully open the project, it is necessary to add the directory arty-a7-100 from the directory board_files/ to the installation directory of Vivado 2020.1. For example:

```
$ which vivado
/opt/Xilinx/Vivado/2020.1/bin/vivado
$ cd ./board_files
$ sudo cp -R ./arty-a7-100 /opt/Xilinx/Vivado/2020.1/data/boards/board_files/
# (do not copy the board_files to /opt/Xilinx/Vitis/2020.1/data/boards/board_files/)
```

Note that the Digilent Guide at https://reference.digilentinc.com/vivado/installing-vivado/2018.2 indicates that an initialization script can be executed in the user's profile to set up a path to additional board files. It is the experience of this author that the TCL initialization script provides an intermittent or non-functional detection of the board files in the user's home folder. By copying to the install directory of the tool, the board files are always found. Otherwise, the following TCL command is supposed to instruct Vivado to locate the board files:

```
set_param board.repoPaths [list "<extracted path>/Vivado/board_files"]
```

Serial Flash Sector-Tester Experiment: Methods of Operation

For the SF3-Experiment, the purpose of the design is to boot a Digilent Inc. Arty-A7-100T (Artix-7) development board with PMOD CLS and PMOD SF3 peripheral boards, which are a 16x2 Character dot-matrix LCD display, and a 256 Mbit serial flash, respectively. Each PMOD connects to the FPGA with its own dedicated SPI bus via a moderately high-speed plug and jack. The PMOD CLS connects to board PMOD port JB. The PMOD SF3 connects to board PMOD port JC.

Serial Flash Sector-Tester Experiment: Method of Operation: iterative erase/program/read-back byte memory test from beginning to end of the serial flash

Serial Flash Sector-Tester Experiment: Design Theory

In the VHDL example, the four switches are debounced as mutually exclusive inputs, as are the four buttons. Each time a button is depressed and then released, a single pass of 1/32 of the memory space at the current memory index is tested for erase/program/read-back byte errors. Upon the next button depress, the subsequent 1/32 of the memory space is tested with cumulative results displayed. To test the whole memory without needing to press a button 32 times; a switch can be placed in the on position and will select the same pattern index (A, B, C, or D) as the button of the same index would have. Button 0 and Switch 0 select test pattern A. Button 1 and Switch 1 select test pattern B. Button 2 and Switch 2 select test pattern C. Button 3 and Switch 3 select test pattern D. A red color on all four LD0, LD1, LD2, LD3, indicate that the test is paused and waiting for user input; or that the test has completed. A green color on LD0, or LD1, LD2, LD3, indicates which switch or button was depressed. A white LED indicates ERASE (ERS), PROGRAM (PRO), TEST READ-BACK (TST), or DISPLAY INCREMENT (END), to show the sequential advancement of the testing of each memory area in four steps, starting with a white color on LD0, then LD1, LD2, LD3.

Please read the source code comments to discover the custom design of clock dividers, clock enable dividers, SPI bus drivers, PMOD SF3 and PMOD CLS operational drivers. Conceptual-only FSM diagrams are also included in this portfolio in the PDF document `SF3-Design-Documents/SF3-Experiment-Design-Diagrams.pdf`.

Note that in the AXI example, drivers downloaded from Digilent Inc. for the PMOD SF3 and PMOD CLS are used in the block design with some minimal modification and update to Xilinx Vivado and Vitis release 2020.1. The AXI example demonstrates integration of vendor components plus adding additional C code.

Serial Flash Sector-Tester Experiment: 3rd-party references:

How To Store Your SDK Project in SPI Flash
https://reference.digilentinc.com/learn/programmable-logic/tutorials/htsspisf/start

Master XDC files for all Digilent Inc. boards, including Arty-A7-100T
https://github.com/Digilent/digilent-xdc

Digilent Inc IP library for Xilinx Vivado
https://github.com/Digilent/vivado-library/