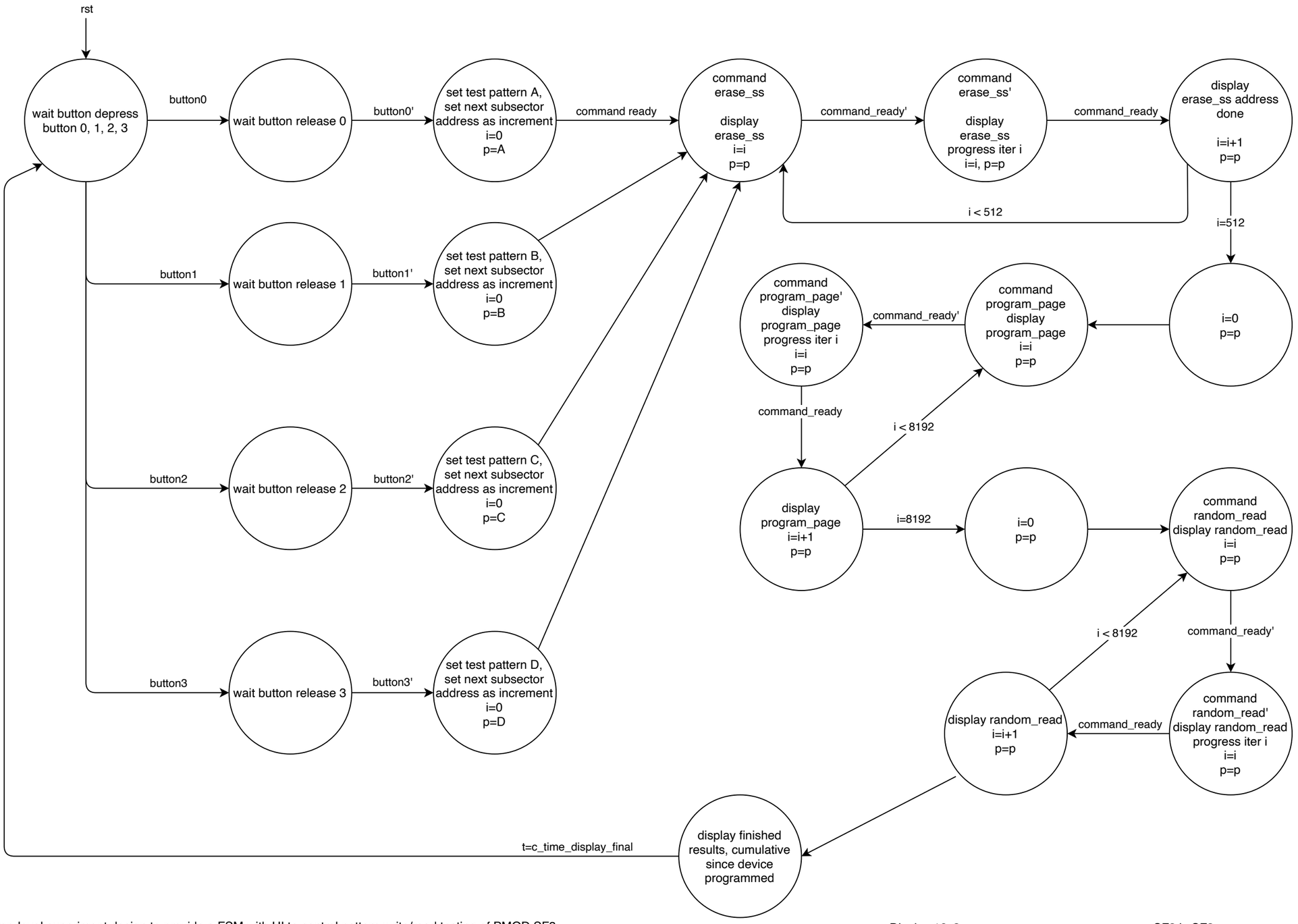


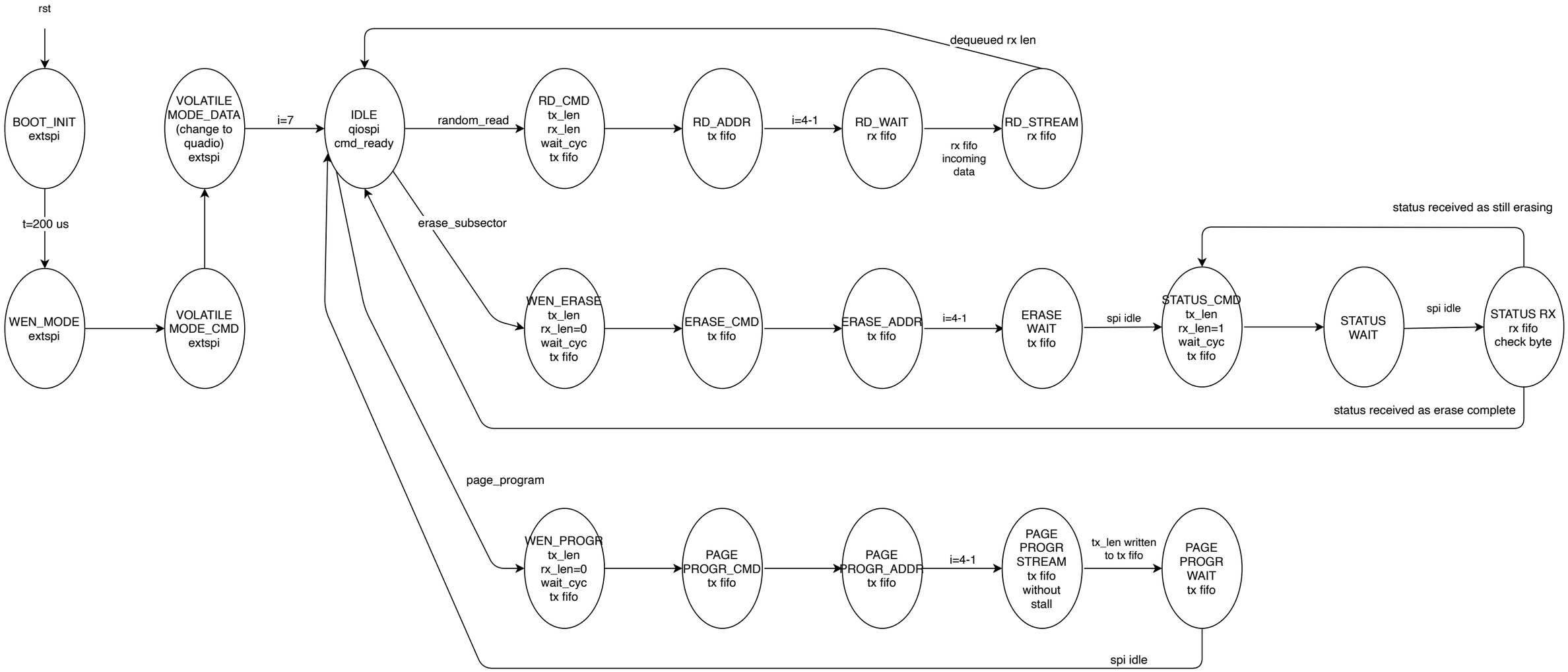
A top-level experiment design to provide a FSM with UI to control pattern write/read testing of PMOD SF3.
With this FSM, there are 32 groups of 32 sectors a piece.

Refer to project source code for more details of the FSM.
This drawing is a simplified conceptual representation of a more complex machine.

Display 16x2 :

```
SF3 PA hADDRESS_
ERS ERR 67108864
```

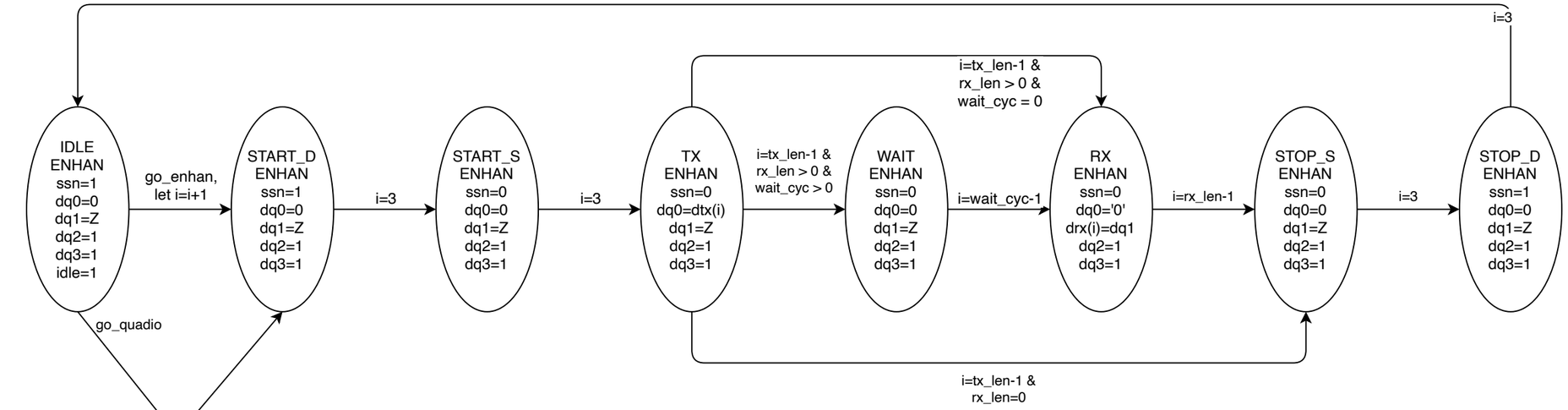
SF3 is SF3
PA = P* or PA or PB or PC or PD
hADDRESS = h00100000
ERS = GO_ or ERS or PRO or TST or END
ERR is ERR
67108864 is decimal in range 00000000 to 67108864



In each transition, tx_len and rx_len are to be multiplied by 8 from the FSM input signals,
as it only makes sense to input into the FSM a byte count, while the FSM requires transitioning
based upon a bit count.

N25Q chip FSM for communicating wtih the SPI Machine, with the N25Q as only SPI slave on the bus.

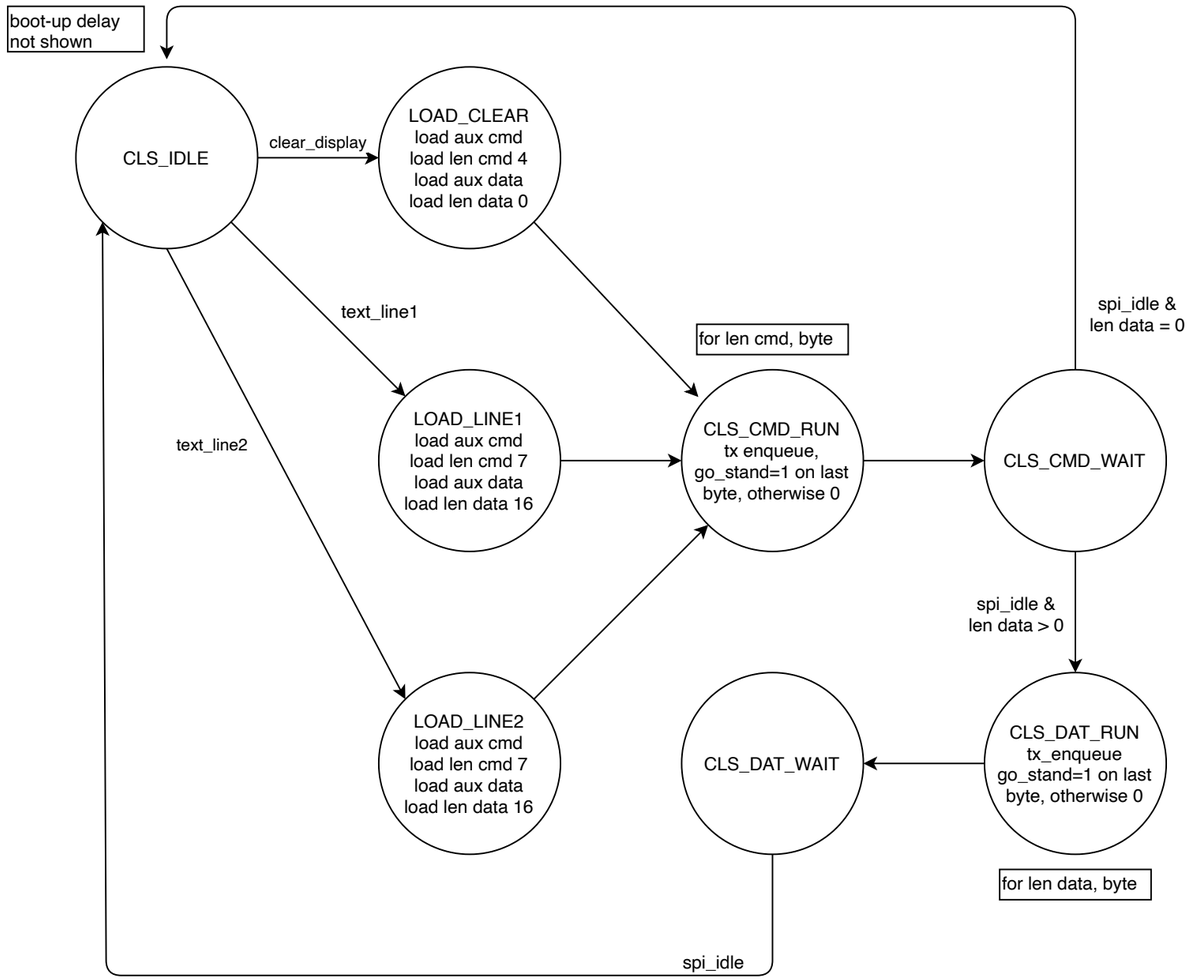
Refer to project source code for more details of the FSM.
This drawing is a simplified conceptual representation of a more complex machine.



In each transition, tx_len and rx_len are to be multiplied by 8 from the FSM input signals,
as it only makes sense to input into the FSM a byte count, while the FSM requires transitioning
based upon a bit count.

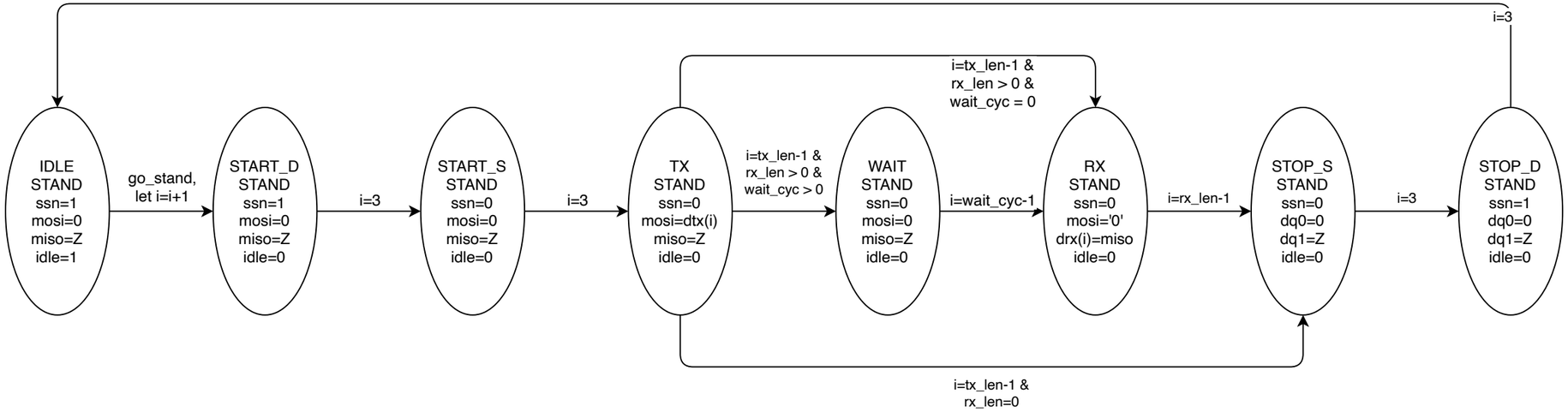
Generic SPI FSM, with the only one SPI slave on the bus.

Refer to project source code for more details of the FSM.
This drawing is a simplified conceptual representation of a more complex machine.
Note that this drawing indicates operation of either Extended SPI or Quad IO SPI.
The source code only implemented Extended SPI due to the Quad IO for N25Q
requiring some transmission parts to only output data on MOSI and other parts
to be output using all four bits. This diagram shows the original design intent, but
ony Extended SPI was implemented. In other words, this diagram is incorrect.



A FSM to operate the Digilent Inc. PMOD CLS LCD display communication to via the Standard SPI-machine FSM.

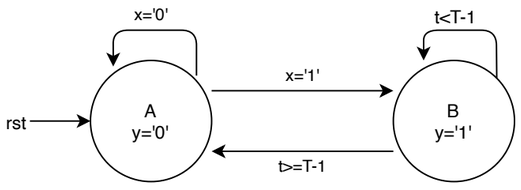
Refer to project source code for more details of the FSM.
This drawing is a simplified representation of a more complex machine.



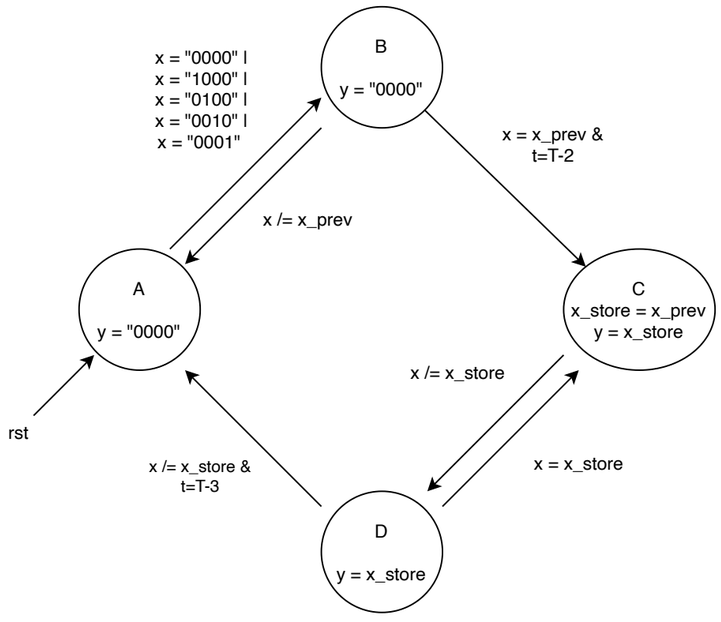
In each transition, tx_len and rx_len are to be multiplied by 8 from the FSM input signals,
as it only makes sense to input into the FSM a byte count, while the FSM requires transitioning
based upon a bit count.

Generic SPI FSM, with only one SPI slave on the bus.

Refer to project source code for more details of the FSM.
This drawing is a simplified representation of a more complex machine
that depends on a clock enable input that is 4 times the rate of the
generated SPI SCK output.



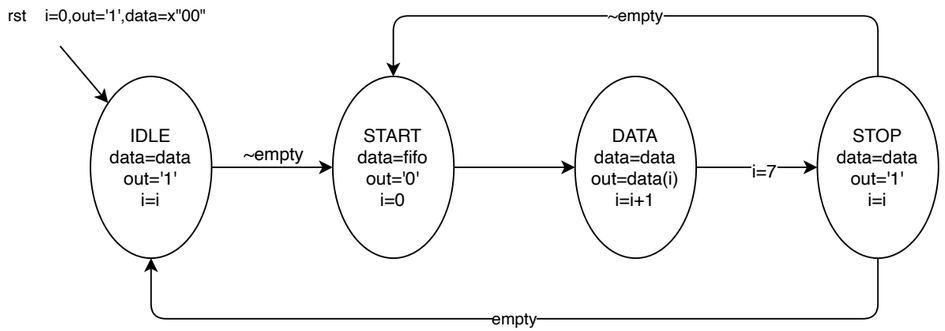
Moore FSM for a synchronous pulse stretcher of signal X that lasts for a duration less than T, with Y lasting exactly T cycles.



Full 4-button combined debouncer.

x is defined as a four-bit value.
x_prev is defined as a four-bit value that holds the previous clock cycle value of x.
x_store is defined as a four-bit value that holds the value of x and updates the
debouncer FSM entered state C during the transition BC..

The registers x_prev and x_store could be combined into one register, with its capture of X
being a clock-enable during transitions and states of a more complex diagram.



A TX ONLY UART output to UART chip from the FPGA, with the FSM executing at BAUD rate as its clock.

Refer to project source code for more details of the FSM.
This drawing is a simplified representation of a more complex machine.