CprE 381, Computer Organization and Assembly Level Programming

Team Contract – Project Part 1

Project Teams Group: ___4_4_____

Team Members: _____Ben Towle_____

_____Lalith_Vattyam_____

_____Gabe Carlson_____

Discuss the following aspects of teamwork with your team – make sure to get input from each member. Write down your team's consensus for each of the bolded headings. Italicized text contains instructions and examples and should be deleted once you've read it. Please see the example contract for rough length expectations.

Course Goals: *List and acknowledge the goals of your individual team members.*

- *Finish project on time*
- *Familiarize myself with Gitlab*
- *Learn how high-level components connected together to form a single cycle MIPS processor*
- *Work efficiently with group while following specified roles*
- *Learn enough about computer architecture to have basic understanding and conversations*
- *Efficiency with VHDL*

Team Expectations:

- **Conduct:** *What are the expectations for personal conduct of group members?*
  - Complete assigned tasks on time or communicate delays with group
  - Be respectful even if code takes a couple of times to get correct
  - Be accountable for your responsibilities
  - Don't push non compilable code to gitlab
- **Communication:** *What is the best mode of communication for the group? How often should communication occur? How fast should a response be expected?*
  - *Snapchat group for main method of communication*
  - *Secondary method of communication will be Microsoft Teams*
  - *Tertiary method of communication will be email*
  - *Expected response time should be less than 2 hours in general*
  - *Every day, especially when components are finished and ready for testing*

- **Group conventions:** *Naming conventions? Compilation and simulation methodology? Testbench strategies? Do file usage? Version control strategies? Commenting standards?*

    - *Make sure naming of signals, components, etc. are consistent and easy to understand.*
    - *Testbenches should be the same name as file name with tb_<fileName> leading it (Ex. adder.vhd -> tb_adder.vhd)*
    - *We will be using gitlab for our version control*
    - *Commenting every line isn't necessary, however commenting major points or groupings is needed.*
    - *Each testbench should have a do file*

- **Meetings:** *Given the significant portion of the course that the lab covers, it is expected that your team will spend more time working on the labs than in your scheduled lab sections. How will your group expect to handle this? Please include at least two additional times outside of lab that your team can meet (preferably in-person). Examples of other issues to consider include:*
    - *Work together in-person outside of lab sections?*
        - *Sundays: 2-5pm*
        - *Tuesdays: 2-5pm*
        - *Thursday: 4-7/8pm*
    - *Work together online outside of lab sections?*
        - *Work around individual schedules: Make sure to communicate changes through commit messages, snapchat, etc.*
    - *Work separately on responsibilities?*
        - *Independently, as long as we are communicating with one another*
- **Peer Evaluation Criteria:** *Please create a brief criteria for how effort and contribution are defined. Note that teams with **vastly** divergent scores may require a meeting with course instructor and result in different grades for different group members. Teams with reasonably equitable scores will receive the same grade.*
    - *Effective Communication*
    - *Meeting attendance*
    - *Overall contributions should be relatively equally distributed*
    - *Take ownership for individual assignments*

Role Responsibilities: *Complete the following planning table. Each lab part should be the responsibility of one team member. Also make sure that no one team member is the lead on both the design and test aspects of a single lab part. These guidelines aid in all students having a complete view of the lab. Note that the non-lead is encouraged to participate and support the lead wherever possible, increasing both the quality of the lab part and each team member's knowledge.*

Lab Part	Estimated Time	Design		Test	
		Lead	Timeline	Lead	Timeline
High-level design	1 hr	Ben	Before end of project	Lalith	Before end of project
Test programs	4 hr	Gabe	Before end of project	Lalith	Before end of project
Control logic	2 hr	All	10/5/23	All	10/523
Fetch logic	3 hr	All	10/5/23	All	10/5/23
Barrel shifter	2 hr	Gabe	10/5/23	Ben	10/5/23
ALU integration + Misc updates	2 hr	Ben	10/5/23	Gabe	10/5/23
High-level integration	4 hr	Lalith	Before end of project	Ben	Before end of project
Synthesis (human effort)	1.5 hr	Lalith	Before end of project	Gabe	Before end of project

*Estimated Time is given as a **very rough** guide for even distribution of tasks assuming you've already read through the lab document and have the prerequisite knowledge. Depending on your group's skill and prerequisite knowledge, some tasks may take disproportionately long or short. For your future planning, track this – for future prelabs you will be asked to note why past tasks took longer than expected and how you might avoid such issues in the future.*

Integrity of Work: *Do not delete the following.* We agree that the work we provide to other team members and ultimately submit for a grade is a direct result of our own work as described in the course syllabus. Specifically, we will generate all VHDL code ourselves and not copy VHDL code from online sources, other groups, book companion material, or past student projects to which anyone outside of my team has contributed.

Student Signature Benjamin Towle **Date** 09/28/23

Student Signature Lalith Vattyam **Date** 09/28/23

Student Signature Gabriel Carlson **Date** 09/28/23