COMPLEXITIES OF LAYOUTS
IN THREE-DIMENSIONAL VLSI CIRCUITS

Mokhtar A. Aboelaze and Benjamin W. Wah

Department of Electrical and Computer Engineering

and the Coordinated Science Laboratory

University of Illinois at Urbana-Champaign

Urbana Illinois 61801

ABSTRACT

Recent advances in Very-Large-Scale-Integration (VLSI) fabrication technologies have demonstrated the feasibility of three-dimensional (3-D) circuits in a single chip. Due to the ability and flexibility to connect non-adjacent circuits using the third dimension, the cost of mapping non-planar circuits to two-dimensional (2-D) systems can be reduced. In this paper, we examine the complexities in volume and maximum wire length of mapping circuits represented as undirected graphs to 3-D systems. Tighter bounds than those previously known are shown for various families of graphs, in both the one-active-layer and the unrestricted layouts.

1. INTRODUCTION

Recently, 3-D VLSI circuits have been shown to be feasible. 3-D VLSI circuits are more flexible than their corresponding 2-D counterparts because wire routing is easier and more systematic, the runs of wires are shorter, and the volume of a 3-D realization may be less [16]. Dr. Gibbons, the president of Texas Instruments, predicted the feasibility of such chips in the earlier 1990s [4]. Examples of current implementations include IBM's "modestly" three-dimensional Thermal Conduction Module (TCM) circuit package [3] and Hughes' 32-by-32 3-D cellular computer to be finished in 1987 [12].

In this paper, we show improved bounds on volume and maximum wire length of 3-D layouts, in both the one-active-layer and unrestricted models. The model used here is an extension of Thompson's 2-D model into three dimensions [17]. The model consists of a 3-D grid of width W, length L, and height H, respectively. A vertex in this grid, (x, y, z), where $0 \leq x \leq W$, $0 \leq y \leq L$, and $0 \leq z \leq H$, denotes the location where devices can reside. An edge in the grid represents a wire in the circuit. It is assumed that three mutually perpendicular lines in the grid can pass through one point without physically touching each other. It is further assumed that any active device will require a unit volume, that the cross section of a wire is a unit area, and that the separation between the wires in any direction is of unit length. These assumptions are not over-restrictive as we are evaluating the order-of-magnitude asymptotic complexities. To map a graph into the grid is to find a one-to-one mapping between the vertices of the graph and the vertices of the grid, together with a one-to-one mapping between the edges of the graph and the set of disjoint paths of the grid.

Rosenberg proposed two models of 3-D layouts [15, 16]. The first model is the one-active-layer model in which active devices are allowed to reside in only one layer, and the other layers will be used for the routing of wires. The second model is the unrestricted model in which active devices can be placed

anywhere in the volume.

Rosenberg also proposed layouts for the rearrangeable permutation network which take $\Theta(n^{3/2})$ and $\Theta(n^{3/2}\log n)$ volume in the one-active-layer and the unrestricted layouts, respectively [15, 16]. Preparata proposed a layout for the cube-connected-cycles in 3-D VLSI [14]. Leighton and Rosenberg have found lower and upper bounds for the layout of various families of undirected graphs [7, 10].

2. LOWER BOUNDS ON VOLUME AND MAXIMUM WIRE LENGTH

In this section, we develop improved lower bounds for the various families of undirected graphs in the one-active-layer model. We did not find any improvement in lower bounds for the unrestricted model because the existing lower bounds [16, 10, 8] will be shown to be tight except for the family of graphs with $\Theta(n^{2/3})$ separator.

In the following theorem, the mesh of trees is considered as an example in the family of graphs with $\Theta(\sqrt{N})$ separator, while the tree of meshes is considered as an example in the family of planar graphs. These two example graphs were used by Leighton in proving the lower bound of 2-D layouts [5, 9].

Theorem 1: (a) Any 3-D one-active-layer layout of the mesh of trees will require $\Omega(N \log N)$ volume and $\Omega(\sqrt{N} / \log \log N)$ maximum wire length. (b) Any 3-D one-active-layer layout of the tree of meshes will require $\Omega(N \sqrt{\log N})$ volume and $\Omega(\sqrt{N} / \log N)$ maximum wire length.

Proof: We will prove these lower bounds by contradiction. Leighton proved that any 2-D layout of the N-node mesh of trees will require $\Omega(N \log^2 N)$ area, and that this layout must have $\Omega(\sqrt{N} \log N / \log \log N)$ maximum wire length [9]. He also proved that any 2-D layout of the N-node tree of meshes will require $\Omega(N \log N)$ area, and that this layout must have $\Omega(\sqrt{N} / \sqrt{\log N})$ maximum wire length. Leighton and Rosenberg proved that any 3-D layout of volume V, base area B, and height H can be transformed into a 2-D layout of area $A = 9BH^2 = O(BH^2)$ [10]. Further, if the maximum wire length in the 3-D layout is W_M, then the upper-bound maximum wire length in the 2-D layout is $W_{2d} = O(HW_M)$. We have found that the area required is $4BH^2$ instead of $9BH^2$ and that the degree of the graph can be six instead of four. Due to space limitation, the proof will not be shown here [1].

For the mesh of trees, let us assume the existence of a 3-D one-active-layer layout with a volume $V < \Theta(N \log N)$ and maximum wire length $W < \Theta(\sqrt{N} / \log \log N)$. The base area of this one-active-layer layout should be $\Omega(N)$, as it should be large enough to accommodate the N nodes of the graph. Therefore, the height of this layout is $H < \Theta(\log N)$. According to

† Θ indicates the set of functions with the same order-of-magnitude complexity; O indicates the set of functions with the upper-bound order-of-magnitude complexity; Ω indicates the set of functions with the lower-bound order-of-magnitude complexity.

Leighton and Rosenberg's results [10], this 3-D circuit can be transformed into a 2-D layout with area $A < \Theta(N \log^2 N)$ and maximum wire length $W_{2d} < \Theta(\sqrt{N} \log N / \log \log N)$, which contradict Leighton's results [9]. Thus, any 3-D one-active-layer layout of the mesh of trees will require $\Omega(N \log N)$ volume and $\Omega(\sqrt{N} / \log \log N)$ maximum wire length.

For the tree of meshes, assume the existence of a 3-D one-active-layer layout with volume $V < \Theta(N \sqrt{\log N})$ and maximum wire length $W < \Theta(\sqrt{N} / \log N)$. Since the base of this layout should have $\Omega(N)$ area, the height of this layout is $H < \Theta(\sqrt{\log N})$. Using Leighton and Rosenberg's results [10], we can transform this layout into a 2-D layout with area $A < \Theta(N \log N)$ and maximum wire length $W_{2d} < \Theta(\sqrt{N} / \sqrt{\log N})$, which contradict Leighton's results. Hence, any 3-D one-active-layer layout of the trees of meshes should have $\Omega(N \sqrt{\log N})$ volume and $\Omega(\sqrt{N} / \log N)$ maximum wire length. □

The upper-bound volume of the family of undirected graphs with $\Theta(N^q)$ separator, $1/2 < q \leqslant 1$, will be shown in Section 3.1 to be $O(N^{q+1/2})$. As the base area has $\Omega(N)$ complexity, the height of this layout has $O(N^{q-1/2})$ complexity. Leighton has proved the lower-bound maximum wire length for the family of undirected graphs with $\Theta(N^q)$ separator, $1/2 < q \leqslant 1$, in a 2-D layout to be $\Omega(N^q)$ [9]. From Leighton and Rosenberg's results [10], the maximum wire length in the 3-D one-active-layer layout should be $W_{2d} / H = \Omega(N^q / N^{q-1/2}) = \Omega(\sqrt{N})$.

For the family of graphs with $\Theta(N^q)$, $0 \leqslant q < 1/2$, separator, Paterson, Ruzzo, and Snyder have proved the lower-bound maximum wire length in a 2-D layout of a binary tree to be $\Omega(\sqrt{N} / \log N)$ [13]. In a one-active-layer 3-D layout, a similar argument can be made such that nodes of a binary tree are in one layer, and that the maximum distance between two nodes separated by $2 \log N$ edges is $\Omega(\sqrt{N})$. Hence, the lower bound in the 3-D case is the same as that of the 2-D case.

Table 1 summarizes the lower bounds obtained for the one-active-layer layout and compares them with previously known results.

3. UPPER BOUNDS

Before introducing the results on upper bounds, we review the necessary mathematical background behind the theory of layouts. Thompson introduced the idea of the minimum bisection width of an undirected graph and proved a relation between the minimum bisection width and the minimum area required to lay out the given graph [17]. Lipton and Tarjan introduced the idea of separator for a family of undirected graphs and proved that the family of planar graphs has a $O(\sqrt{N})$ separator [11]. They also proposed a linear-time algorithm to compute this separator. Bhatt and Leighton introduced the ideas of bifurcators and decomposition trees [2]. An N-node undirected graph has (F, α) bifurcator if it can be decomposed into two subgraphs.

Graph Separator $f(N)$	Volume		Maximum Wire Length	
	Previous	New	Previous	New
$\Theta(N^q)$, $0 \leqslant q < 1/2$	$\Omega(N)$ [10]	$\Omega(N)$ [10]	constant [10]	$\Omega(\sqrt{N} / \log N)$ [13]
Planar	$\Omega(N)$ [10]	$\Omega(N \sqrt{\log N})$	constant [10]	$\Omega(\sqrt{N} / \log N)$
$\Theta(\sqrt{N})$	$\Omega(N)$ [10]	$\Omega(N \log N)$	constant [10]	$\Omega(\sqrt{N} / \log \log N)$
$\Theta(N^q)$, $1/2 < q \leqslant 1$	$\Omega(N^{q+1/2})$ [10, 16]	$\Omega(N^{q+1/2})$ [10, 16]	$\Omega(N^{q-1/2})$ [10]	$\Omega(\sqrt{N})$

Table 1. Lower bounds on volume and maximum wire length for the one-active-layer model. (Note that a lower bound is intended to mean the largest known lower bound for a graph in the given family.)

G_1 and G_2, by removing no more than F edges. Both G_1 and G_2 can further be decomposed into two subgraphs by removing no more than F/α edges. In general, any subgraph in level i can be decomposed into two subgraphs by removing no more than F/α^i edges.

A decomposition tree is said to be a fully balanced decomposition tree if (a) when decomposing any subgraph into two smaller subgraphs, the number of nodes in the two smaller subgraphs are equal; and (b) when decomposing any subgraph into two smaller ones, the number of edges connecting this subgraph to the rest of the original graph is divided into two equal sets that are distributed in the two decomposed subgraphs. Bhatt and Leighton also proved that any graph with (F, α) bifurcator has a fully balanced decomposition tree with (F', α) bifurcator, where F' is related to F by a constant [6].

3.1. One-Active-Layer Layouts

In the following theorem, the upper bounds for graphs with $\Theta(\sqrt{N})$ separator are proved. The family of planar graphs is treated in the same way as the family of graphs with $\Theta(\sqrt{N})$ separator here. Although Leighton and Rosenberg have proved the same bounds before, they have assumed in their proof the existence of a layout of an n-node subgraph in which the ports of this subgraph "are sufficiently sparse that the routing is guaranteed to be possible" [10]. We will assume in the following proof that the ports of a subgraph are equally spaced along one side of its layout. In connecting two n-node subgraphs into a 2n-node subgraph, a complete crossbar switch will be used to perform the routing, and the ports in the resulting subgraph will also be equally spaced along one side of the resulting layout. The above model allows us to prove a better upper bound on volume for the family of graphs with $\Theta(N^q)$, $1/2 < q \leqslant 1$, separator. This will be shown in Theorem 3.

Theorem 2: Any undirected graph with $\Theta(\sqrt{N})$ separator has a 3-D one-active-layer layout with $O(N \log N)$ volume and $O(\sqrt{N})$ maximum wire length.

Proof: We assume that the balanced decomposition tree of the graph is known. The proof is by induction on a graph with n nodes. The case for n=1 is trivial. For the induction hypothesis, assume that an n-node graph can be mapped into a parallelepiped with volume $V(n)$, height $H(n)$, and a square base of side $L(n) = kc \sqrt{n}$, where k is a constant. It is further assumed that the $c \sqrt{n}$ ports to connect any node in this subgraph to another node outside this subgraph are aligned and equally spaced along one side of the top layer of this layout (see Figure 1, where the ports are represented by circles). In the induction step, consider the volume needed to lay out four n-node subgraphs. We will combine these four layouts to produce one 4n-node layout with volume $V(4n)$, height $H(4n)$, a square base of side $L(4n) = kc \sqrt{4n}$, and that the $c \sqrt{4n}$ ports of the 4n-node subgraph are aligned and equally spaced along one side of the top layer. This will be done by first showing that one additional layer is needed to accommodate the necessary interconnections when two n-node subgraph layouts are combined to form one 2n-node subgraph layout.

Consider two n-node layouts placed side by side as shown in Figure 1. We have (a) to create $c \sqrt{2n}$ ports in the 2n-node subgraph layout; and (b) to connect a maximum of $c \sqrt{n}$ ports in one of the n-node subgraphs to a maximum of $c \sqrt{n}$ ports in the other n-node subgraph. Since we have assumed that the subgraph has a balanced decomposition tree, half of the $c \sqrt{2n}$ ports in the combined layout will be connected to ports in the first layout, while the other half will be connected to ports in the second layout. It is not hard to prove that if $k \geqslant 2$ one layer is enough to create a complete crossbar switch to perform the required routing. Since one layer is added to combine to n-node layout together, the height can be calculated from the following recurrence.

$$H(2n) = \begin{cases} H(n) + 1 & n > 1 \\ 1 & n \leqslant 1 \end{cases} \quad (4)$$
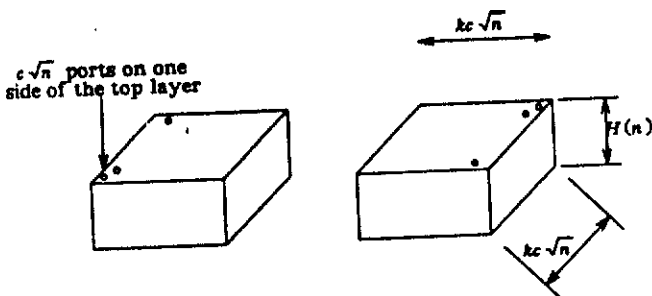
c √n ports on one
side of the top layer

Figure 1. Two n-node subgraph layouts with $\Theta(\sqrt{n})$ separator. (The $c\sqrt{n}$ ports of each layout are represented as circles and are aligned on one side of the top layer.)

Similarly, we can combine two 2n-node subgraph layouts to form one 4n-node subgraph layout. In general, for an N-node subgraph layout, where N is a power of two,

$$H(N) = \log N. \tag{5}$$

Since the base area of an N-node layout is $(kc\sqrt{N})^2$, the total volume will be

$$V_{1AL}(N) = k^2 c^2 N \log N = O(N \log N) \tag{6}$$

In computing the volume, no constraint is put on the routing of wires, hence, a wire can run along the $\log N$ layers in a zig-zag fashion in the worst case. The maximum wire length is

$$W_{1AL}(N) = O\left[2\sum_{i=0}^{\log_2 N} kc\sqrt{\frac{N}{2^i}}\right] = O(\sqrt{N}) \tag{7}$$

According to the theory of induction, the theorem is proved. □

Theorem 3: Any undirected graph with $\Theta(N^q)$ separator, $1/2 < q \leqslant 1$, has a 3-D one-active-layer layout with $O(N^{q+1/2})$ volume and $O(\sqrt{N})$ maximum wire length.
Proof: The proof is similar to that of Theorem 2 except that cn^q edges connect any n-node subgraph to the rest of the graph. Due to space limitation, the proof will not be shown here [1]. □

Note that the upper bounds on volume and maximum wire length are optimal because they are the same as the corresponding lower bounds (see Table 1). □

Table 2 shows the upper bounds in the one-active-layer model and compares them against previously known results [8, 10]. Note that the upper bounds on volume are tight in all cases except for the family of planar graphs.

3.2. Unrestricted Layouts

Theorem 4: Any undirected graph with $\Theta(N^q)$ separator, $0 \leqslant q \leqslant 1$, has a 3-D unrestricted layout with volume

$$V(N) = \begin{cases} O(N) & 0 \leqslant q < 2/3 \\ O(N \log^3 N) & q = 2/3 \\ O(N^{3q/2}) & 2/3 < q \leqslant 1 \end{cases} \tag{8}$$

with maximum wire length

$$W(N) = \begin{cases} O(N^{1/3}) & 0 \leqslant q < 2/3 \\ O(N^{1/3}\log N) & q = 2/3 \\ O(N^{q/2}) & 2/3 < q \leqslant 1 \end{cases} \tag{9}$$

Proof: We assume that the balanced decomposition tree of the graph is known. The proof is by induction on a graph with n nodes. The case for n=1 is trivial. For the induction hypothesis, assume that an n-node layout is in the form of a cube. Further, assume that the cn^q ports of this layout are arranged in the form of a square with side $k\sqrt{cn^q}$ in one of the faces of the cube, where k is a constant. In the induction step, we will show that eight n-node subgraphs can be combined into one 8n-node

Graph Separator $f(N)$	Volume		Maximum Wire Length	
	Previous	New	Previous	New
$\Theta(N^q)$, $0 \leqslant q < 1/2$	$O(N)$ [10]	$O(N)$ [10]	$O(\sqrt{N}/\log N)$ [10]	$O(\sqrt{N}/\log N)$ [10]
Planar	$O(N \log N)$ [10]	$O(N \log N)$	$O(\sqrt{N})$ [10]	$O(\sqrt{N})$
$\Theta(\sqrt{N})$	$O(N \log N)$ [10]	$O(N \log N)$	$O(\sqrt{N})$ [10]	$O(\sqrt{N})$
$\Theta(N^q)$, $1/2 < q \leqslant 1$	$O(N^{q+1/2} \log N)$ [10]	$O(N^{q+1/2})$	$O(\sqrt{N})$ [10]	$O(\sqrt{N})$

Table 2. Upper-bound volume and maximum wire length for the 3-D one-active-layer layouts. (The previous and new results may be the same but obtained by different methods.)

layout in the form of a cube, and the $c(8n)^q$ ports of this layout are arranged in the form of a square of side $k\sqrt{c(8n)^q}$.

The induction step is proved by first arranging the eight n-node layouts in the corners of a larger cube, such that ports of the four upper cubes are directed downwards, while ports of the four lower cubes are directed upwards (see Figure 2). We will first combine two n-node subgraph layouts to form one 2n-node layout. We have (a) to create $c(2n)^q$ new ports for the 2n-node layout; and (b) to connect the ports in the two n-node layouts. Figure 3 shows the $2(cn^q)$ ports of the upper and lower layouts, each in the form of a square with side $k\sqrt{cn^q}$, where k is a constant. By adding $2^q k\sqrt{cn^q}$ layers between the upper and lower
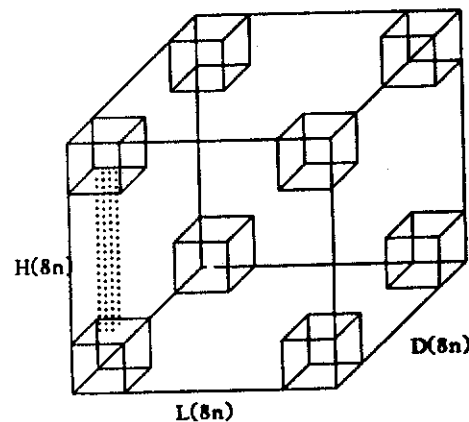

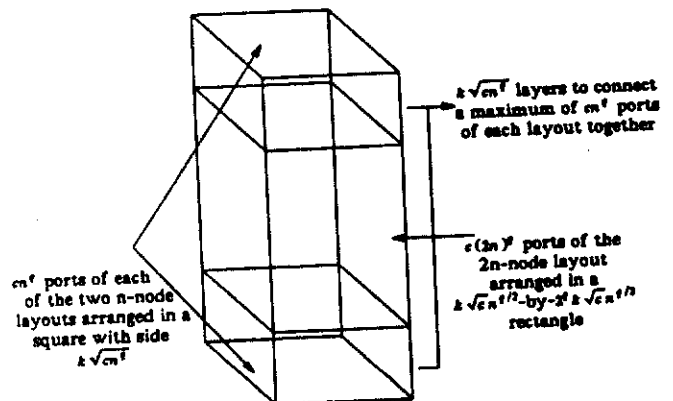Figure 2. Combining eight n-node layouts to form one 8n-node layout.

Figure 3. Combining two n-node layouts to form one 2n-node layout in the unrestricted model.

545

cubes in Figure 3, we can create a complete 3-D crossbar switch to perform the necessary routing between the newly created $c(2n)^q$ ports and any of the $2cn^q$ ports in the two original n-node layouts. The newly created $c(2n)^q$ ports are arranged in the form of a rectangle of length $k\sqrt{cn^q}$ and width $2^q k\sqrt{cn^q}$. To perform the necessary connections between the two n-node subgraph layouts, each with a maximum of cn^q ports, another complete 3-D crossbar switch with $k\sqrt{cn^q}$ layers is created between the upper and lower layouts in Figure 3.

In a similar way, we can combine four $2n$-node layouts to form two $4n$-node layouts and two $4n$-node layouts into one $8n$-node layout. In each case, we have added $\Theta(\sqrt{cn^q})$ layers between the two layouts concerned. The height, length, and width of the $8n$-node layout can be computed from the following recurrences.

$$H(8n) = \begin{cases} 2H(n) + k_1\sqrt{cn^q} & n > 1 \\ 1 & n = 1 \end{cases} \quad (10)$$

$$L(8n) = \begin{cases} 2L(n) + k_2\sqrt{cn^q} & n > 1 \\ 1 & n = 1 \end{cases} \quad (11)$$

$$D(8n) = \begin{cases} 2D(n) + k_3\sqrt{cn^q} & n > 1 \\ 1 & n = 1 \end{cases} \quad (12)$$

where k_1, k_2, and k_3 are constants. Solving the last three equations, we get

$$D(N)=L(N)=H(N)= \begin{cases} O(N^{1/3}) & 0 \leq q < 2/3 \\ O(N^{1/3}\log N) & q = 2/3 \\ O(N^{q/2}) & 2/3 < q \leq 1. \end{cases} \quad (13)$$

The volume of the layout will be

$$V(N) = \begin{cases} O(N) & 0 \leq q < 2/3 \\ O(N\log^3 N) & q = 2/3 \\ O(N^{3q/2}) & 2/3 < q \leq 1. \end{cases} \quad (14)$$

For the maximum wire length, note that the maximum wire length of the $8n$-node layout is equal to the maximum wire length of the n-node layout plus $\alpha L(8n)$, where $L(8n)$ is the length of each side of the $8n$-node layout, and α is a constant. (Due to the crossbar connection, we did not extend any port more than a length of $\alpha L(8n)$). The maximum wire length can be computed from the following recurrence.

$$W(8n) = W(n) + \alpha L(8N). \quad (15)$$

Substituting L from Eq. (13),

$$W(N) = \begin{cases} O(N^{1/3}) & 0 \leq q < 2/3 \\ O(N^{1/3}\log N) & q = 2/3 \\ O(N^{q/2}) & 2/3 < q \leq 1. \end{cases} \quad (16)$$

According to the theory of induction, the theorem is proved. □

Table 3 shows the upper bounds obtained here for the volume and maximum wire length, respectively, and compares them with previously known results [7, 10, 8]. Note that all the upper bounds on volume obtained here are optimal except for the family of graphs with separator $\Theta(n^{2/3})$

REFERENCES

[1] M. Aboelaze and B. W. Wah, Complexities of Layouts in Three-Dimensional VLSI Circuits. Computer Systems Group, Tech. Rep. #63, Coordinated Science Laboratory, University of Illinois at Urbana-Champaign, Jan. 1987.

[2] S. N. Bhatt and F. T. Leighton, "A Framework for Solving VLSI Graph Layout Problems," *J. of Computer and System Sciences*, vol. 28, pp. 300-343, 1984.

[3] A. J. Blodgett and D. R. Barbour, "Thermal Conduction Module: A High-Performance Multilayer Ceramic Pack-

age," *IBM J. of Research and Development*, vol. 26, no. 1, pp. 30-36, Jan. 1982.

[4] J. F. Gibbons, "SOI—A Candidate for VLSI?," *VLSI Design*, vol. 3, pp. 54-55, 1982.

[5] F. T. Leighton, "New Lower Bounds Techniques for VLSI," *Proc. 22nd Annual IEEE Symposium on Foundation of Computer Science*, pp. 1-12, Oct. 1981.

[6] F. T. Leighton, *Complexity Issues in VLSI*, Foundations in Computing Series, M.I.T. Press, Cambridge, Mass., 1983.

[7] F. T. Leighton and A. L. Rosenberg, "Automatic Generation of Three-Dimensional Circuit Layouts," *IEEE Int'l Conf. on Computer Design: VLSI in Computers*, pp. 633-636, 1983.

[8] F. T. Leighton and A. Rosenberg, *Three-Dimensional Circuits Layouts*, Tech. Rep. MIT/LCS/TM-262, MIT, June 1984.

[9] F. T. Leighton, "New Lower Bounds for VLSI," *Mathematical Systems Theory*, pp. 47-70, 1984.

[10] F. T. Leighton and A. L. Rosenberg, "Three-Dimensional Circuit Layout," *SIAM J. on Computing*, vol. 15, pp. 793-813, Aug. 1986.

[11] R. J. Lipton and R. E. Tarjan, "A Separator Theorem for Planar Graphs," *Conference on Theoretical Computer Science*, pp. 1-10, U. of Waterloo, Waterloo, Canada, Aug. 1977.

[12] G. R. Nudd, R. D. Etchells, and Jan Grinberg, "Three-Dimensional VLSI Architecture for Image Understanding," *J. Parallel and Distributed Computing*, vol. 2, pp. 1-29, Feb. 1985.

[13] M. S. Paterson, W. L. Ruzzo, and L. Snyder, "Bounds on Minimax Edge Length for Complete Binary Trees," *Proc. 13th Annual Symposium on Theory of Computing*, pp. 293-299, ACM, Milwaukee, WI, 1981.

[14] F. P. Preparata, "Optimal Three-Dimensional VLSI Layouts," *Mathematical System Theory*, vol. 16, pp. 1-8, Jan. 1983.

[15] A. L. Rosenberg, "Three-dimensional Integrated Circuits," in *VLSI Systems and Computations*, ed. H. T. Kung, B. Sproull, and G. Steele, pp. 69-80, Computer Science Press, Rockville, MD., 1981.

[16] A. L. Rosenberg, "Three-Dimensional VLSI: A Case Study," *J. of the ACM*, vol. 30, no. 3, pp. 397-416, July 1983.

[17] C. D. Thompson, A Complexity Theory for VLSI, Ph.D. Dissertation, Dept. Computer Science, Carnegie-Mellon University, Pittsburgh, PA, 1980.

Graph Separator $f(N)$	Volume		Maximum Wire Length	
	Previous	New	Previous	New
$\Theta(N^q)$, $0 \leq q < 1/2$	$O(N)$	$O(N)$	$O(N^{1/3})$	$O(N^{1/3})$
Planar	$O(N\log^{3/2}N)$	$O(N)$	$O(N^{1/3}\sqrt{\log N})$	$O(N^{1/3})$
$\Theta(\sqrt{N})$	$O(N\log^{3/2}N)$	$O(N)$	$O(N^{1/3}\sqrt{\log N})$	$O(N^{1/3})$
$\Theta(N^q)$, $1/2 < q < 2/3$	$O(N^{q+1/2}\log^{3/2}N)$	$O(N)$	$O(N^{q/3+1/6}\sqrt{\log N})$	$O(N^{1/3})$
$\Theta(N^{2/3})$	$O(N^{7/6}\log^{3/2}N)$	$O(N\log^3 N)$	$O(N^{7/18}\sqrt{\log N})$	$O(N^{1/18}\log N)$
$\Theta(N^q)$, $2/3 < q < 1$	$O(N^{q+1/2}\log^{3/2}N)$	$O(N^{3q/2})$	$O(N^{q/3+1/6}\sqrt{\log N})$	$O(N^{q/2})$

Table 4. Upper-bound volume and maximum wire length for the 3-D unrestricted layouts. (All previous bounds were derived by Leighton and Rosenberg [10]. The previous and new results may be the same but obtained by a different method.)