

searches as well as the equality and threshold searches, has been developed in [8].

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## Authors' Reply<sup>2</sup>

C. V. RAMAMOORTHY, J. L. TURNER,  
AND B. W. WAH

The idea on the design of cellular associative memories for ordered retrievals had occurred to one of us (Ramamoorthy) around 1970 when he was a consultant to Texas Instruments Incorporated. Subsequently, at his suggestion, the second author (Turner) at the University of Texas, Austin, explored and designed the system. The basic idea was also communicated to Dr. W. Litzler and Mr. Wes Wester of Texas Instruments and the thesis committee of Mr. Turner [4] around the same time. The second author's thesis [4] which was submitted in August 1972 and is available from the Library of the University of Texas at Austin, contains the basic designs and algorithms [4, pp. 14, 21, 32, 46] described in the paper. In 1975, the third author (Wah) improved and applied all the algorithms for associative searches based on database machine design principle. The current design also focuses on the use of associative memory for multiple response resolution.

It is unfortunate that we were not aware of the designs developed in Siberia, USSR due to the fact that several Russian documents are unavailable in the western world. A careful and thorough translation and reading of the documents sent by Dr. Fet makes us to come to the following conclusions. There seems to exist some similarities in some of the functions performed by his design. However, all the functions of Dr. Fet's cell, Turner's design, and the design presented in the paper have already been conceived in the pioneering work of Dr. W. H. Kautz in 1969 [2] (as well as in [7] of our paper). We also are not able to understand the complete design because Dr. Fet did not provide us with References [2], [3], and [7] of his comments which we did not have any access to. His design only considered the problem from a logic design point of view, but did not consider the implementation problem of asynchronous logic design. Furthermore, our design has focused on the simple but very important problem of resolving mul-

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C. V. Ramamoorthy is with the Computer Science Division, Department of Electrical Engineering and Computer Science, and the Electronics Research Laboratory, University of California, Berkeley, CA 94720.

J. L. Turner is with the National Semiconductor Corporation, Santa Clara, CA 95051.

B. W. Wah is with the School of Electrical Engineering, Purdue University, West Lafayette, IN 47907.

tiple responses in an associative memory which so far has been the stumbling block in the development of fast associative memories. Based on the later papers that Dr. Fet has sent us, since we do not have access to some of his earlier work, he does not seem to understand or attack the basic problem on multiple response resolution and does not have any explicit or implicit evidence on his part. It is also unfortunate that his work was not referenced in the extensive surveys of Parhami [3], nor the well known work and books of Prof. Caxton Foster on associative processors [1].

It is quite possible that similar, same, or better ideas have been developed in different parts of the world. The problem discussed here would not have happened if there are open cooperation and publication of research papers. It is hoped that in the future the communication channels can be improved so that researchers can cooperate on common ideas. Lastly, we consider Dr. Fet's ideas to be unique and we thank him for bringing his contributions to our attention.

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## A Remark on the Nonminimality of Certain Multiple Fault Detection Algorithms

WOLFGANG COY

**Abstract**—Poage has constructed a complex fault detection algorithm which generates a complete and minimal test set of all multiple stuck-at faults of a given combinational network. Several authors have derived from his method fast and simple multiple fault detection algorithms, which are claimed to generate complete test sets with a "near-minimal" or "near-optimal" number of tests. We show that the algorithms by Bossen and Hong and the algorithm by Yang and Yau may generate test sets with an exponential number of tests (relative to the number of inputs) where a linear number of tests is sufficient for a complete multiple fault detection test set.

**Index Terms**—Algorithms, cause-effect analysis, combinational networks, fault detection, fault functions, multiple stuck-at faults, test complexity, test pattern generation, redundant networks.

## I. INTRODUCTION

Several multiple stuck-at-fault detection algorithms [2]-[4] are based on a fault description model developed by Poage [1]. Poage's method uses an algebraic expression  $f(y_1, \dots, y_k)$  which describes the "state" (namely, stuck-at-0, stuck-at-1, or fault-free) of every line  $y_1, \dots, y_k$  of a given combinational circuit.

Assigning values to the "states" of  $y_1, \dots, y_k$  allows the description of every possible multiple stuck-at-fault in the circuit. By a complex computation it is possible to generate from this expression a complete test set with a minimal number of tests. Bossen and Hong [2] reduced this expression to an expression which covers only the "checkpoints" of the circuit. The resulting algebraic expression is also capable of modeling every possible multiple stuck-at-fault. Furthermore they have shown two simple and fast algorithms for the generation of complete test sets for general and for nonredundant circuits (algorithm *G* resp. *NR*). Algorithm *G* uses as input data only the functional

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The author is with the Department of Informatics, University of Dortmund, Dortmund, West Germany and the Faculty of Mathematics and Informatics, University of Bremen, Bremen, West Germany.