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TO: Mark IV Development Group

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SUBJECT: Mark IV correlator configurations to 128 complex lags

Mark 4 internal memo IM081 presented a set of three basic configurations for the processing of 32-complex lag continuum data. This memo expands these modes to add simultaneous auto-correlation capability, and also adds additional modes to expand to 128 complex lags.

Definitions

Figure 1 (reproduced and augmented from Mark IV memo 194) shows the high-level interconnection diagram of the Mark IV correlator as configured for the U.S.-developed version (i.e. no data distributor). The following definitional terms were agreed on:

Correlator 'Segment' - a set of four correlator boards in a correlator crate, each of which receive the same set of 64 channels of data. Each segment is served by one Input Board; each crate contains two segments. For purposes of discussion, the segments of the correlator are numbered 0-3, and the correlator boards within each segment are numbered 0-3, as indicated in Figure 1.

Correlator 'Slice' - the set of four correlator boards, one from each of four segments, which have the same correlator-board number. The slices are diagrammatically indicated on Figure 1. Note that, since each of the four correlator segments receives only four channels of data from each Station Unit, at least one 'slice' would be assigned in order to process all 16 channels simultaneously.

Figure 2 shows the schematic definition of a 'double-block', which is the minimum requirement for complex correlation:

'Double-block' - Consists of 2 out of the 8 'blocks' on a correlator chip, and is the typical configuration for continuum processing of a single baseline-channel. Four such double-blocks are resident on each chip. Each double-block can process 32 complex lags (with validity). As is indicated in Figure 2, the double-block is configured so that the X-data ('reference station') is rotated and a vernier-delay is applied to the Y-data ('remote station'). [Though rotators and vernier-delay controllers exist at both X and Y inputs, only the rotator is used for X and the vernier-delay for Y.]. The block at which the X signal is input is called the 'X-block'; the block at which the Y signal is input is called the 'Y-block'.

Note that both correlator blocks shown in Figure 2 are identical, however the cascade connections are not quite symmetric. This restricts the X input to always be the 'reference' station and Y the 'remote' station for complex correlation.

Configurations processing more than 32 complex lags require the insertion of 'mid-blocks' between the 'X-block' and the 'Y-block'. This is accommodated by on-chip switching to a maximum of 128 complex lags; beyond 128 complex lags it is necessary to cascade from chip to chip using the so-called 'cascade' inputs and outputs. This memo does not cover modes in which it is necessary to cascade from chip to chip.

32 Complex-Lag Processing Modes

Four basic operating modes, designated A32, B32 and C32, are available for 32 complex-lag processing. For each of these modes, it is assumed that all 16 channels available from each Station Unit are to be cross-correlated with all 16 channels from all other Station Units. These modes are summarized in Table 1 below:

	Scan Parameters			Correlator Configuration		
Mode	#stns	#base-lines	#chns/ station	#slices	hardware utilization	Comments
A32	16	120	16	4	100%	Complete 16-stn processing
B32	11	55	16	2	99%	Complete 11-stn processing
C32	8	28	16	1	100%	Complete 8-stn processing

Table 1: Mark IV correlator 32-complex-lag processing modes

Chip Configurations

In 32 complex-lag mode, each correlator chip will be configured to one of the three following modes:

1. Mode B7: '2x2 XX Complex Cross-correlation' mode (Appendix B7 of Mark4 memo 237), which has the correlation matrix shown in Table 2:

		Remote X2	Remote X3
Ref	X0	32C	32C
	X1	32C	32C

Table 2: Chip mode B7 (with validity/sample enabled)

2. Mode B13: '2x2 XX Complex Auto-correlation' mode (Appendix B13 of Mark4 memo 237), which has the correlation matrix shown in Table 3:

		Remote X0	Remote X1	Remote X2	Remote X3
Ref	X0	32R	32C	-	-
	X1	-	32R	-	-
	X2	-	-	32R	-
	X3	-	-	32C	32R

Table 3: Chip mode B13 (with validity/sample enabled)

3. Mode H1: See Figure 3 (attached), which has the correlation matrix shown in Table 4:

		Remote X0	X1	X2	X3
Ref	X0	-	32C	32C	-
	X1	-	32R	32C	-
	X2	-	-	-	-
	X3	-	-	-	32R

Table 4: Chip mode H1 (with validity/sample enabled)

(Note: Thanks to Will Aldrich for sleuthing out this mode.)

Mode A32

Mode A32 supports 16 stations of 16 channels each, with full auto-correlation. A single correlator board processes all 120 cross-correlation baselines plus 16 auto-correlations for a single channel. Table 5 suggests a possible assignment of correlator chips on a single correlator board. Each entry indicates the particular correlator-chip number to which the corresponding correlation should be assigned.

		Remote															
	Stn	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**
Ref	**0**	28	28	0	0	1	1	2	2	3	3	4	4	5	5	6	6
	1		28	0	0	1	1	2	2	3	3	4	4	5	5	6	6
	2			28	28	7	7	8	8	9	9	10	10	11	11	12	12
	3				28	7	7	8	8	9	9	10	10	11	11	12	12
	4					29	29	13	13	14	14	15	15	16	16	17	17
	5						29	13	13	14	14	15	15	16	16	17	17
	6							29	29	18	18	19	19	20	20	21	21
	7								29	18	18	19	19	20	20	21	21
	8									30	30	22	22	23	23	24	24
	9										30	22	22	23	23	24	24
	10											30	30	25	25	26	26
	11												30	25	25	26	26
	12													31	31	27	27
	13														31	27	27
	14															31	31
	15																31

Table 5: Correlator Mode A32 Correlator-Chip Assignments

Chip configurations 0-27: Mode B7
28-31: Mode B13

Mode B32

Mode B32 supports 11 stations of 16 channels each, with full auto-correlation. 55 cross-correlation baselines plus 11 auto-correlations are processed for each of two channels on a each correlator board, . Table 6 suggests a distribution of processing of the first channel over correlator chips 0-14; the second channel would be allocated correlator chips 16-30.

		Remote										
	Stn	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**
Ref	**0**	10	10	10	0	0	1	1	2	2	3	3
	1		10	10	0	0	1	1	2	2	3	3
	2			11	11	11	4	4	5	5	6	6
	3				11	11	4	4	5	5	6	6
	4					12	12	12	7	7	8	8
	5						12	12	7	7	8	8
	6							13	13	13	9	9
	7								13	13	9	9
	8									14	14	14
	9										14	14
	10											15

Table 6: Correlator Mode B32 Correlator-Chip Assignments

Chip configurations 0-9: Mode B7
10-15: Mode H1

Mode C32

Mode C32 supports 8 stations of 16 channels each, with full auto-correlation. Table 7 suggests a distribution of processing of the first channel over correlator chips 0-7; the second, third and fourth channels will be allocated to correlator chips 8-15; 16-23 and 24-31, respectively.

		Remote							
	Stn	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**
Ref	**0**	6	6	0	0	1	1	2	2
	1		6	0	0	1	1	2	2
	2			6	6	3	3	4	4
	3				6	3	3	4	4
	4					7	7	5	5
	5						7	5	5
	6							7	7
	7								7

Table 7: Correlator Mode C32 Correlator-Chip Assignments

Chip configurations 0-5: Mode B7
6-7: Mode B13

64 Complex-Lag Processing Modes

Four basic operating modes, designated A64, B64 and C64, are available for 64 complex-lag processing. For each of these modes, it is assumed that all 16 channels available from each Station Unit are to be cross-correlated with all 16 channels from all other Station Units. These modes are summarized in Table 8 below:

	Scan Parameters			Correlator Configuration		
Mode	#stns	#base-lines	#chns/ station	#slices	hardware utilization	Comments
A64	11	55	16	4	98%	Complete 11-stn processing
B64	8	28	16	2	100%	Complete 8-stn processing
C64	5	10	16	1	94%	Complete 5-stn processing

Table 8: Mark IV correlator 64-complex-lag processing modes

64 Complex-Lag Chip Configurations

In 64 complex-lag mode, each correlator chip will be configured to one of the two following modes:

1. Mode B9: '2(1x1) XX Complex Cross-correlation' mode (Appendix B9 of Mark4 memo 237), which has the correlation matrix shown in Table 9:

		Remote	
		X2	X3
Ref	X0		64C
	X1	64C	

Table 9: Chip mode B9 (with validity/sample enabled)

2. Mode B15: '2(1x1) XX Complex Auto-correlation' mode (Appendix B15 of Mark4 memo 237), which has the correlation matrix shown in Table 10:

		Remote			
		X0	X1	X2	X3
Ref	X0				64C
	X1		64R		
	X2			64R	
	X3				

Table 10: Chip mode B15 (with validity/sample enabled)

Mode A64

Mode A64 supports all cross-correlations and auto-correlations for 11 stations of 16 channels each. A single correlator board processes all 55 cross-correlation baselines plus 11 auto-correlations for a single channel. Table 11 suggests a possible assignment of correlator chips on a single correlator board. Each entry indicates the particular correlator-chip number to which the corresponding correlation should be assigned.

		Remote										
	Stn	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**
Ref	**0**	25	0	1	2	3	4	5	6	7	8	25
	1		25	0	1	2	3	4	5	6	7	8
	2			26	9	10	11	12	13	14	15	26
	3				26	9	10	11	12	13	14	15
	4					27	16	17	18	19	20	27
	5						27	16	17	18	19	20
	6							28	21	22	23	28
	7								28	21	22	23
	8									29	24	29
	9										29	24
	10											30

Table 11: Correlator Mode A64 Correlator-Chip Assignments

Chip configurations 0-24: Mode B9
25-30: Mode B15; chip 30 used only for single auto-corr
31: Not used

Mode B64

Mode B64 supports 8 stations of 16 channels with full auto-correlation. Each correlator board processes 28 cross correlation baselines, plus 8 station auto-correlations, for each of two channels. Table 12 suggests a distribution of processing of the first channel over correlator chips 0-15; the second channel would be allocated correlator chips 16-31.

		Remote							
	Stn	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**
Ref	**0**	12	0	1	2	3	4	5	12
	1		12	0	1	2	3	4	5
	2			13	6	7	8	9	13
	3				13	6	7	8	9
	4					14	10	11	14
	5						14	10	11
	6							15	15
	7								15

Table 12: Correlator Mode B64 Correlator-Chip Assignments

Chip configurations 0-11: Mode B9
12-15: Mode B15

Mode C64

Mode C64 supports 5 stations of 16 channels each, with full auto-correlation. Each correlator board processes 10 cross-correlation baselines, plus 5 station auto-correlations, for each of four channels. Table 13 suggests a distribution of processing of the first channel over correlator chips 0-6; the second, third and fourth channels will be allocated to correlator chips 8-14; 16-22 and 24-30, respectively.

		Remote				
	Stn	**0**	**1**	**2**	**3**	**4**
Ref	**0**	4	0	1	2	4
	1		4	0	1	2
	2			5	3	5
	3				5	3
	4					6

Table 13: Correlator Mode C64 Correlator-Chip Assignments

Chip configurations 0-3: Mode B9
4-6: Mode B15
7: Not used

128 Complex-Lag Processing Modes

Four basic operating modes, designated A128, B128 and C128, are available for 128 complex-lag processing. For each of these modes, it is assumed that all 16 channels available from each Station Unit are to be cross-correlated with all 16 channels from all other Station Units. These modes are summarized in Table 14 below:

	Scan Parameters			Correlator Configuration		
Mode	#stns	#base-lines	#chns/ station	#slices	hardware utilization	Comments
A128	8	28	16	4	100%	Complete 8-stn processing
B128	5	10	16	2	85%	Complete 5-stn processing
C128	4	6	16	1	100%	Complete 4-stn processing

Table 14: Mark IV correlator 128-complex-lag processing modes

128 Complex-Lag Chip Configurations

In 128 complex-lag mode, each correlator chip will be configured to one of the two following modes:

1. Mode B17: '1x1 XX Complex Cross-correlation' mode (Appendix B17 of Mark4 memo 237), which has the correlation matrix shown in Table 15:

		Remote
		X3
Ref	X0	128C

Table 15: Chip mode B17 (with validity/sample enabled)

2. Mode B19: 'Two-input XX Auto-correlation' mode (Appendix B19 of Mark4 memo 237), which has the correlation matrix shown in Table 16:

		Remote X0	Remote X3
Ref	X0	128R	
	X3		128R

Table 16: Chip mode B19 (with validity/sample enabled)

Mode A128

Mode A128 supports all cross-correlations and auto-correlations for 8 stations of 16 channels each. A single correlator board processes all 28 cross-correlation baselines plus 8 auto-correlations for a single channel. Table 17 suggests a possible assignment of correlator chips on a single correlator board. Each entry indicates the particular correlator-chip number to which the corresponding correlation should be assigned.

		Remote							
	Stn	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**
Ref	**0**	28	0	1	2	3	4	5	6
	1		28	7	8	9	10	11	12
	2			29	13	14	15	16	17
	3				29	18	19	20	21
	4					30	22	23	24
	5						30	25	26
	6							31	27
	7								31

Table 17: Correlator Mode A128 Correlator-Chip Assignments

Chip configurations 0-27: Mode B17
28-31: Mode B19

Mode B128

Mode B128 supports 5 stations of 16 channels with full auto-correlation. Each correlator board process 10 cross correlation baselines, plus 5 station auto-correlations, for each of two channels. Table 18 suggests a distribution of processing of the first channel over correlator chips 0-12; the second channel would be allocated correlator chips 16-28.

		Remote				
	Stn	**0**	**1**	**2**	**3**	**4**
Ref	**0**	10	0	1	2	3
	1		10	4	5	6
	2			11	7	8
	3				11	9
	4					12

Table 18: Correlator Mode B128 Correlator-Chip Assignments

Chip configurations 0-9: Mode B17
10-12: Mode B19; only half of chip 12 used
13-15: Not used

Mode C128

Mode C64 supports 4 stations of 16 channels each, with full auto-correlation. Each correlator board processes 6 cross-correlation baselines, plus 4 station auto-correlations, for each of four channels. Table 19 suggests a distribution of processing of the first channel over correlator chips 0-7; the second, third and fourth channels will be allocated to correlator chips 8-15; 16-23 and 24-31, respectively.

		Remote			
	Stn	**0**	**1**	**2**	**3**
Ref	**0**	6	0	1	2
	1		6	3	4
	2			7	5
	3				7

Table 19: Correlator Mode C128 Correlator-Chip Assignments

Chip configurations 0-5: Mode B17
6-7: Mode B19

Information to be Passed to Correlator Resource Manager

For a given scan, the following information must be passed to the correlator resource manager (CRM):

1. Correlator mode (A32, B64, etc).
2. Station Unit list, ordered as desired for reference/remote stations. [Normally, the correlator resources will be allocated before the explicit SU list is available.]
3. For each Station Unit, list of valid output channels.
4. Some housekeeping information that will allow the CUCC to properly tag and dispatch the correlator data to the proper NFS destination.

Based upon this information, the CRM will assign and configure the necessary correlator boards to receive and process the expected data. The CRM does not need any detailed channel information since the SU embeds detailed processing parameters in the data stream.

The function of the CRM may reside entirely in the CCC or may be split between the CCC and CUCC's.

In the absence of an explicit request for a particular slice, the CRM should assign slices in cyclical order so as exercise as much correlator hardware as possible over a period of time.

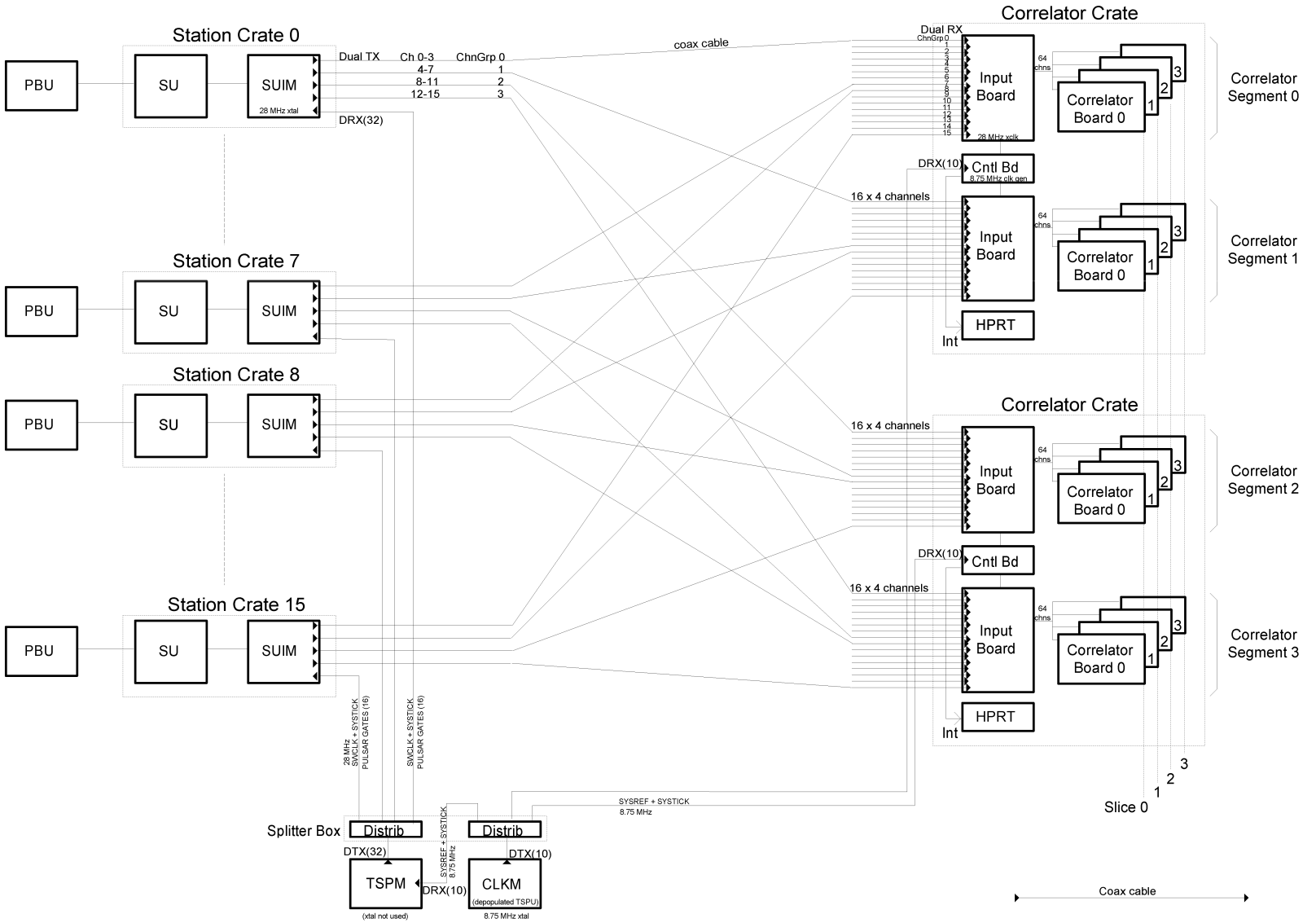
Correlator Resource Allocation Guidelines

The following guidelines are suggested for allocation of correlator resources:

1. Allocation will be strictly made in physical 'slices'. This restricts the maximum number of simultaneous scans to four.
2. For cases where the number of stations is less than the maximum for a given mode, the extra resources available on any given correlator board will be dedicated as much as possible to 'mirroring'.

Other Modes

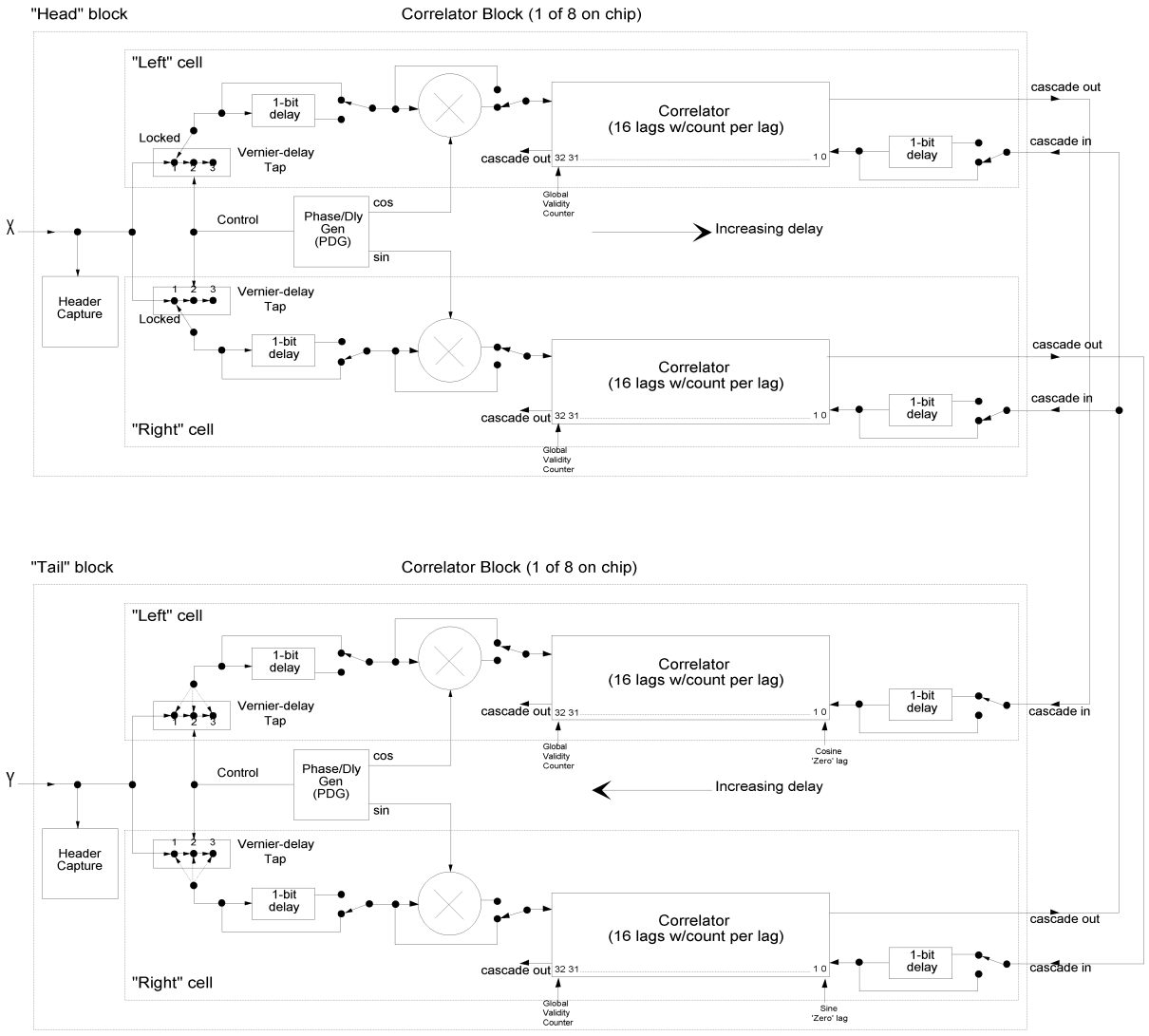
This note deals only with modes which do not use chip-to-chip cascading, which limits the number of complex lags to 128. 'Cascade' modes will be dealt with in future discussions.



Correlator Signal Interconnection Diagram w/o Data Distributor
(16 stations, 16 channels/station, 32 Msamples/sec/channel)

SYSTEM2.DRW

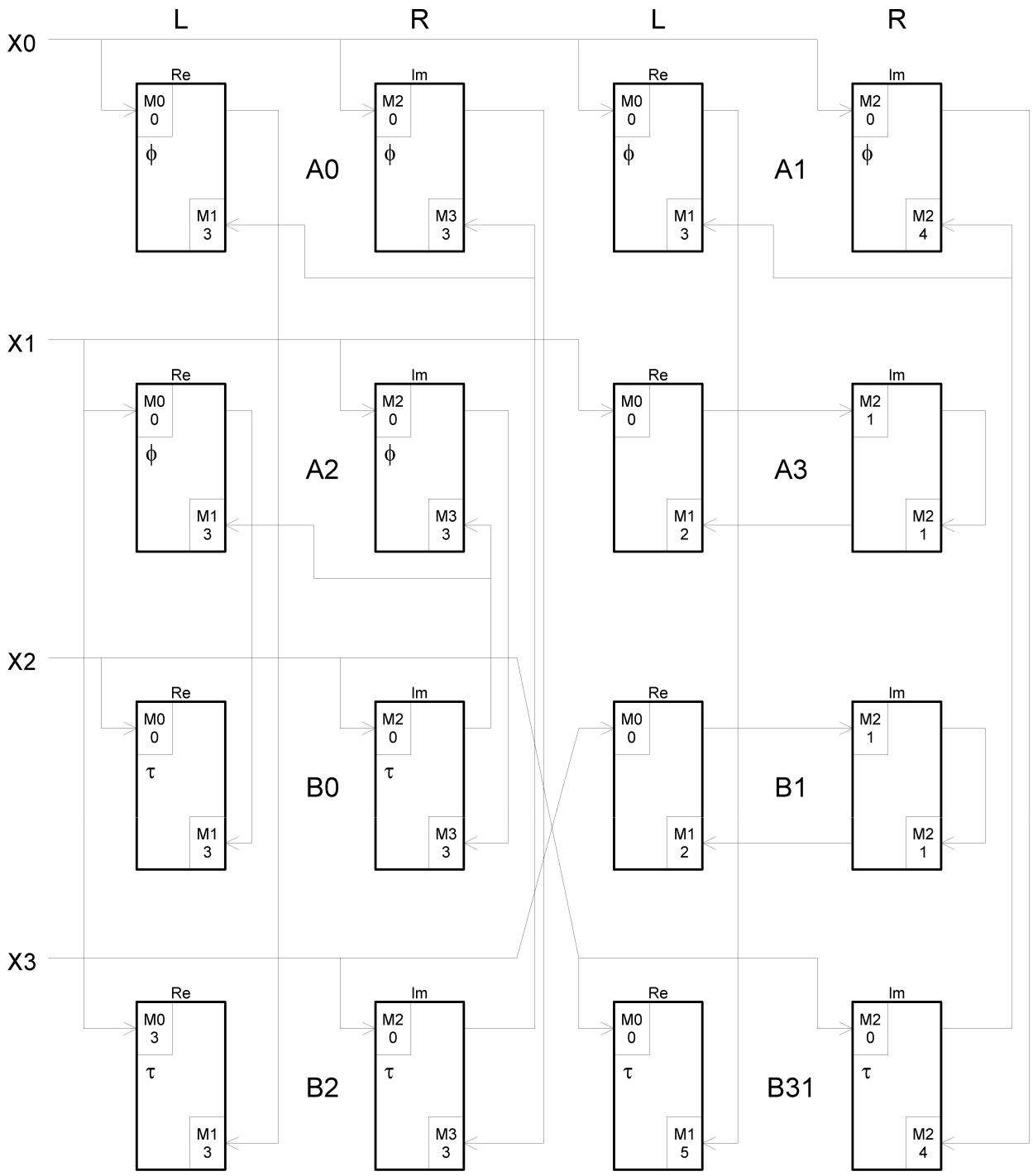
ARW
23 Nov 99



Note 1: Direction of 'increasing delay' defined as correlation with relatively later-recorded Y with respect to X.
Note 2: Data readout order within block -
Right cell 0-32 (33 24-bit words)
Left cell 0-32 (33 24-bit words)
Header capture 0-9 (10 24-bit words)
Note 3: Block readout order within chip - B2,B3,A0,A1,A2,B1,B0,A3
Note 4: Static-parameter write order - B2,B3,A0,A1,A2,B1,B0,A3 (1 24-bit word/block)
Note 5: Dynamic-parameter write order - A1,B2,A0,B3,B1,B0,A2,A3 (22 16-bit words/block)
Note 6: PDG Residue read order - A1,B2,A0,B3,B1,B0,A2,A3 (22 16-bit words/block)

Figure 2: A Correlator 'Double-Block'
(Typical Complex Cross-Correlation Configuration with 32 complex lags)

CORRBLK.DS4
ARW
18 OCT 99




```
snake = complex : X0 : X1 : A0I- : B2I ;
snake = complex : X0 : X2 : A1I- : B3I ;
snake = complex : X1 : X2 : A2I- : B0I ;
auto = X1 : : A3I : A3r ;
auto = X3 : : B1I : B1r ;
```

Ref \ Remote	X0	X1	X2	X3
X0		32C	32C	
X1		32A	32C	
X2				
X3				32A

Figure 3: Correlator Chip Mode H1

MODEH1.DRW
ARW 23 Nov 99