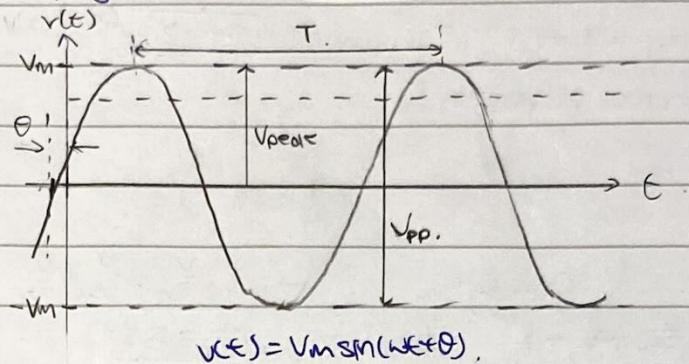


## AC circuit theory

Terms and definitions.

- By convention, we represent the DC parameters such as voltage  $V$  and current  $I$  in uppercase; the AC time varying voltage  $v$  and current  $i$  is lower case.
- For a sinusoidally varying voltage  $v(t)$ : [same as current  $i(t)$ ].



$T$ : Period

$\omega$ : Angular frequency  $[\omega = \frac{2\pi}{T}]$

$\theta$ : Phase (w.r.t.  $\sin(\omega t)$  in this case)

$V_{peak}$ : Peak voltage (Amplitude),

$V_{pp}$ : Peak-to-peak voltage [ $V_{pp} = 2V_{peak}$ ]

$V_{rms}$ : Root mean squared voltage [ $V_{rms} = \sqrt{\frac{V}{T}}$ ]

\* The voltage can have a DC offset  $V_0$   $\rightarrow$  voltage need not vary about 0.

$$\text{i.e. } v(t) = V_0 + V_m \sin(\omega t + \theta).$$

- It is often useful to mathematically represent the sinusoids in their complex form.

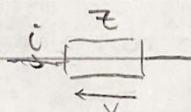
$$v(t) = V_m e^{j\omega t} = V_m (\cos \omega t + j \sin \omega t), \quad \text{where } j = \sqrt{-1}.$$

- For an AC current, the RMS value is equal to the value of the DC value that would produce the same average power dissipation in a resistive load.

- For sinusoidal voltages and currents, we can convert to RMS by dividing the peak value by  $\sqrt{2}$ .  $A_{rms} = \sqrt{\frac{1}{T} \int_0^T [A \sin(\omega t)]^2 dt} = \frac{A_p}{\sqrt{2}}$ .

## Ohm's law

- Ohm's law states that at a constant temp, the current flowing through an ohmic device is prop. to the pd. applied across it.



$$V = iZ$$

units of  $Z$  is  $\Omega$ .

- Impedance  $Z$  is the ratio of pd. applied to the current.

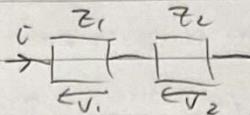
- The voltage either side of an ohmic device may not have the same phase  
 $\rightarrow Z$  is represented by a complex no.

- Impedance at DC ( $f=\omega=0$ ) is represented by resistance  $R$ .

# For Personal Use Only -bkwk2

Impedances in series and in parallel.

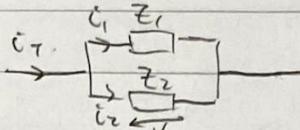
## ① Impedance in series



$$KVL: V_T = V_1 + V_2 \rightarrow i_T Z_T = i_T Z_1 + i_T Z_2.$$

$$\therefore Z_T = Z_1 + Z_2 \quad [\text{In general, } Z_T = \sum Z_i].$$

## ② Impedance in parallel



$$KCL: i_T = i_1 + i_2 \rightarrow \frac{V}{Z_T} = \frac{V}{Z_1} + \frac{V}{Z_2}.$$

$$\therefore \frac{1}{Z_T} = \frac{1}{Z_1} + \frac{1}{Z_2} \quad [\text{In general, } \frac{1}{Z_T} = \sum \frac{1}{Z_i}].$$

\* We can define admittance  $Y$  ( $Y = \frac{1}{Z}$ ) s.t.  $Y_T = \sum Y_i$ .

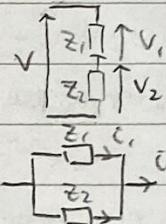
(DC equivalent is conductance  $G$  ( $G = \frac{1}{R}$ ) so  $G_T = \sum G_i$ ).

$$\begin{aligned} \text{In general, } Z &= R+jX \\ \text{so } Y &= \frac{1}{Z} = \frac{1}{R+jX} = \frac{R-jX}{R^2+X^2} \\ &= \frac{R}{R^2+X^2} - j\frac{X}{R^2+X^2} \quad [Y = G + jB] \\ &\quad \downarrow \quad \downarrow \\ &\text{conductance or susceptibility } G. \\ &\rightarrow G = \frac{1}{R} \text{ only in DC where } X = 0. \end{aligned}$$

Potential divider and current divider.

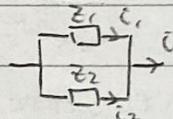
- For components in series  $\rightarrow$  potential divider.

$$\hookrightarrow V_2 = V \frac{Z_2}{Z_1 + Z_2}$$



- For components in parallel  $\rightarrow$  current divider

$$\hookrightarrow I_2 = I \frac{Z_1}{Z_1 + Z_2}$$



## Passive components.

Passive components.

Component	Symbol	Unit	Variable	Material	Equation
Resistor	$\square$	ohm ( $\Omega$ )	R	$\rho / \sigma$	$R = \rho \frac{l}{A}$
Capacitor	$\text{---}$	Farad (F)	C	$\epsilon_r$	$C = \frac{\epsilon_r \epsilon_0 A}{d}$
Inductor	$\text{---}$	Henry (H)	L	$M_r$	$L = M_r \mu_0 N^2 A / l$

- Certain types of capacitors and inductors have a polarity  $+\text{---} -$

- Under DC conditions:

$\hookrightarrow$  Capacitors act like infinite resistance (open circuit)

$\hookrightarrow$  Inductors act like zero resistance. (short circuit)

- Under high frequency AC conditions:

$\hookrightarrow$  Capacitors act like zero resistance (short circuit)

$\hookrightarrow$  Inductors act like infinite resistance. (open circuit).

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## Capacitors.

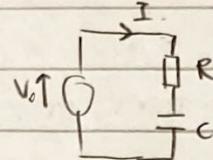
- From the geometry of a // plate capacitor,  $C = \frac{\epsilon_0 \epsilon_r A}{d}$
- Using the defn of  $C$  ( $C = \frac{Q}{V}$ ) we find that  $I_C = C \frac{dV}{dt}$ .
- Transient response of a capacitor:

### ① Charging

$$V_o = V_C + IR$$

$$V_o = V_C + RC \frac{dV_C}{dt}$$

$$\rightarrow V_C = V_o (1 - e^{-\frac{t}{RC}})$$

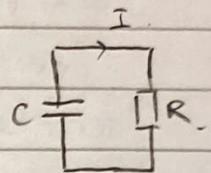


### ② Discharging

$$V_C = -IR$$

$$V_C = -RC \frac{dV_C}{dt}$$

$$\rightarrow V_C = V_o e^{-\frac{t}{RC}}$$



↳ The time constant  $\tau$  for a capacitor is  $\tau = RC$ .

- The impedance of a capacitor  $Z_C$  is given by  $Z_C = \frac{1}{j\omega C}$ .

↳ Consider  $V(t) = V_m e^{j\omega t}$ .

For a capacitor,  $i(t) = C \frac{d}{dt} V(t)$  so  $i(t) = j\omega C V_m e^{j\omega t}$

$$\rightarrow Z_C = \frac{V(t)}{i(t)} = \frac{1}{j\omega C}$$

↳ The current  $i(t)$  leads the voltage  $v(t)$  by  $\frac{\pi}{2}$  [CIVIL]

- The reactance of a capacitor  $X_C$  is given by  $X_C = \frac{1}{\omega C}$ . [ $Z_C = -jX_C$ ].

## Inductors.

- From the geometry of an inductor,  $L = \frac{M_0 M_r N^2 A}{l}$ .

- Using the defn of  $L$  ( $L = \frac{d\Phi}{I}$ ), we find that  $V_L = L \frac{dI}{dt}$ .

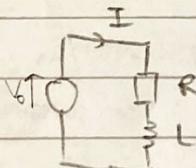
- Transient response of an inductor:

### ① Charging

$$V_o = V_L + IR$$

$$V_o = L \frac{dI}{dt} + IR$$

$$\rightarrow I_C = \frac{V_o}{R} (1 - e^{-\frac{Rt}{L}})$$

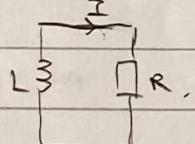


### ② Discharging

$$V_L = -IR$$

$$L \frac{dI}{dt} = -I_L R$$

$$\rightarrow I_L = \frac{V_o}{R} e^{-\frac{Rt}{L}}$$



↳ The time constant  $\tau$  for an inductor is  $\tau = \frac{L}{R}$ .

- The impedance of an inductor  $Z_L$  is given by  $Z_L = j\omega L$ .

↳ Consider  $i(t) = I_m e^{j\omega t}$

For an inductor,  $v(t) = L \frac{d}{dt} i(t)$  so  $v(t) = j\omega L I_m e^{j\omega t}$

$$\rightarrow Z_L = \frac{V(t)}{i(t)} = j\omega L$$

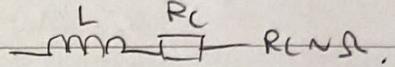
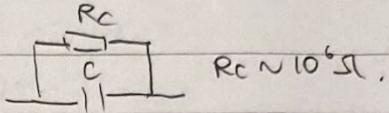
↳ The current  $i(t)$  lags the voltage  $v(t)$  by  $\frac{\pi}{2}$  [CIVIL]

- The reactance of an inductor  $X_L$  is given by  $X_L = \omega L$  [ $Z_L = jX_L$ ].

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## Real capacitors and inductors.

- In reality, no capacitor/inductor is perfect so we can represent that imperfection theoretically by adding a resistor in parallel/series.
- For capacitors, a parallel resistance represents the leakage current through the dielectric.
  - ↳ An ideal capacitor has 0 resistance for DC but in reality there is a leakage current  $\rightarrow R_c$  in //.
- For inductors, a series resistance represents the resistance of the wire
  - ↳ An ideal inductor has 0 resistance for DC but in reality there is finite resistance  $\rightarrow R_L$  in series



## Polar diagrams.

- We can analyse both capacitance and inductance in terms of the magnitude & phase of the voltage, current and impedance.
- ↳ We usually use the RMS voltage and current to consider time varying functions.

- Consider a series RLC circuit.

$$Z_T = Z_R + Z_L + Z_C$$

$$= R + (X_L - X_C)j. \quad [z = R + Xj].$$

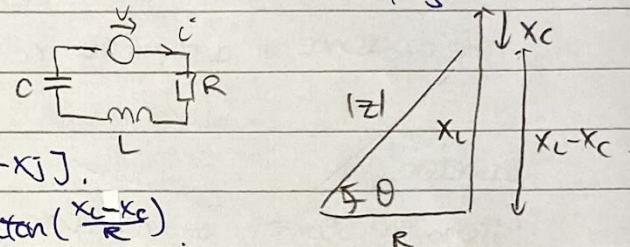
$$\rightarrow |z| = \sqrt{R^2 + (X_L - X_C)^2}, \quad \theta = \arctan\left(\frac{X_L - X_C}{R}\right).$$

From this,  $|V| = I|z|$  and  $V$  leads  $I$  by  $\theta$  rad.

(note the current  $I$  is the same (magnitude + phase) in the same across each component since they are connected in series).

↳  $|V|/|I|$  gives the amplitude of voltage/current;

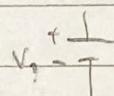
$\text{Re}(V)/\text{Re}(I)$  gives the (measurable) voltage/current at a particular instant.



## Sources.

### Voltage sources.

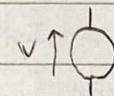
- Symbols



battery



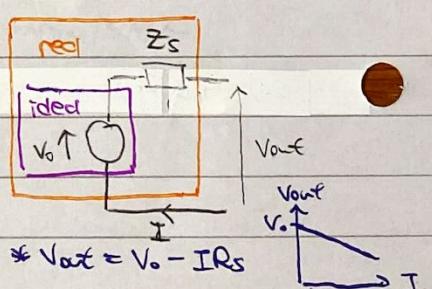
DC voltage source



AC voltage source

- An ideal voltage source will have a constant voltage  $V_0$  (or amplitude  $V$ ) across its terminals and no resistance.

- We can make the voltage source real by adding an impedance  $Z_S$  in series, where  $Z_S$  is the internal impedance of the source.



$$* V_{out} = V_0 - I R_S$$

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## Current sources

- Symbols



DC current source



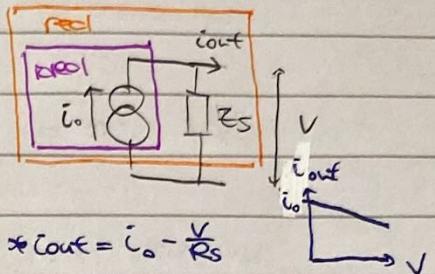
AC current source

- An ideal current source will always provide a constant current  $I_0$  (or amplitude  $i$ ) across its terminals and has no resistance.

- We can make the current source real by adding an impedance  $Z_S$  in parallel, where  $Z_S$  is the internal resistance of the source.

\* The p.d. across a current source is given by  $iZ_S$ .  $\Rightarrow i_{out} = i_0 - \frac{V}{R_S}$

(As an ideal source has no resistance, effectively  $Z_S \rightarrow \infty$  so p.d. across source is  $\infty$ ).

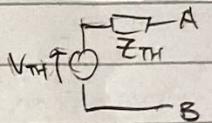


## Thevenin and Norton equivalents

obeys Ohm's law  $V = iZ$ .

- Thévenin's thm states that any 2-terminal, linear network of sources and impedances may be replaced by a single voltage source  $V_{TH}$  in series w/ an impedance  $Z_{TH}$

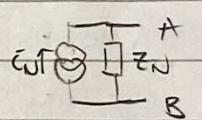
$\hookrightarrow V_{TH}$ : open circuit voltage at terminals A and B.



$\hookrightarrow Z_{TH}$ : The impedance seen at AB after "killing" all sources.

- Norton's thm states that any 2-terminal, linear network of sources and impedances may be replaced by a single current source  $I_N$  in parallel w/ an impedance  $Z_N$ .

$\hookrightarrow I_N$ : short circuit current at terminals A and B.



\* To "kill" a voltage source  $\rightarrow$  provide no pd.  $\rightarrow$  short circuit.

To "kill" a current source  $\rightarrow$  provide no current  $\rightarrow$  open circuit.

- If we treat the network as a black box and measure the open circuit voltage and short circuit current, we can replace it w/ a Thévenin/Norton equivalent w/ the same properties.

- Converting between Thévenin and Norton equivalents,

Some way for getting  $Z_{TH}$  and  $Z_N$   $\rightarrow Z_{TH} = Z_N$ .

For Thévenin,

$$V_{TH} = I_N Z_N$$

; For Norton,

$$I_N = \frac{V_{TH}}{Z_{TH}}$$

\*  $V_{TH} = V_{out}$  given  $i=0$  (i.e. no load attached / open circuit).

$\rightarrow$  useful for finding the individual voltage source from the original network.

\* The power dissipations of the Thévenin and Norton equivalent circuits are not necessarily conservative, even though the power dissipated by the output terminals (loading impedance) is the same.

\* To combine voltage sources  $\rightarrow$  make them in series  $\rightarrow V_T = \sum V_i$

To combine current sources  $\rightarrow$  make them in parallel  $\rightarrow I_T = \sum I_i$

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**Kirchhoff's laws for voltages and currents**

**Kirchhoff's voltage law (KVL)**

- By consv. of energy, the work done by a battery / power source in driving a current is equal to the energy dissipated within the circuit.
- KVL states that the sum of voltages around a closed loop must be 0, i.e.

$$\sum_{\text{loop}} V_i = 0$$

- KVL is the basis for mesh analysis.

**Kirchhoff's current law (KCL)**

- By consv. of charge, the current flowing into any pt. of a circuit must equal the current which flows out of that pt. (else we would accumulate/dissipate charge).
- KCL states that the sum of currents at every junction must be 0, i.e.

$$\sum_{\text{node}} I_i = 0$$

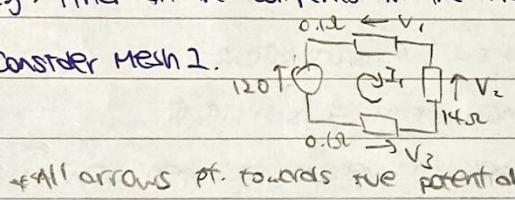
- KCL is the basis for nodal analysis.

**Mesh analysis**

- Mesh analysis applies KVL systematically to a circuit and produces simultaneous eqns which may be solved to give the mesh currents.
- A mesh is a loop in a circuit with no loops inside it.

- e.g.: Find all the currents in the network below.

Consider Mesh 1.



KVL.

$$120 - V_1 - V_2 - V_3 = 0.$$

$$(120 - 0.1I_1 - 14(I_1 - I_3) - 0.1(I_1 - I_2)) = 0.$$

$$14.2I_1 - 0.1I_2 - 14I_3 = 120.$$

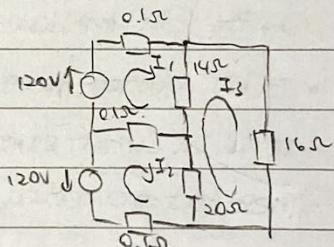
$$\text{Similarly, Mesh 2 : } -0.1I_1 + 20.2I_2 - 20I_3 = 120$$

$$\text{Mesh 3 : } -14I_1 - 20I_2 + 50I_3 = 0.$$

→ solving gives  $I_1 = 23.1\text{A}$ ,  $I_2 = 20.6\text{A}$ ,  $I_3 = 14.7\text{A}$ .

\* For qn. involving a current source, assign a voltage  $V$  across the source and apply KVL as usual. After "losing" an eqn. from eliminating  $V$ , use KCL to "regain" an additional eqn.

\* Mesh analysis can be applied in the same way for AC circuits



\* AS WE GO along a mesh,  
think whether  $V$  increases/decreases.

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Nodal analysis.

- Nodal analysis applies KCL systematically to a circuit and produces simultaneous eqns. which may be solved to give the nodal voltages.
- Voltages are assigned to each principal node of a network - nodes where 3 or more branches of a circuit join.

- e.g. Find the voltages of each principal node in the network below.

consider Node 1.

The circuit diagram shows three nodes labeled  $V_1$ ,  $V_2$ , and  $V_3$ . Node  $V_1$  is at the top,  $V_2$  is at the bottom left, and  $V_3$  is at the bottom right. There are resistors of  $0.1\Omega$ ,  $16\Omega$ ,  $14\Omega$ ,  $14\Omega$ ,  $0.6\Omega$ , and  $20\Omega$ . Voltage sources of  $+120V$ ,  $-120V$ , and  $120V$  are also present. Currents  $I_1$  through  $I_6$  are indicated flowing through the resistors.

KCL

$$I_1 + I_2 + I_3 = 0.$$

$$\frac{V_1 - 120}{0.1} + \frac{V_1 - V_3}{16} + \frac{V_1 - V_2}{14} = 0.$$

$$10 \cdot 13V_1 - 0.07V_2 - 0.0675V_3 = 1200,$$

Similarly, Node 2 :  $-0.07(V_1 + 0.12V_2 - 0.05V_3) = 0$

Node 3 :  $-0.0675V_1 - 0.05V_2 + 10.11V_3 = -1200$ .

→ solving gives  $V_1 = 117.7V$ ,  $V_2 = 0.24V$ ,  $V_3 = -118V$ .

\* Nodal analysis can be applied in the same way for AC circuits.

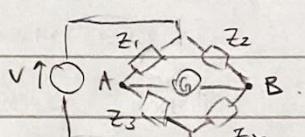
Bridge circuits.

- Bridge circuits are used in instrumentation applications when resistance / impedance is to be measured.
- They all have the same basic symmetry, → the Wheatstone bridge used for resistance and the Wien and Maxwell bridges used for impedances (Capacitance and inductance resp.).
- At the balance pt, there will be no current through an ammeter/voltmeter  $G$  and the two sides are at the same voltage.

$$V_A = V \cdot \frac{Z_x}{Z_1 + Z_3} = V_B = V \cdot \frac{Z_x}{Z_1 + Z_2} \rightarrow \frac{Z_x + Z_2}{Z_1 + Z_3} = \frac{Z_x}{Z_2}.$$

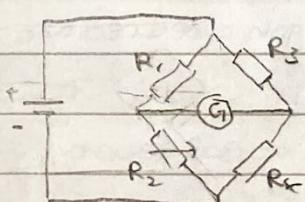
$$1 - V_A = V \cdot \frac{Z_1}{Z_1 + Z_3} = 1 - V_B = V \cdot \frac{Z_2}{Z_1 + Z_2} \rightarrow \frac{Z_x + Z_2}{Z_1 + Z_3} = \frac{Z_2}{Z_1}$$

$$\therefore \frac{Z_x}{Z_3} = \frac{Z_2}{Z_1} \quad \text{or} \quad \frac{Z_x}{Z_2} = \frac{Z_3}{Z_1}$$

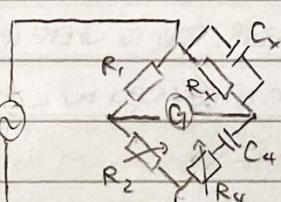


- circuit diagrams for common bridges.

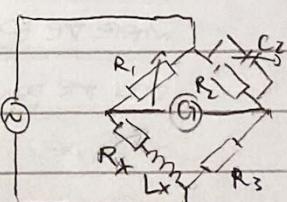
Wheatstone bridge



Wien bridge



Maxwell bridge

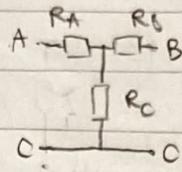
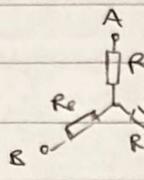


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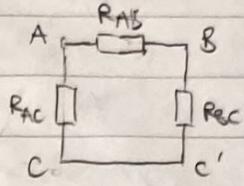
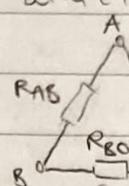
## The star-delta transformation.

- The transformation between star and delta networks make the overall network easier to analyse.

Star ( $\Delta$  or T)



Delta ( $\pi$ )



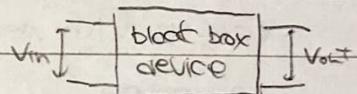
- Delta to star :  $R_A = \frac{R_{AB}R_{AC}}{\Sigma R}$ ;  $R_B = \frac{R_{AB}R_{BC}}{\Sigma R}$ ;  $R_C = \frac{R_{AC}R_{BC}}{\Sigma R}$ ,  $\Sigma R = R_{AB} + R_{BC} + R_{AC}$
- Star to delta :  $G_{AB} = \frac{G_A G_B}{\Sigma G}$ ;  $G_{BC} = \frac{G_B G_C}{\Sigma G}$ ;  $G_{AC} = \frac{G_A G_C}{\Sigma G}$ ,  $\Sigma G = G_A + G_B + G_C$ .
- \* For AC, replace  $R$  w/  $Z$ ,  $G$  w/  $Y$ .  $[G = \frac{1}{R}, Y = \frac{1}{Z}]$ .

## Principle of superposition

- The superposition theorem states that the current in any branch of a circuit, or the voltage at any node, may be found by the algebraic addition of the currents/voltages produced by each source separately.
- When the effect of 1 source is considered, the other sources are "killed" (for non-tied sources, they are replaced by their internal resistances).

## Filters

Voltage transfer function, gain and cut-off frequency



- Consider a circuit as a block box that takes in an input voltage  $V_{in}$  ( $V_1$ ) and returns an output voltage  $V_{out}$  ( $V_2$ ).
- The voltage transfer function of the circuit is defined as  $H(j\omega) = \frac{\text{output voltage}}{\text{input voltage}} = \frac{V_2}{V_1} = \frac{V_2}{V_{in}}$
- The magnitude of the voltage transfer function is the gain/attenuation of the circuit,  $|H(j\omega)| > 1 \rightarrow \text{gain}; |H(j\omega)| < 1 \rightarrow \text{attenuation}$ .
- The gain (or attenuation) in a logarithmic (decibels dB) scale is defined as :

↳ Power gain

$$G_p = 10 \log_{10} \left( \frac{P_{out}}{P_{in}} \right)$$

↳ Voltage gain

$$G_v = 20 \log_{10} \left( \frac{V_{out}}{V_{in}} \right)$$

[20 instead of 10 because  $P \propto V^2$ ]

- The cut-off frequency  $f_c$  ( $\omega_c$ ) is defined as  $|H(j\omega_c)| = \frac{1}{\sqrt{2}}|H_{max}|$ , where  $|H_{max}|$  is the max. magnitude of the voltage transfer function. (Half-power frequency / 3dB frequency).
- We can find cutoff frequency from the voltage transfer function, where we get a ratio of 2 complex nos.  $\frac{A+jB}{D+jE}$ . Simply set D=E to find the cutoff frequency  $\omega_c$ .

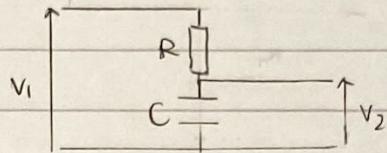
(since the denominator becomes  $D(j\omega)$ , and  $|1+j1| = \sqrt{2}$ )

\* Since  $\arg(j\omega) = 45^\circ$ , there is a phase diff. of  $45^\circ$  b/w  $V_{in}$  and  $V_{out}$ .

# For Personal Use Only -bkwk2

Low-pass filter — related to upper cut off frequency  $f_2, \omega_2$ .

- A low-pass filter (LPF) is used to pass low frequencies and block high frequencies.
- The circuit for a first order LPF is as follows:



$$\omega \rightarrow 0, H(j\omega) \rightarrow 1$$

$$\omega \rightarrow \infty, H(j\omega) \rightarrow 0.$$

The voltage transfer function  $H(j\omega)$  is given by

$$H(j\omega) = \frac{V_2}{V_1} = \frac{Z_C}{Z_C + Z_R} = \frac{\frac{1}{j\omega C}}{\frac{1}{j\omega C} + R} = \frac{1}{1 + j\omega CR} = \frac{1}{1 + (\omega RC)^2} = \frac{1}{\sqrt{1 + (\omega RC)^2}} \exp(-j\pi \operatorname{atan}(\omega RC))$$

From this, we can see that the gain in decibels is

$$G = 20 \log_{10} |H(j\omega)| = 20 \log_{10} \left( \frac{1}{\sqrt{1 + (\omega RC)^2}} \right) = -10 \log_{10} (1 + (\omega RC)^2)$$

and the phase is

$$\phi = \operatorname{arg}(H(j\omega)) = -\tan^{-1}(\omega RC)$$

Also, when expressing the voltage transfer function  $H(j\omega)$  in the form

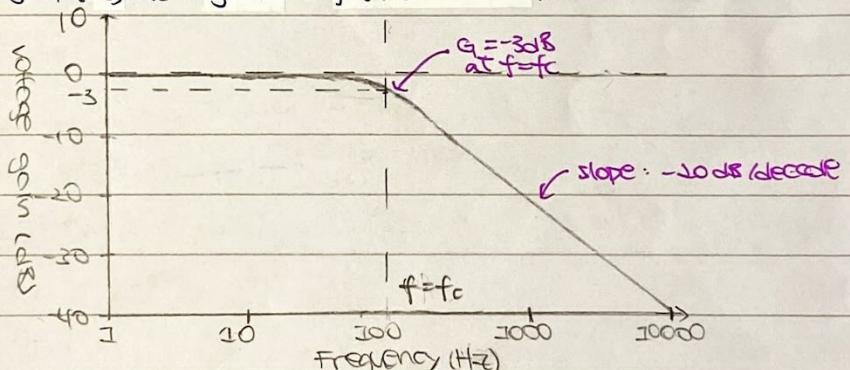
$$H(j\omega) = \frac{1}{1 + j\omega CR}$$

We can see the cut-off frequency is

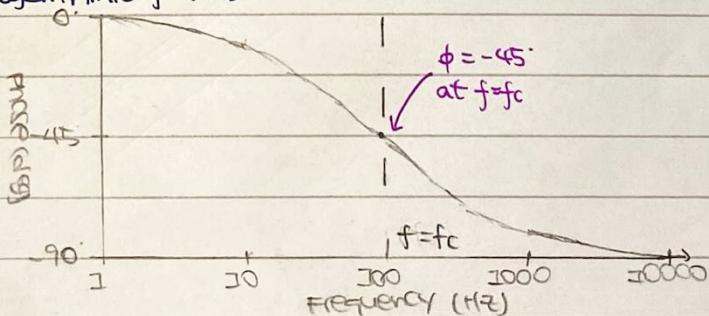
$$\omega_c = \frac{1}{CR} \quad \text{or} \quad f_c = \frac{\omega_c}{2\pi} = \frac{1}{2\pi CR}$$

- We can plot the Bode plot for the LPF.

①  $G = 20 \log_{10} |1 + j\omega CR|$  (dB) vs logarithmic  $f$  (Hz)



②  $\phi$  (deg) vs logarithmic  $f$  (Hz).



\* For high frequencies,  $1 + (\omega RC)^2 \approx (\omega RC)^2$

$$\text{so } G = -10 \log_{10} (1 + (\omega RC)^2) \approx -10 \log_{10} (\omega RC)^2 = -20 \log_{10} (\omega RC)$$

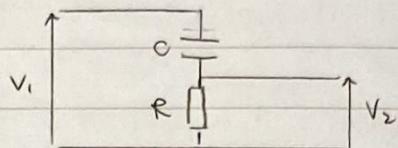
→ The slope is -20 dB/decade for high frequencies in plot ①.

# For Personal Use Only -bkwk2

High-pass filter / related to lower cut off frequency  $f_1/\omega_1$

- A high-pass filter (HPF) is used to pass high frequencies and block low frequencies

- The circuit for a first order HPF is as follows:



$$\omega \rightarrow 0, H(j\omega) \rightarrow 0$$

$$\omega \rightarrow \infty, H(j\omega) \rightarrow 1$$

The voltage transfer function  $H(j\omega)$  is given by

$$H(j\omega) = \frac{V_2}{V_1} = \frac{Z_C}{Z_C + Z_R} = \frac{R}{R + j/\omega C} = \frac{j\omega CR}{1 + j\omega CR} = \frac{\omega CR + j\omega CR}{1 + (\omega CR)^2} = \frac{\omega CR}{\sqrt{1 + (\omega CR)^2}} \exp(j\arg(\frac{1}{1 + (\omega CR)^2}))$$

From this, we can see that the gain in decibels is

$$G = 20 \log_{10}|H(j\omega)| = 20 \log_{10}\left(\frac{\omega CR}{\sqrt{1 + (\omega CR)^2}}\right)$$

and the phase is

$$\phi = \arg(H(j\omega)) = \tan^{-1}\left(\frac{1}{\omega CR}\right)$$

Also, when expressing the voltage transfer function  $H(j\omega)$  in the form,

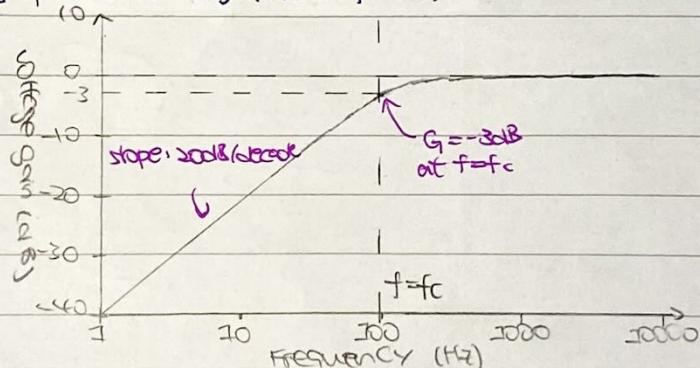
$$H(j\omega) = \frac{j\omega CR}{1 + j\omega CR}$$

We can see that the cut-off frequency is

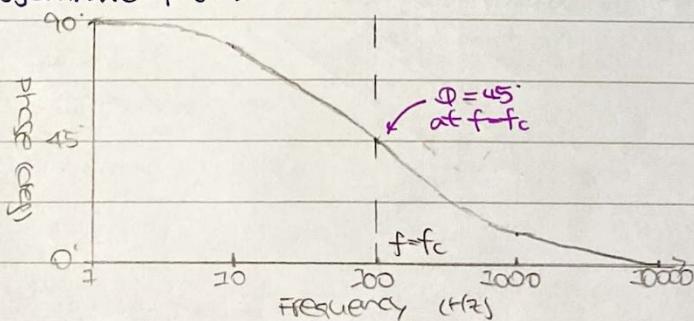
$$1 = \omega_1 CR \rightarrow \omega_1 = \frac{1}{CR}, \quad \text{or} \quad f_1 = \frac{\omega_1}{2\pi} = \frac{1}{2\pi CR}$$

- We can plot the Bode plot for the HPF.

①  $G = 20 \log_{10}|H(j\omega)|$  (dB) vs logarithmic  $f$  (Hz)



②  $\phi$  (deg) vs logarithmic  $f$  (Hz)



\* For low frequencies,  $1 + (\omega CR)^2 \approx 1$

$$\text{so } G = 20 \log_{10}\left(\frac{\omega CR}{\sqrt{1 + (\omega CR)^2}}\right) \approx 20 \log_{10}\left(\frac{\omega CR}{\sqrt{1}}\right) = 20 \log_{10}(\omega CR)$$

→ The slope is 20dB/decade for low frequencies in plot ①.

## Resonant circuits

### Electrical resonance

- Capacitors and inductors store and release energy at different times in the cycle. The amount of energy exchanged between the 2 elements is at a maximum at resonance.
- Adding a resistor (resistance) introduces damping to the system.
- For a LC circuit, (no R → undamped system), resonance occurs when the impedance of the capacitor and inductor are equal and opposite (i.e.  $Z_C = -Z_L$ ).
- The frequency at which resonance occurs in a LC circuit is the undamped natural frequency  $\omega_n$ .

$$Z_C = -Z_L$$

(same as undamped resonant frequency)

$$\frac{1}{j\omega C} = -j\omega L$$

$$\omega_n = \frac{1}{\sqrt{LC}} \quad \text{or} \quad f_n = \frac{1}{2\pi\sqrt{LC}}$$

- At the undamped natural frequency  $\omega_n$ , the impedances of

↳ Series LC circuit :  $Z_T = Z_C + Z_L = 0$

↳ Parallel LC circuit :  $Z_T = \frac{Z_C Z_L}{Z_C + Z_L} \rightarrow \infty$ .

\* In both cases, the impedances of the circuit only have a real part.

- For a RLC circuit, resonance occurs at the damped resonant frequency  $\omega$ , which is approximately equal to the undamped natural frequency  $\omega_n$  for light damping.

$$\omega = \omega_n \sqrt{1 - 2S^2}$$

where S is the damping ratio. ( $S=0$  when undamped).

- At the undamped natural frequency  $\omega_n$ , the impedances of

↳ Series RLC circuit :  $Z_T = Z_R + Z_C + Z_L = R$  (minimum)

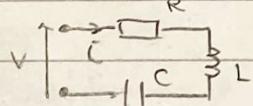
↳ Parallel RLC circuit :  $Z_T = \frac{Z_R Z_C Z_L}{Z_R Z_C + Z_R Z_L + Z_C Z_L} = R$ . (maximum)

\* In both cases, the impedances of the circuit only have a real part

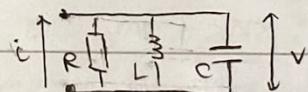
### Series and parallel RLC circuits.

- Series and parallel RLC circuits are as follows :

Series



Parallel



We can represent the circuits as 2nd order ODEs.

KVL:  $V = iR + L \frac{di}{dt} + \frac{q}{C}$

KCL:  $i = \frac{V}{R} + \frac{q}{C} + C \frac{dv}{dt}$

$$\frac{d^2q}{dt^2} = L \frac{d^2i}{dt^2} + R \frac{di}{dt} + \frac{1}{C} i$$

$$\frac{d^2i}{dt^2} = C \frac{d^2v}{dt^2} + \frac{1}{R} \frac{dv}{dt} + \frac{1}{L} v$$

\* R term is the 1st order term → damping of the system

- Series and parallel RLC circuits equivalents are only useful for finding the bandwidth as the Q factor for a series/parallel RLC circuit is easy to find.

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$Q$  factor.

- The  $Q$  factor (quality factor) is a measure of damping of a system/resonator.

↳  $Q < \frac{1}{2}$  → underdamped

↳  $Q > \frac{1}{2}$  → overdamped.

↳  $Q = \frac{1}{2}$  → critically damped

$$[Q = \frac{1}{2\zeta}]$$

-  $Q$  factor can be defined as:

↳ ratio of energy stored in resonant component to energy dissipated in resistor per cycle.

↳ ratio of the system's centre frequency to its bandwidth  $Q = \frac{\omega_0}{\Delta\omega} = \frac{f_0}{\Delta f}$ , (related to the sharpness of the peak at resonance).

$Q$  factor of individual resonant components.

- The  $Q$  factor of individual resonant components is a measure of the imperfections of the component. (Higher  $Q$  factor → closer to an ideal component).

- The  $Q$  factor of individual resonant components depends on the frequency, but we usually evaluate it at resonance.

- The imperfections of a real component can be modelled by adding a resistor in series or in parallel w/ an ideal component.

↳ Resistor in series:  $Q = \frac{I^2 X}{I^2 R_S} = \frac{X}{R_S}$

$$Q_L = \frac{\omega_n L}{R_{LS}} \quad Q_C = \frac{1}{\omega_n C R_{CS}}$$

↳ Resistor in parallel:  $Q = \frac{V^2 X}{V^2 R_P} = \frac{R_P}{X}$

$$Q_L = \frac{R_P}{\omega_n L} \quad Q_C = \omega_n C R_{CP}$$

- For any given frequency, the imperfections, and hence  $Q$  factor of a component is the same for both a resistor connected in series or in parallel.

↳ Inductor.

$$Q_L = \frac{\omega_n L}{R_{LS}} = \frac{R_P}{\omega_n L}$$

$$R_{LS} = \frac{(\omega_n L)^2}{R_{LP}} = \frac{1}{Q^2} R_{LP}$$

$$R_{LP} = \frac{(\omega_n L)^2}{R_{LS}} = Q^2 R_{LS}$$

↳ Conductor

$$Q_C = \frac{1}{\omega_n C R_{CS}} = \omega_n C R_{CP}$$

$$R_{CS} = \frac{1}{(\omega_n C)^2 R_{CP}} = \frac{1}{Q^2} R_{CP}$$

$$R_{CP} = \frac{1}{(\omega_n C)^2 R_{CS}} = Q^2 R_{CS}$$

\*This is only valid for a large enough  $Q$ :

↳ For the 2 configurations to be equivalent,  $Z_{\text{series}} = Z_{\text{parallel}}$ .

$$R_{LS} + j\omega L = \frac{j\omega L R_P}{R_P + j\omega L}$$

$$j\omega C R_{CS} + I = \frac{j\omega C R_{CP}}{1 + j\omega C R_{CP}}$$

Comparing real parts, we get the expressions above.

Comparing imaginary parts, we find that we req -

$$R_{LS} + R_{LP} = R_{LP}$$

$$R_{CS} + R_{CP} = R_{CP}$$

i.e.  $R_{CP} \gg R_{CS}$  (true for large  $Q$ )

i.e.  $R_{CP} \gg R_{CS}$  (true for large  $Q$ ).

# For Personal Use Only -bkwk2

Q factor for series and parallel RLC circuits.

- The Q factor of a circuit can be found by using the 1st definition of Q factor if the circuit is a (pure) series or parallel RLC circuit.

$$\hookrightarrow \text{series RLC circuit: } Q = \frac{I^2 X}{I^2 R} = \frac{X}{R}$$

$$Q = \frac{X_L}{R} = \frac{\omega L}{R}, \quad \rightarrow \quad Q = \frac{\omega L}{R}, \quad Q = \frac{1}{\omega CR}$$

$$Q^2 = \frac{L}{RC} \quad \rightarrow \quad Q = \frac{1}{R} \sqrt{\frac{L}{C}}$$

$$\hookrightarrow \text{parallel RLC circuit: } Q = \frac{V^2 X}{V^2 R} = \frac{X}{R}$$

$$Q = \frac{R}{X_C} = \frac{R}{\frac{1}{\omega C}} \quad \rightarrow \quad Q = \frac{R}{\omega L}, \quad Q = \omega CR$$

$$Q^2 = \frac{R^2 C}{L} \quad \rightarrow \quad Q = R \sqrt{\frac{C}{L}}$$

- The Q factor is also the ratio of output signal to input signal for a (pure) series or parallel RLC circuit at resonance.

$\hookrightarrow$  Series RLC circuit:

$$\text{At resonance, } Z_C = -Z_L \text{ so } Z_T = R.$$

$$V_x = V \frac{Z_x}{Z_T} = V \frac{Z_x}{R} \quad \rightarrow \quad |V_x| = V \frac{|Z_x|}{R} = V \frac{X}{R}.$$

$$\therefore |V_x| = Q |V|$$

$\hookrightarrow$  Parallel RLC circuit.

$$\text{At resonance, } Z_C = -Z_L \text{ so } Z_T = R.$$

$$i_x = i \frac{Z_T}{Z_x} = i \frac{R}{Z_x} \quad \rightarrow \quad |i_x| = i \frac{R}{|Z_x|} = i \frac{R}{X}$$

$$\therefore |i_x| = Q |i|$$

bandwidth.

- The bandwidth  $\Delta\omega$  is the difference between the lower and upper half-power frequencies  $\omega_{1/2}$ .

$$\Delta\omega = \omega_2 - \omega_1$$

- The half-power frequency is defined as the frequency of which the power consumption is half that of resonance (3dB frequency).

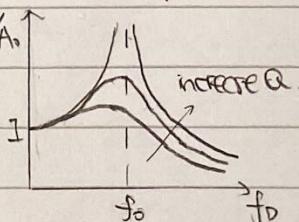
- The resonant frequency  $\omega_r$  is (approximately) the mean of the 2 half-power frequencies.

- The bandwidth of a circuit is related to the Q factor of the circuit.

$$Q = \frac{\omega_r}{\Delta\omega} = \frac{f_0}{\Delta f}$$

- A large Q represents a sharp peak at resonance, and thus a small bandwidth.

- To find the Q factor of a general RLC circuit, we must convert it into a (pure) series or parallel RLC circuit, where  $Q = \frac{1}{R} \sqrt{\frac{L}{C}}$  or  $Q = R \sqrt{\frac{C}{L}}$ .



Two port model : the amplifier model

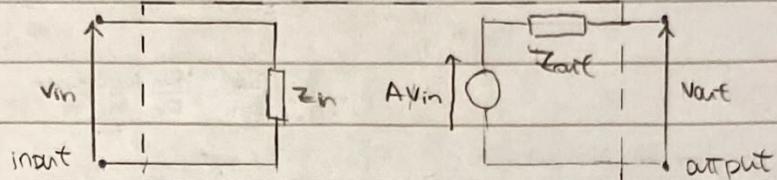
The voltage amplifier.

- A voltage amplifier takes in an input voltage  $V_{in}(t)$  and returns an output voltage  $V_{out}(t)$ ,

$$V_{in}(t) \rightarrow \text{amplifier} \rightarrow V_{out}(t) = A V_{in}(t)$$

where  $A$  is the voltage gain of the amplifier.

- The circuit for a general voltage amplifier is as follows.



We can represent any amplifier using 3 parameters:

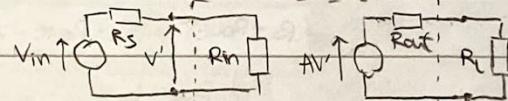
↳ Input impedance (usually resistance) :  $Z_{in}$

↳ Output impedance (usually resistance) :  $Z_{out}$

↳ Voltage gain :  $A = \frac{V_{out}}{V_{in}}$

\* This model assumes linear gain (i.e.  $A$  is a constant). However, it is possible to have an amplifier w/ a gain that is a function of frequency.

- Consider connecting the amplifier to an input voltage source and an output load resistance.



We now have a pair of potential dividers.

$$V' = V_{in} \frac{R_{in}}{R_{in} + R_s}$$

$$V_{out} = A V' \frac{R_L}{R_L + R_{out}}$$

$$\therefore \frac{V_{out}}{V_{in}} = A \cdot \frac{R_{in}}{R_{in} + R_s} \cdot \frac{R_L}{R_L + R_{out}}$$

The max. gain of the circuit  $\frac{V_{out}}{V_{in}}$  is the gain of the amplifier  $\frac{A V'}{V'} = A$ , which can be

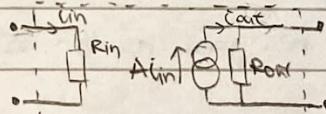
achieved when  $R_{in} \gg R_s$  and  $R_L \gg R_{out}$ .  $\rightarrow \frac{R_{in}}{R_{in} + R_s} = 1$  and  $\frac{R_L}{R_L + R_{out}} = 1$ .

→ We often want an amplifier circuit w/ high  $R_{in}$  and low  $R_{out}$ .

\* Note the gain of the circuit  $\frac{V_{out}}{V_{in}}$  is different from the gain of the amplifier  $\frac{A V'}{V'} = A$ .

Other amplifiers.

- A current amplifier takes in an input current  $i_{in}(t)$  and returns an output current  $i_{out}(t)$ .



where  $A = \frac{i_{out}}{i_{in}}$  and the output impedance is now in // w/ the current source.

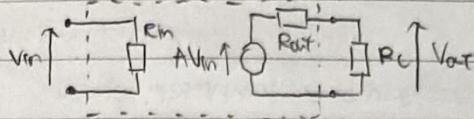
- A transimpedance amplifier takes in an input current  $i_{in}(t)$  and returns an output voltage  $V_{out}(t)$

- A transconductance amplifier takes in an input voltage  $V_{in}(t)$  and returns an output current  $i_{out}(t)$ .

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## Power of an amplifier circuit

- When analysing the performance of an amplifier, it is useful to consider the power that might be generated into a given load resistance  $R_L$ .



The powers of the input and output can be given as.

$$P_{in} = \frac{V_{in}^2}{R_{in}}$$

$$P_{out} = \frac{V_{out}^2}{R_L}$$

$$\therefore A_p = \frac{P_{out}}{P_{in}} = \frac{V_{out}^2 R_L}{V_{in}^2 R_{in}} = \left( \frac{V_{out}}{V_{in}} \right)^2 \frac{R_L}{R_{in}}$$

Using the decibel scale,

$$G_p = 20 \log_{10} \left( \frac{P_{out}}{P_{in}} \right)$$

- We can achieve max. power transfer to the load when  $R_{out} = R_L$ .

Potential divider at output:

$$V_{out} = A_{V_{in}} \frac{R_L}{R_L + R_{out}}$$

Power supplied to load:

$$P_L = \frac{V_{out}^2}{R_L} = \frac{(A_{V_{in}})^2}{R_L} \left( \frac{R_L}{R_L + R_{out}} \right)^2$$

$$= (A_{V_{in}})^2 \frac{R_L}{(R_L + R_{out})^2}$$

$R_L$  is the only variable:

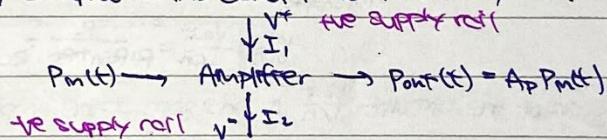
$$\frac{dP_L}{dR_L} = 0$$

$$0 = (A_{V_{in}})^2 \left[ \frac{(R_L + R_{out})^2 - 2R_L(R_L + R_{out})}{(R_L + R_{out})^4} \right]$$

$$\cancel{2R_L(R_L + R_{out})} = (R_L + R_{out})^2$$

$$\boxed{R_{out} = R_L}$$

- The output power  $P_{out}$  can be greater than the input power  $P_{in}$  because the amplifier's external power supply can provide this extra power. (usually DC power supply).

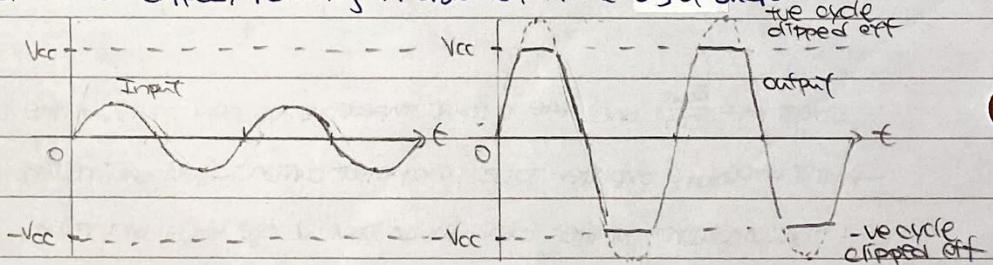


The power of the power supply is given by  $P_{dc} = V^+ I_1 + V^- I_2$

- The efficiency of an amplifier is defined as.

$$\eta = \frac{\text{output power}}{\text{total power supplied}} = \frac{P_{out}}{P_{out} + P_{in}}$$

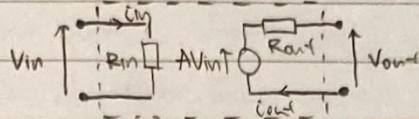
- The DC power supply of the amplifier also sets up the max. pos. and neg. output voltage swing of the output.  $\rightarrow V^- \leq V_{out} \leq V^+$
- If the gain is too high and the voltage tries to exceed the power supply's voltage, the output signal will be clipped, resulting in distortion in the signal shape.



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Evaluating the parameters for the amplifier model.

- To find the gain and input impedance, we can simply refer to the original circuit.



$$A = \frac{V_{out}}{V_{in}}$$

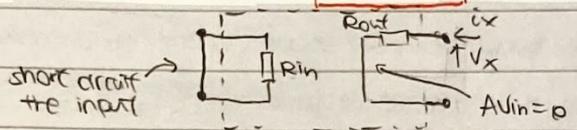
$$R_{in} = \frac{V_{in}}{I_{in}}$$

- To find the output impedance, we first have to short out the input to avoid any effects of the input voltage source / impedance. (so  $R_{out}$  is not a function of  $V_{in}$ ,  $R_{in}$ ).

Now, apply a test voltage  $V_x$  across the output terminals and measure the test current  $i_x$ .

We define the output impedance  $R_{out}$  as

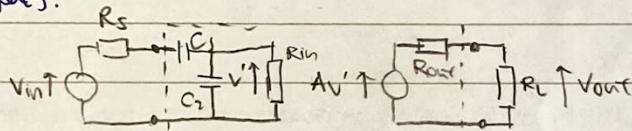
$$R_{out} = \frac{V_x}{i_x}$$



\* Use standard nodal analysis to find a relationship between  $V_x$  and  $i_x$ .

## Frequency response of an amplifier

- the frequency response of an amplifier may be affected by the gain (can be a function of frequency) and only reactive components of the input (output).
- consider an amplifier w/ a bandpass filter at the input (similar to op-amp for a bandpass filter at the output).



$C_1$  acts as a HPF;  $C_2$  acts as a LPF  $\rightarrow C_1 + C_2$  act as a BPF (passes midband freq.)

We assume  $C_1 \gg C_2$  so their effects on the frequency response of the amplifier can be considered separately.

$$Z_C = \frac{1}{j\omega C}$$

At low frequencies, we only consider  $C_1$  and assume  $C_2$  is an open circuit ( $Z_{C2} \ll Z_{C1}$ )

$$V' = V_{in} \cdot \frac{R_m}{R_s + j\omega C_1 + R_m} = V_{in} \cdot \frac{j\omega C_1 R_m}{1 + j\omega C_1 (R_s + R_m)}$$

Lower cut-off frequency (of high pass filter) when

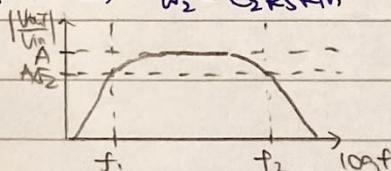
$$1 = \omega C_1 (R_s + R_m) \rightarrow \omega_1 = \frac{1}{C_1 (R_s + R_m)} , f_1 = \frac{1}{2\pi C_1 (R_s + R_m)}$$

At high frequencies, we only consider  $C_2$  and assume  $C_1$  is a short circuit ( $Z_{C1} \gg Z_{C2}$ )

$$V' = V_{in} \cdot \frac{\frac{R_m}{R_s + j\omega C_1 R_m}}{\frac{R_m}{R_s + j\omega C_2 R_m}} = V_{in} \cdot \frac{R_m}{R_s (1 + j\omega C_2 R_m) + R_m}$$

Upper cut-off frequency (of low pass filter) when

$$f_2 = \omega_2 = \frac{R_s + R_m}{C_2 R_s R_m} , f_2 = \frac{1}{2\pi C_2 R_s R_m}$$



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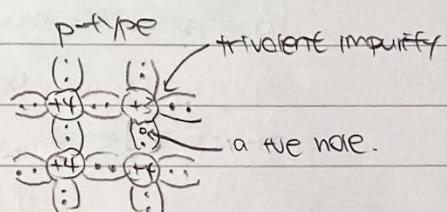
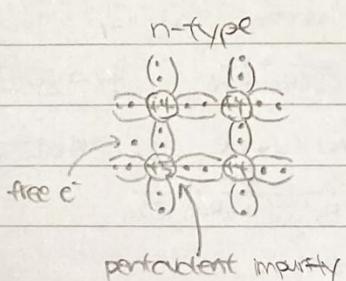
## Semiconductors and diodes

### Semiconductors

- A semiconductor is insulating at low temp., and conducting at high temp.  $\rightarrow$  non-linear
  - Semiconductors have a low  $e^-$  density  $\rightarrow$  incorporating dopant atoms can dramatically alter its properties.
  - Silicon (Si) is the most common semiconductor. Si has a tetrahedral structure and each atom forms 4 covalent bonds w/ neighbouring Si atoms.
  - At low temp., the covalent bonds are strong  $\rightarrow$  bonding  $e^-$  do not have enough energy to break free and move through the crystalline structure  $\rightarrow$  act as insulator.
  - At high temp., bonding  $e^-$  have enough energy to overcome covalent bond  $\rightarrow$  the  $e^-$  can move through the crystalline structure freely  $\rightarrow$  act as conductor.
- + Even at room temp., the atoms/ $e^-$  have thermal energy ( $E = k_B T$ ). Although the average thermal energy  $\approx 25\text{ meV}$  is insufficient to overcome the covalent bond  $\approx 1.1\text{ eV}$ , (from the Maxwell-Boltzmann distribution, there is a finite prob. a small no. of  $e^-$  can break free  $\rightarrow$  weakly conducting).
- When an  $e^-$  becomes delocalised, it effectively leaves behind a free hole
  - If we apply an electric field, the  $e^-$  and holes can move  $\rightarrow$  current.  
( $e^-$  move opp dir. to E field ; holes move same dir. as E field).

### Doping silicon.

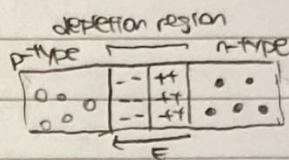
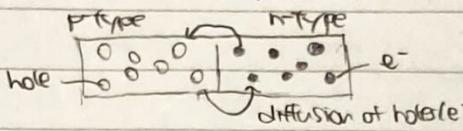
- The conductivity of Si can be increased considerably by the addition of impurities (dopants).
- To add delocalised  $e^-$ , we dope w/ a pentavalent metal (P, Sb, As); To add holes, we dope w/ a trivalent metal (B, Ga, In)
- The conc. of dopants is typically in the range of 1 per  $10^5$ - $10^8$  Si atoms.
- If we add a pentavalent dopant atom, 1 of the 5 valence  $e^-$  is freed  $\rightarrow$  n-type;  
If we add a trivalent dopant atom, we have 1 free hole  $\rightarrow$  p-type.



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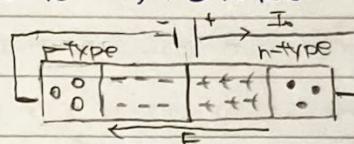
## The p-n junction and diodes

- The p-n junction is where the doping abruptly changes from p-type to n-type.
- When the junction is formed,  $e^-$  diffuse from n-type to p-type; holes diffuse from p-type to n-type. This results in a depletion region where there are no free  $e^-$  or holes.
- This produces an electric field which opposes diffusion. The potential associated with this electric field is the contact/built-in potential. ( $\sim 0.7\text{V}$  for Si).



When no ext. voltage is applied, there is no net flow of current across a p-n junction.

- If we apply an ext. voltage as follows, this is known as reverse biasing.

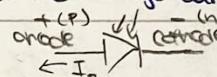


More  $e^-$  will be removed from the n-type and more holes will be removed from the p-type.

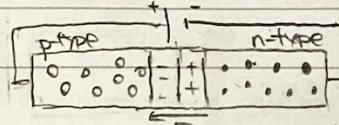
→ This increases the size of the depletion region.

- There will also be a reverse saturation/leakage current  $I_0$  ( $\text{nA}$ ) when reverse biased.

↳ Increase in light density increases the leakage current  $I_0$ .

↳ Such devices are photodiodes.  (acts like a current source)

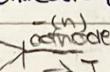
- If we reverse the ext. voltage as follows, this is known as forward biasing.

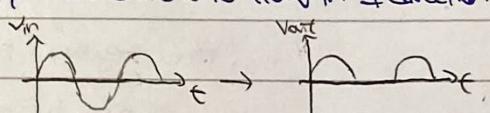


More holes/ $e^-$  pushed towards the junction by the two terminals in the p-type/n-type respectively.

→ This decreases the size of the depletion region. (No depletion region when  $V_{ext} = V_{bi} \approx 0.7\text{V}$ )

- This characteristic of the p-n junction of allowing significantly more current to flow in 1 direction when forward biased is known as rectification.

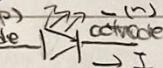
↳ Such devices are diodes 



- When a diode is forward biased,  $e^-$  moving across the depletion region can fall into the empty holes from the p-type layer →  $e^-$  drop from conduction band to valence band.

→ energy released in the form of photons.

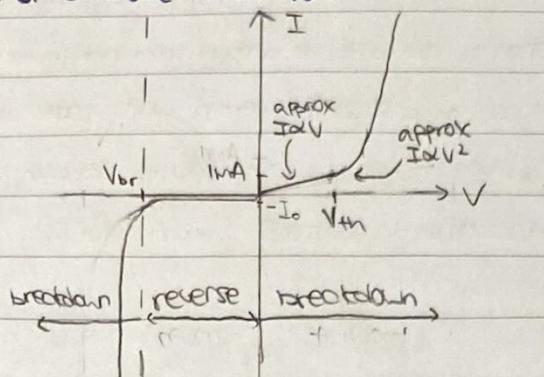
→ The energy difference between bands, hence frequency of light emitted depends on the material.

↳ Such devices are light-emitting diodes (LED). 

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I-V characteristic of a diode

- The I-V characteristic of a diode is as follows.



where  $V_{th}$  is the threshold voltage ( $\sim 0.7V$  for Si,  $\sim 0.25V$  for Ge).

$I_0$  is the reverse saturation current ( $\sim 1nA$ ).

$V_{br}$  is the breakdown voltage ( $\sim 150V$ ).

- The forward bias relationship between  $I$  and  $V$  (ideal diode eqn.)

$$I(V) = I_0 \left[ \exp\left(\frac{qV}{kT}\right) - 1 \right] \quad \text{for } V \geq V_{br}$$

where  $q$  is the electronic charge

$\eta$  is the ideality factor ( $\frac{1}{2}$  for Si, 1 for Ge).

For small voltages around the threshold voltage  $V_{th}$ ,  $I \propto V^2$  (approximately).

Load line and operating point.

- Plotting the load line on the I-V characteristic of the diode, the intersection of the 2 lines gives the operating pt. of the diode.

- We can find the load line by finding an eqn. for the circuit involving the pd across the diode  $V_D$  and the current through the diode  $I_D$ , then make  $I_D$  the subject (function of  $V_D$ ).

e.g. Find the load line and the operating pt.

KCL at node A:  $\frac{6-V_A}{100} + \frac{4-V_A}{100} + \frac{V-V_A}{200} = 0$ .

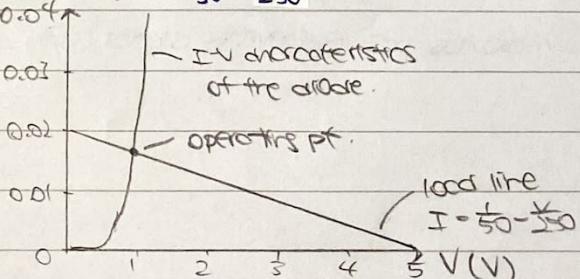
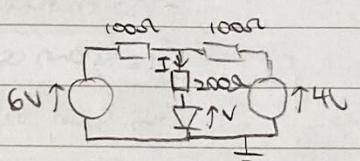
$$V_A = \frac{20+V}{5}$$

Consider the  $200\Omega$  resistor:

$$I = \frac{V_A - V}{200}$$

$$= \frac{20+V}{5(200)} - \frac{V}{200}$$

$$I(A) = \frac{1}{50} - \frac{V}{250}$$



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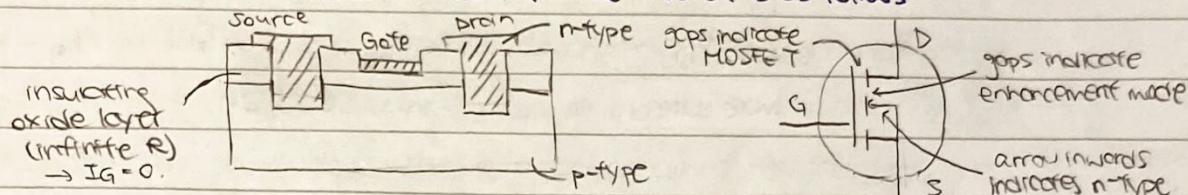
## Metal Oxide Semiconductor Field Effect Transistor

Metal oxide semiconductor field effect transistor (MOSFET).

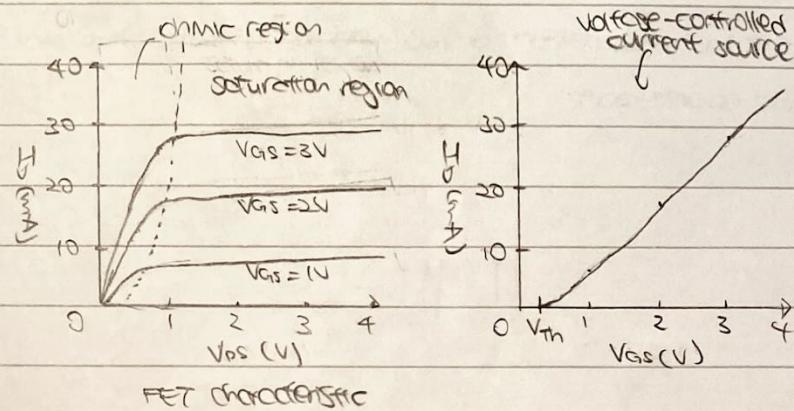
- MOSFETs are a type of FET, where its output is controlled by input voltage.
- All MOSFETs have 3 connections - gate (G), drain (D), source (S). charge carrier moves from source to drain
- MOSFETs can be categorized as n-channel/p-channel and enhancement mode/depletion mode,
  - ↳ n-channel: driven by  $e^-$  ; p-channel: driven by holes
  - ↳ enhancement mode: gate voltage  $V_G$  only +ve ; depletion mode: gate voltage  $V_G$  +ve or -ve.

The n-channel enhancement mode MOSFET.

- The structure of a n-channel enhancement mode MOSFET is as follows :



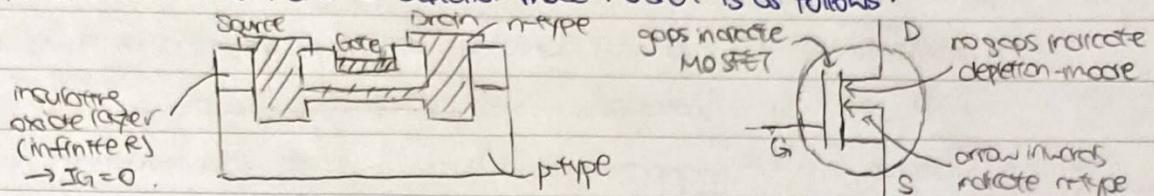
- If a voltage is applied between the drain and source ( $V_{DS}$ ), when there is no gate voltage ( $V_{GS}=0$ ), no drain current will flow ( $I_D=0$ ) as one of the p-n junctions will always be reverse biased  $\rightarrow$  no charge carriers in the space between the drain and the source.
- If a +ve gate voltage is applied ( $V_{GS}>0$ ), there will be an electric field between the gate and the bottom of the MOSFET  $\rightarrow$  attract  $e^-$  to the interface between the gate oxide and the p-type substrate (some  $e^-$  from p-type substrate but most  $e^-$  from n-type region of drain/source)
- For a large enough gate voltage ( $V_{GS} > V_{th}$ ) enough  $e^-$  will accumulate in between the drain and the source  $\rightarrow$  inversion layer (n-type conducting channel inside the p-type substrate)
- If we now apply a voltage between the drain and source ( $V_{DS}$ ), a drain current ( $I_D$ ) will flow through this inversion layer.
- For small values of  $V_{DS}$ ,  $I_D$  increases linearly + rapidly  $\rightarrow$  ohmic region.
- For larger values of  $V_{DS}$ , the voltage between the gate and drain ( $V_{GD}$ ) decreases, reducing the no. of  $e^-$  in the inversion layer so  $I_D$  levels off  $\rightarrow$  saturation region.



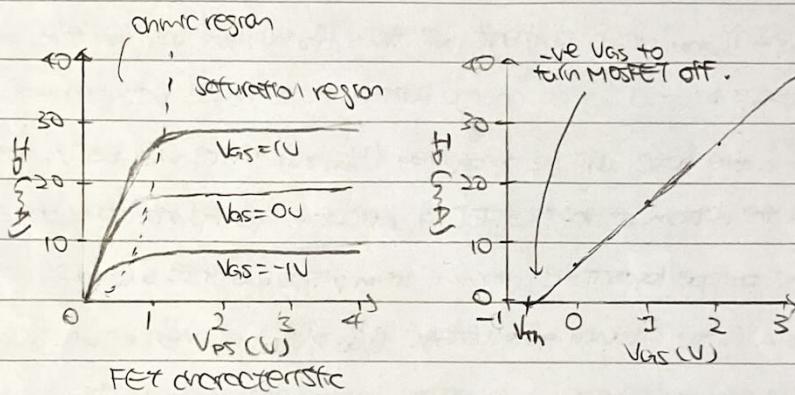
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The n-channel depletion mode MOSFET

- The structure of a n-channel depletion mode MOSFET is as follows:



- If a voltage is applied between the drain and source ( $V_{DS}$ ), there is a drain current ( $I_D$ ) even when there is no gate voltage ( $V_{GS} = 0$ )
- The application of a +ve gate voltage ( $V_{GS} > 0$ ) has the same effect as the enhancement mode, but a negative gate voltage ( $V_{GS} < 0$ ) sets up an electric field that repels e<sup>-</sup> away from the n-type channel → conductivity decreases. (No n-type channel for v. ve  $V_{GS}$  → not conductive)
- The conduction of the n-type channel is controlled by the +ve and -ve  $V_{GS}$  → depletion mode MOSFET better suited to bipolar signals (AC signals).
- The graphs are very similar to that of the enhancement mode, but the gate voltages  $V_{GS}$  are shifted down slightly (so  $V_{GS}$  can be -ve).



p-type MOSFETs.

- The working principles are exactly the same as n-type, but the polarities are reversed.  
n-type → p-type ; p-type → n-type ; +ve  $V_{GS}$  → -ve  $V_{GS}$  ; attract e<sup>-</sup> → attract holes etc.
- The characteristic and graphs are exactly the same but everything is -ve.  
(alternatively, we can change  $V_{GS} \rightarrow V_{GS}$ ,  $V_{DS} \rightarrow V_{SD}$ ,  $I_{DS} \rightarrow I_{SD}$  instead).
- + Note some measurement devices/software give the same plot for p-type as their n-type counterpart.

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Safe operating region of a FET.

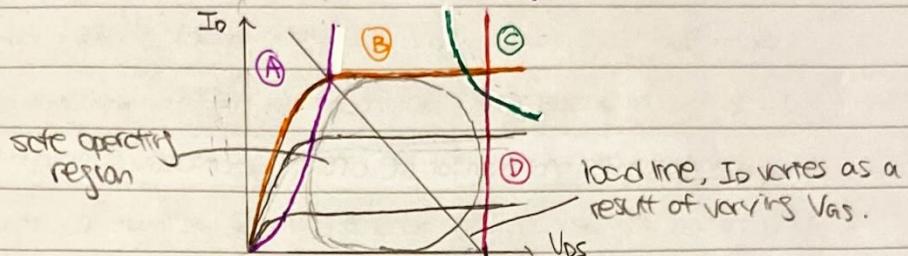
- The FET characteristic sets the safe operating region (or forbidden zones) for the circuit based on the following limiting factors

↳ ① : Non-linear, (for  $I_D$ ,  $V_{GS}$ ) , low-resistance region.

↳ ② : Max. limit of  $V_{GS}$ . If  $V_{GS} > V_{GSmax}$ , the oxide layer blows up.

↳ ③ : Max. power dissipation limit,  $(V_{DS}I_D)_{max}$ . If  $V_{DS} > V_{DSmax}$ , the FET becomes v. hot.

↳ ④ : Max. value of  $V_{DS}$ . If  $V_{DS} > V_{DSbreak}$ , the FET gets destroyed.



- Ideally, the load line should cross diagonally through the safe operating region and the operating pt. should be as central as possible (to allow for max. swing abt. the operating pt.).

Designing FET based circuits.

- There are 2 stages to designing any FET circuit:

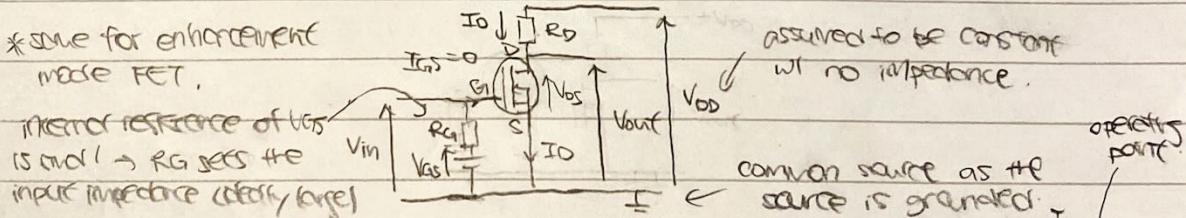
↳ 1) DC analysis (DC biasing, operating pt.)

↳ 2) AC analysis (small signal model)

- Although these are analysed separately, the decisions made in one design will directly affect the other through the choice of components at each design stage.

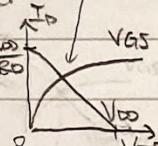
**DC analysis: Common source amplifier.**

- The circuit for a common source amplifier is as follows:



- Considering resistor  $R_D$ ,  $I_D = \frac{V_{DD} - V_{DS}}{R_D} = -\frac{1}{R_D}V_{DS} + \frac{V_{DD}}{R_D}$  → load line

$V_{GS}$  is seen by the voltage source.



- We can plot the load line on the FET characteristic. The intersection of the curves give the operating pt. (Determined by choice of  $V_{GS}$ ,  $V_{DS}$ ,  $I_D$ ).

- If  $I_D/V_{DS}$  is unspecified, we choose  $V_{DS} = \frac{V_{DD}}{2}$  for maximum voltage swing of the output

- We can estimate the gain of the circuit graphically :  $G_m = \frac{\Delta V_{out}}{\Delta V_{in}} = \frac{\Delta V_{DS}}{\Delta V_{in}}$  (Xslope).

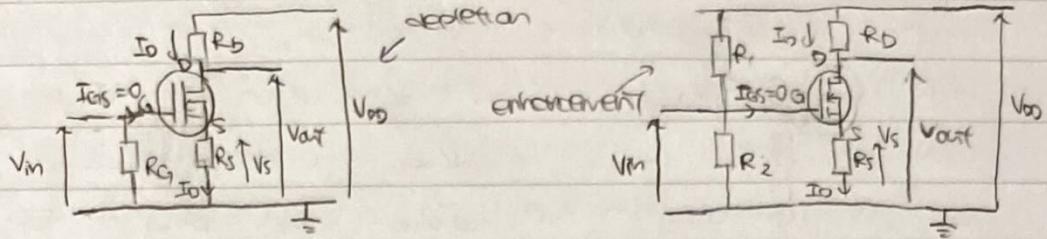
(In this case, we have -ve gain, (inverting amplifier), i.e. signals get inverted)

↳ -ve gain in dB means the signal is attenuated. ( $|A|/|A_{in}| < 1$ )

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DC analysis: self-biased amplifier.

- The circuit for a self-biased amplifier is as follows:



- Considering resistor  $R_d$ ,  $I_D = \frac{V_{DD} - V_{DS}}{R_d} = -\frac{1}{R_d} V_{DS} + \frac{V_{DD}}{R_d}$   $\rightarrow$  load line.

$$V_{AS} = V_{DS} - V_S ; \quad V_{AS} = -I_D V_S \text{ (depletion mode)} ; \quad V_{DS} = V_{DD} \cdot \frac{R_2}{R_1 + R_2} - I_D V_S \text{ (enhancement mode)}$$

- If  $I_D/V_{DS}$  is unspecified, we choose  $V_{DS} = \frac{V_{DD}}{2}$  for maximum voltage swing at the output.

\* we cannot estimate the gain of the circuit graphically as  $V_{out} = V_o$ , not  $V_{DS}$ .

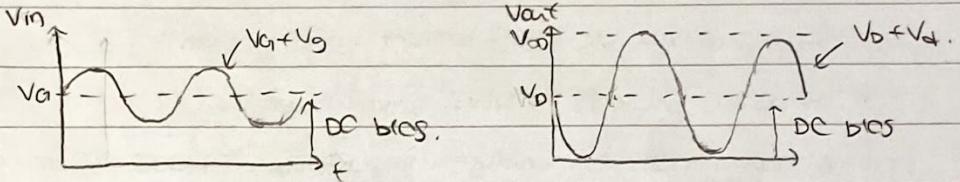
(In this circuit, we avoid the need for  $V_G$  as we have  $R_s$ . However  $R_s$  reduces the gain of the circuit (AC SSM)).

DC analysis: variables in upper case  
AC analysis: variables in lower case

Motivation for small signal model (SSM).

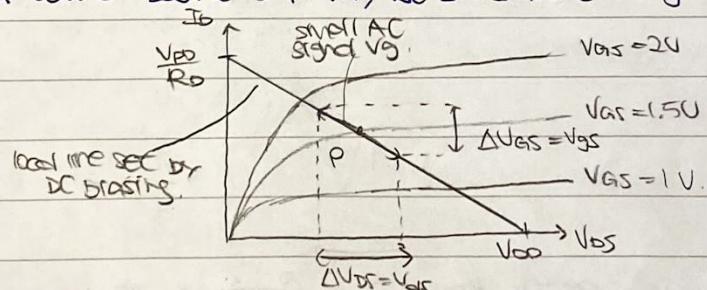
- When there is no input/output connected, (steady state),  $V_{in} = V_g$ ,  $V_{out} = V_o$ .

When a small signal  $v_g$  is applied at the input,  $V_{in} = V_g + v_g$ .  $V_{out} = V_o + v_o$ .



- When we apply the small signal  $v_g$  at the input, we are changing  $V_{DS}$ ,  $I_D$  and  $V_{DS}$  accordingly, and shifting the operating pt. slightly. ( $\hookrightarrow$  see how these parameters change as a result of  $v_g$ ). (Graphically, we are moving up/down the load line).

- In the case of a common source amplifier, we can estimate the gain of the circuit graphically.



The gain is given by  $\boxed{\text{Gain} = \frac{\Delta V_{DS}}{\Delta V_{GS}} = \frac{V_{GS}}{V_{GS}}}$

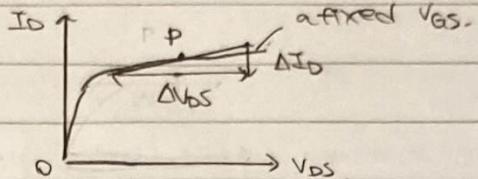
- Although the graphical method works for AC analysis, it is tedious to plot and is quite inaccurate  $\rightarrow$  we need a new model: Small signal model (SSM).

(SSM is a mathematical model for the FET  $\rightarrow$  draw drawing graphs).

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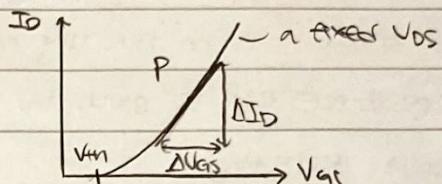
AC analysis: small signal model (SSM)

- We can use 2 parameters to describe the AC properties of the FET characteristic. (i.e. How  $V_{DS}$ ,  $V_{GS}$ , and  $I_D$  affect each other)
- FIRST, we consider the  $I_D$  vs  $V_{DS}$  characteristic w/ fixed  $V_{GS}$ ,



To describe what happens if  $V_{DS}$  changes a bit around the operating pt. P, we can use the partial derivative:  $\Delta I_D = \frac{\partial I_D}{\partial V_{DS}}|_{V_{GS}} \Delta V_{DS}$ .

- Now consider the  $I_D$  vs  $V_{GS}$  characteristic w/ fixed  $V_{DS}$ .



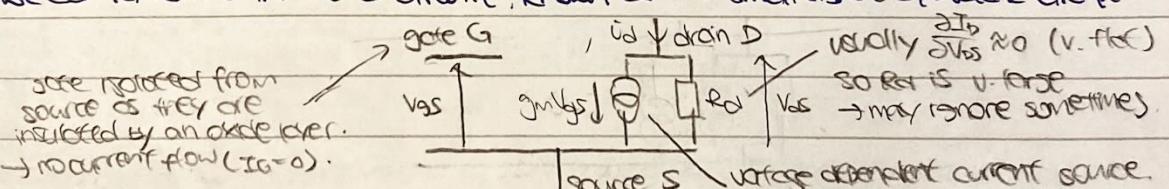
To describe what happens if  $V_{GS}$  changes a bit around the operating pt. P, we can use the partial derivative:  $\Delta I_D = \frac{\partial I_D}{\partial V_{GS}}|_{V_{DS}} \Delta V_{GS}$ .

- We can combine these 2 effects to express small change in  $I_D$  due to small changes in  $V_{DS}$  and  $V_{GS}$ :  $\Delta I_D = \frac{\partial I_D}{\partial V_{DS}}|_{V_{GS}} \Delta V_{DS} + \frac{\partial I_D}{\partial V_{GS}}|_{V_{DS}} \Delta V_{GS}$ .
- It is simpler to use parameters to represent the 2 changes that are defined by the FET characteristic — these are the small signal parameters for the FET.

$$\frac{\partial I_D}{\partial V_{DS}|_{V_{GS}}} = \frac{1}{R_d} \text{ drain resistance} ; \quad \frac{\partial I_D}{\partial V_{GS}|_{V_{DS}}} = g_m \text{ mutual conductance.}$$

- Also, using AC parameters, i.e.  $\Delta I_D = g_d$ ,  $\Delta V_{DS} = V_{DS}$ ,  $\Delta V_{GS} = V_{GS}$ , the above expression becomes:  $i_d = \frac{V_{DS}}{R_d} + g_m V_{GS}$

- We can represent this as a circuit, known as the small signal equivalent circuit

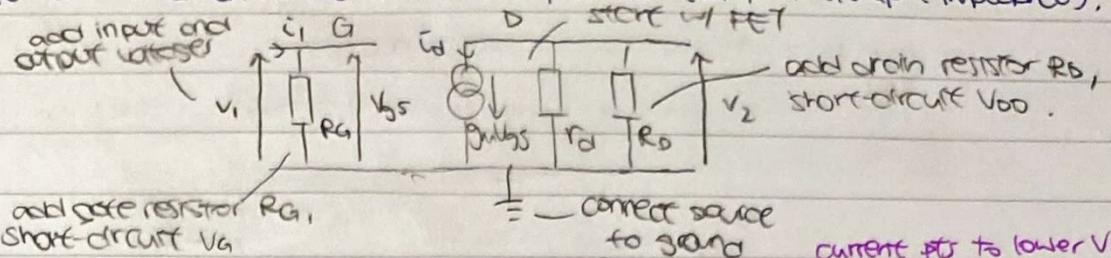


- Replacing the FET in the circuit w/ its equivalent model allows us to calculate the circuit's small signal properties — gain, input/output impedance.
- Any constant DC sources (e.g.  $V_{DD}$ ) are effectively not there, i.e. connected to GND as we cannot change it regardless of the AC input signal.
- Alternatively, we can treat the power supply as a very large capacitor. At high frequencies, it will have zero impedance ( $Z_C = j\omega C$ ) → connected to GND

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AC analysis: Common source amplifier (refer to DC analysis for circuit)

- we use SSM to determine the small signal properties (Gain, input/output impedance).



- At the input of the amplifier (Gate),  $V_1 = V_{GS}$

$$\text{At the output of the amplifier (Drain), } g_m V_{GS} = \frac{0 - V_2}{R_D // R_D} = -\frac{V_2}{R_D}$$

$$\text{Combining the 2 eqns, } g_m V_1 = -\frac{V_2}{R_D // R_D}$$

$$\frac{V_2}{V_1} = -g_m (R_D // R_D)$$

current pts to lower V;

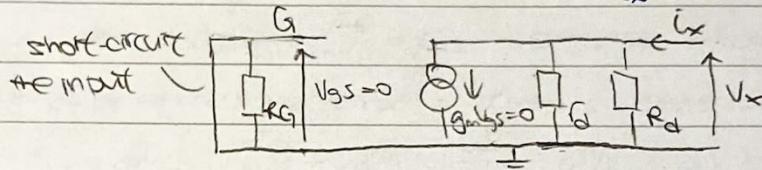
voltage pts to higher V.

\* The -ve sign shows it is an inverting amplifier (shifts phase by 180°).

- The input resistance  $R_{in}$  is given by  $R_{in} = \frac{V_1}{I_1}$

In this case,  $R_{in} = R_G$

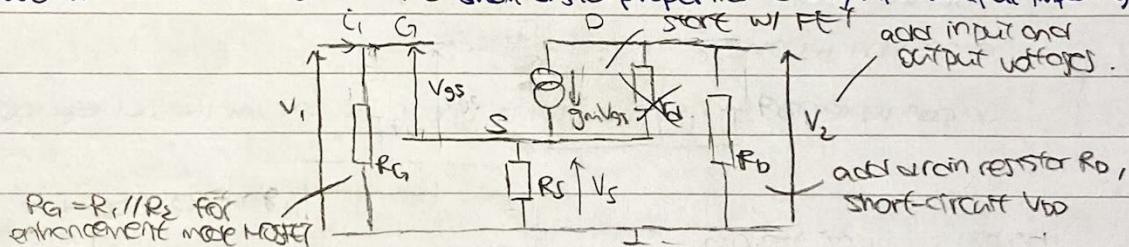
- The output resistance  $R_{out}$  is given by  $R_{out} = \frac{V_x}{I_x}$ , provided we shorted the input.



In this case,  $R_{out} = R_D // R_D$ . (specific result!)

AC analysis: Self-biased amplifier (refer to DC analysis for circuit).

- we use SSM to determine the small signal properties (Gain, input/output impedance).



To simplify analysis, we assume that  $I_D$  is very large  $\rightarrow$  can be ignored.

- At the input of the amplifier (Gate),  $V_1 = V_{GS} + V_S$ .

$$\text{At the output of the amplifier (Drain), } g_m V_{GS} = \frac{0 - V_2}{R_D} = -\frac{V_2}{R_D} \rightarrow V_2 = -g_m V_{GS} R_D$$

$$\text{At the source, } g_m V_{GS} = \frac{V_S - 0}{R_S} = \frac{V_S}{R_S} \rightarrow V_S = g_m V_{GS} R_S$$

$$\text{Combining the 3 eqns, } V_1 = V_{GS} + g_m V_{GS} R_S = V_{GS} (1 + g_m R_S)$$

$$\therefore \frac{V_2}{V_1} = -\frac{g_m V_{GS} R_D}{V_{GS} (1 + g_m R_S)} = -\frac{g_m R_D}{1 + g_m R_S}$$

\* The -ve sign shows it is an inverting amplifier (shifts phase by 180°).

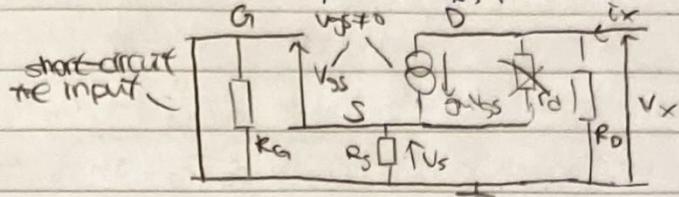
\*  $R_S$  reduces the value of the gain but is a critical part of setting the operating pt.

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- The input resistance  $R_{in}$  is given by  $R_{in} = \frac{V_1}{I_1}$

In this case,  $R_{in} = R_G$ .

- The output resistance  $R_{out}$  is given by  $R_{out} = \frac{V_x}{I_x}$ , provided we shorted the input.



We cannot find  $R_{out}$  if we neglect  $R_D$ . However, we can say  $R_{out} \approx R_D$ ,

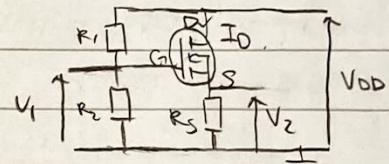
(say  $R_D \rightarrow \infty$ ). As impedance of voltage source is equal its // impedance, the total impedance of the  $V_{GS}, R_S$  branch  $\rightarrow \infty$ , i.e. can be ignored, so  $R_{out} \approx R_D$ .

\* If we included  $R_D$  in the SSM,  $\frac{V_2}{V_1} = -\frac{g_m R_D}{R_D + g_m R_F R_D + R_S + R_D}$ ;

$$R_{in} = R_G ; R_{out} = \frac{R_D (R_S + R_D (1 + g_m R_S))}{R_D + R_S + R_D (1 + g_m R_S)}$$

AC analysis: Source follower.

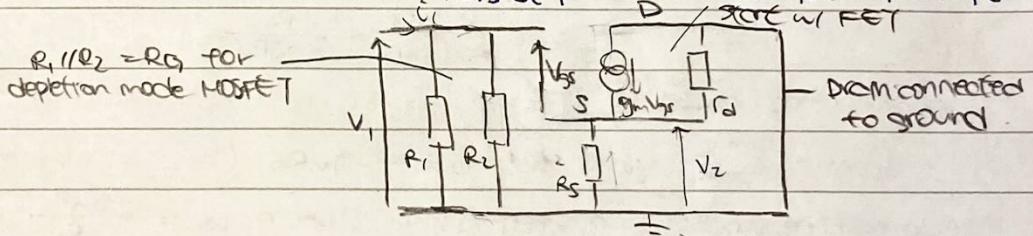
- The circuit for a source follower is as follows :



(For completeness - DC analysis:  $V_2 = I_D R_S$ ,  $V_{DS} = V_{DD} - V_2 \therefore I_D = -\frac{1}{R_S} V_{DS} + \frac{V_{DD}}{R_S}$ ).

The intersection between the load line and the FET characteristic gives the operating pt.

- We use SSM to determine the small signal properties (Gm, input/output impedance).



- At the input of the amplifier (Gate),  $V_1 = V_{GS} + V_2$

At the output of the amplifier (Drain/Source),  $g_m V_{GS} = \frac{V_2 - 0}{R_D // R_S} = \frac{V_2}{R_D // R_S} \rightarrow V_2 = g_m V_{GS} (R_D // R_S)$

Combining the 2 eqns,  $V_1 = V_{GS} + g_m V_{GS} (R_D // R_S) = V_{GS} (1 + g_m (R_D // R_S))$

$$\therefore \frac{V_2}{V_1} = \frac{g_m V_{GS} (R_D // R_S)}{V_{GS} (1 + g_m (R_D // R_S))} = \frac{g_m (R_D // R_S)}{1 + g_m (R_D // R_S)}$$

\* Most of the time  $g_m (R_D // R_S) \gg 1$ , so  $1 + g_m (R_D // R_S) \approx g_m (R_D // R_S) \therefore \frac{V_2}{V_1} \approx 1$  (buffer).

- The input resistance  $R_{in}$  is given by  $R_{in} = \frac{V_1}{I_1}$

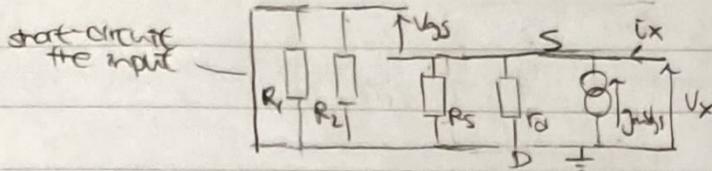
In this case,  $R_{in} = R_1 // R_2$

\* We can basically find  $R_{in}$  by inspection -  $R_{in}$  is either equal to  $R_G$  or  $R_1 // R_2$ .

$(R_1 // R_2$  if no ext. voltage source is used and an enhancement mode FET is used).

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- The output resistance  $R_{out}$  is given by  $R_{out} = \frac{V_x}{i_x}$ , provided we shorted the input.



- At the source node,  $V_K = -V_{GS}$ .

At the source and drain nodes,  $i_x + g_m V_{GS} = \frac{V_x - 0}{R_S / |R_d|} \rightarrow i_x = \frac{V_x}{R_S / |R_d|} - g_m V_{GS}$ .

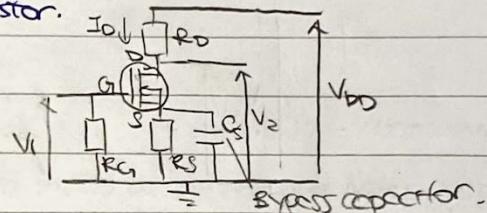
Combining the 2 eqns,  $i_x = \frac{V_x}{R_S / |R_d| + g_m} = V_x (R_S / |R_d| + g_m)$ .

$$\therefore \frac{V_x}{i_x} = \frac{1}{R_S / |R_d| + g_m} = \frac{R_S / |R_d|}{1 + g_m (R_S / |R_d|)}$$

- The circuit has a gain of 1 w/ a high input resistance and low output resistance. It is commonly used as a buffer - separating different circuits that may interfere w/ each other.

## AC analysis: Bypass capacitors

- For a self-biased amplifier, we add a resistor  $R_S$  to set the operating pt. However,  $R_S$  reduces the overall gain of the amplifier.
- This can be avoided by adding a bypass capacitor in parallel w/  $R_S$  to allow AC current to bypass the resistor.



Now  $R_S$  is effectively replaced by  $Z_S$ , where  $Z_S = R_S // Z_C$

$$Z_S = \frac{R_S / j\omega C_S}{R_S + j\omega C_S} = \frac{R_S}{1 + j\omega R_S C_S}$$

For high frequencies AC, ( $\omega \rightarrow \infty$ ),  $Z_S \rightarrow 0$  (or when  $\omega R_S C_S \gg 1$ )

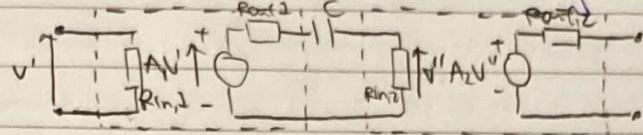
$\therefore G_{am} = -\frac{g_m R_D}{1 + j\omega R_S C_S}$  tends to  $G_{am} = -g_m R_D$ . (Same as common source amplifier)  
(We have reasonable gain when  $\omega > \omega_c$ , where  $\omega_c = \frac{1 + j\omega R_S C_S}{C_S R_S}$ ).

## AC analysis: (de)coupling capacitors

- If it is okay to connect the power supplies (assuming some  $V_{DD}$ ) and the ground connections.
- However, we cannot connect the output of the 1st circuit w/ the input of the 2nd circuit as they were designed w/ diff. operating pts  $\rightarrow$  add a decoupling capacitor to prevent DC current from flowing from one circuit to another.

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- From the BIM model, we can determine  $R_{in}$  and  $R_{out}$  for each circuit. From this, we can determine the suitable capacitance of the decoupling capacitor.



$R_{out1} + Z_C$  and  $R_{out2}$  form a potential divider (high pass filter).  $\rightarrow$  losses.

$$\text{Gain} = \frac{V''_3}{V''_1} = \frac{R_{in2}}{Z_C + R_{out1} + R_{in2}} = \frac{j\omega C R_{in2}}{1 + j\omega C (R_{out1} + R_{in2})}$$

.. cut off frequency  $f_c$  given by

$$1 = \omega C (R_{out1} + R_{in2})$$

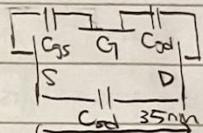
$$f_c = \frac{1}{2\pi C (R_{out1} + R_{in2})}$$

- We also often use decoupling capacitors at the inputs and outputs of each amplifier circuit to protect the load / input sources. (Same method as above to find the cut off frequency  $f_c$ ).

AC analysis : Miller effect.

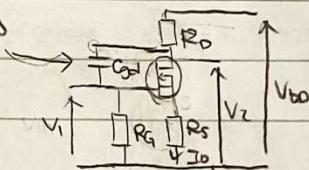
- In a real FET, we get unwanted / parasitic capacitance which occurs due to the small distances between the (metal) electrodes that make the transistor.

- Typical values :  $C_{sd} \sim 1\text{pF}$ ;  $C_{ds} \sim 2\text{pF}$ ;  $C_{gs} \sim 5\text{pF}$



\*  $C_{gd}$  is the most important  $\rightarrow$  connect input and output.

the capacitor could allow the input signal to bypass the amplifier.



- In general, for any capacitor which connects the input of an amplifier to its output, there are losses / affected bandwidth due to the Miller effect.

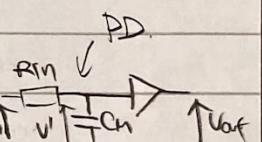
$$\begin{aligned} V_{out} &= A V_{in} \\ C_C &= \frac{V_{out} - V_{in}}{Z_C} \\ &= \frac{V_{in}(1-A)}{j\omega C} \end{aligned}$$

$$\begin{aligned} \text{LPF} &\quad \text{actually there is also a} \\ &\quad \text{capacitance at the output,} \\ &\quad C_{H2} = (1-A)C. \end{aligned}$$

$$\begin{aligned} \frac{1}{j\omega C} &= \frac{1}{j\omega C_H} (1-A) \\ C_H &= (1-A)C \end{aligned}$$

$$\therefore \frac{1}{j\omega C} = \frac{1}{j\omega C_H} (1-A)$$

Miller capacitance  $\rightarrow C_H = (1-A)C$  increases w/ gain.



- We effectively have a potential divider (low pass filter)  $\rightarrow$  losses  $V_{in} \uparrow \frac{1}{1 + \frac{1}{j\omega C_H}}$ . The cut off frequency  $f_c$  is given by

$$f_c = \frac{1}{2\pi C_H R_f} \quad (\text{standard result}).$$

..  $\uparrow A \rightarrow \uparrow C_H \rightarrow f_c \downarrow \rightarrow \downarrow f_{H2}(\text{BW})$ . (as we have a low pass filter)

- Instead of 1 amplifier w/ large gain  $\rightarrow$  cascade multiple amplifiers w/ smaller gain.

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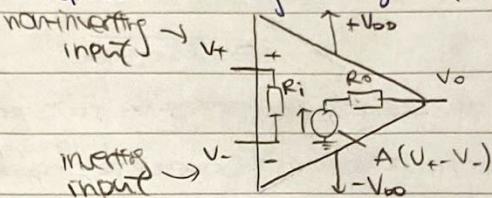
## Designing FET circuits

- 1) choose a suitable FET ( $g_m$ ,  $f_0$ , price)
- 2) choose an operating pt. ( $I_D$ ,  $V_{DS}$ ,  $V_{GS}$ )  $\rightarrow$  calculate resistors ( $R_o$ ,  $R_{in}$ ,  $R_S$ ) or  $R_1, R_2$   
adjust  
accordingly
- 3) use SSM of the circuit to calculate gain, input/output resistance ( $G_i$ ,  $R_{in}$ ,  $R_{out}$ )

## Operational amplifiers (OpAmps)

### Ideal OpAmp.

- An opamp can be represented using a single symbol (one model).



- OpAmps can work w/ DC and AC input voltages and are usually supplied by a bipolar or dual power supply.

- An ideal opamp has the following properties:

↳ Infinite open-loop gain,  $A = \infty$        $\rightarrow$  Infinite input resistance,  $R_i = \infty$

↳ Zero output resistance,  $R_o = 0$ ,

↳ As the gain  $A$  is infinite and the output voltage  $V_o = A(V_+ - V_-)$  is finite,  $V_+ - V_- = 0$

↳ Infinite input resistance  $R_i$  means there is no current into either input,  $i_+ = i_- = 0$

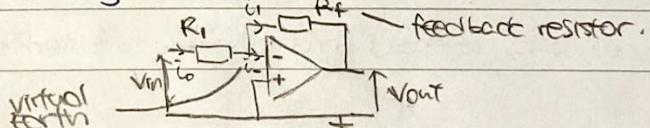
Voltage rule

$V_+ - V_- = 0$

current rule

### Inverting OpAmp.

- The circuit of an inverting opamp is as follows:



- Using the voltage rule,  $V_+ = V_- = 0$  (Ground),  $V_-$  is referred to as virtual earth, since  $V_+ = 0$ .

Using the current rule,  $i_+ = i_- = 0 \quad \therefore i_o = i_+ + i_- = 0$

$$i_o = \frac{V_{in} - 0}{R_i} = i_1 = \frac{0 - V_{out}}{R_f}$$

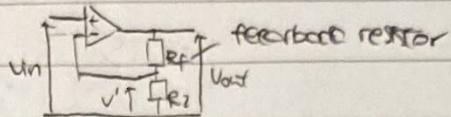
$$\rightarrow \frac{V_{out}}{V_{in}} = -\frac{R_f}{R_i} \quad (\text{closed loop gain})$$

- The opamp is inverting because the (closed loop) gain of the circuit is  $-ve$ , i.e. the output is  $180^\circ$  out of phase w/ the input.

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Non-inverting OpAmp.

- The circuit of a non-inverting OpAmp is as follows:



- Using the voltage rule,  $V_+ = V_- = V_{in} = V'$

$$\text{Consider the potential divider, } V' = V_{out} \cdot \frac{R_2}{R_f + R_2}$$

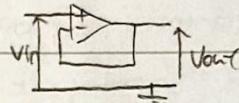
$$V_{in} = V_{out} \cdot \frac{R_2}{R_f + R_2}$$

$$\rightarrow \frac{V_{out}}{V_{in}} = \frac{R_f + R_2}{R_2} = 1 + \frac{R_f}{R_2} \quad (\text{closed loop gain})$$

- The OpAmp is non-inverting because the (closed loop) gain of the circuit is true, i.e. the output is in phase w/ the input

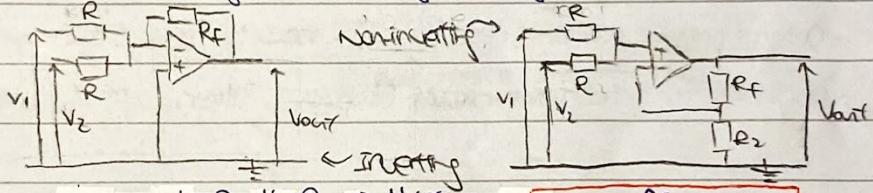
- A special type of non-inverting OpAmp is the voltage follower, where  $R_f = 0$  and  $R_2 = \infty$ .

The resulting circuit would have a (closed loop) gain of 1 (Buffer), i.e.  $\frac{V_{out}}{V_{in}} = 1$



Summing amplifier: ✓ voltages connected to same input

- The circuit of an inverting/non-inverting summing amplifier is as follows:



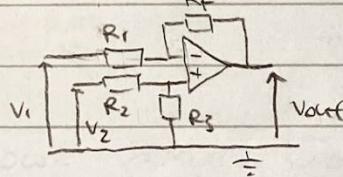
$$\text{- Inverting} \leftarrow \text{KCL: } \frac{V_1 - 0}{R_1} + \frac{V_2 - 0}{R_2} = \frac{0 - V_{out}}{R_f} \rightarrow V_{out} = -\frac{R_f}{R} (V_1 + V_2)$$

$$\text{Noninverting} \leftarrow \text{PD: } V_+ = (V_1 - V_2) \cdot \frac{R_1}{R_1 + R_2} + V_2 = \frac{V_1 + V_2}{2} = V_-$$

$$\text{PD: } V_- = \frac{V_1 + V_2}{2} = V_{out} \cdot \frac{R_2}{R_2 + R_f} \rightarrow V_{out} = \left(1 + \frac{R_f}{R_2}\right) \left(\frac{V_1 + V_2}{2}\right).$$

Difference amplifier: ✓ voltages connected to different inputs.

- The circuit of a difference amplifier is as follows:



- Superposition:  $V_{out} = V_{out,1} + V_{out,2}$

$$V_{out,1} \leftarrow \text{set } V_2 = 0 \rightarrow \text{Inverting OpAmp} \quad \therefore V_{out,1} = -V_1 \frac{R_f}{R_1}$$

$$V_{out,2} \leftarrow \text{set } V_1 = 0 \rightarrow \text{PD: } V_+ = V_2 \frac{R_3}{R_2 + R_3} = V_-$$

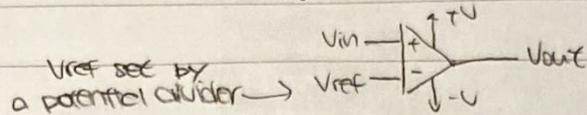
$$\text{KCL: } -\frac{V_-}{R_1} = \frac{V_{out} - V_-}{R_f} \rightarrow V_{out,2} = V_2 \left( \frac{R_3}{R_2 + R_3} \right) \left( 1 + \frac{R_f}{R_1} \right)$$

$$\therefore V_{out} = V_2 \left( \frac{R_3}{R_2 + R_3} \right) \left( 1 + \frac{R_f}{R_1} \right) - V_1 \frac{R_f}{R_1}$$

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## Voltage Comparator

- The circuit of a simple voltage comparator is as follows:



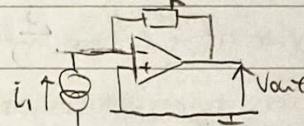
- If  $V_m > V_{ref}$ , then  $V_{out} = +V$ ; If  $V_m < V_{ref}$ , then  $V_{out} = -V$ .

↳ The ideal opamp has infinite gain ( $A = \infty$ ), so if  $V_+ > V_-$ ,  $V_{out} = +V$ ;  $V_+ < V_-$ ,  $V_{out} = -V$ ,

However, the max. voltage available to the output is set by the bipolar supply rails  $\pm V$ .

## Transimpedance amplifier.

- The circuit of a transimpedance amplifier is as follows:



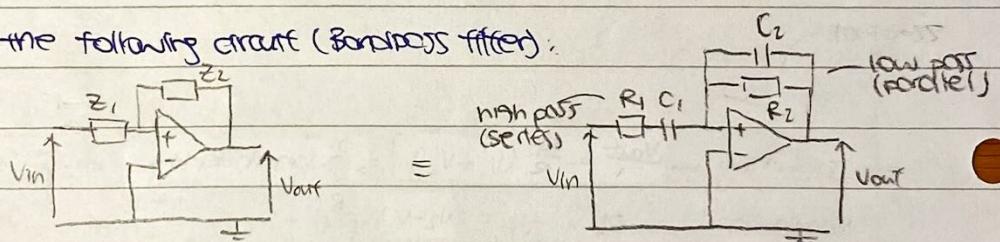
- A transimpedance amplifier takes in an input current  $i_i$ , and gives an output voltage  $V_{out}$ , so the gain is effectively an impedance. —  $\frac{V_{out}}{i_i} = R$

\* Transimpedance amplifiers useful for converting a light signal into a voltage signal.

## Opamps circuits with reactive components

- Opamps can be used w/ reactive components to make frequency dependent circuits.

- Consider the following circuit (Bandpass filter):



$R_1, C_1$  act as a HPF;  $R_2, C_2$  act as a LPF  $\rightarrow R_1 C_1, R_2 C_2$  act as a BPF (passes midband freq.)

We assume  $C_1 \gg C_2$  so their effects on the frequency response can be considered separately.

$$Z_1 = R_1 + \frac{1}{j\omega C_1} = R_1 \left(1 + \frac{1}{j\omega C_1 R_1}\right)$$

$$\therefore \frac{V_{out}}{V_{in}} = -\frac{Z_2}{Z_1} = -\frac{R_2}{R_1} \left(\frac{1}{1 + j\omega C_1 R_1}\right) \left(\frac{1}{1 + j\omega C_2 R_2}\right)$$

midband gain      LPF      HPF  
high freq cutoff      low freq cutoff

From this, we can see that:

$$\hookrightarrow \text{midband gain} = \frac{R_2}{R_1}$$

$$\hookrightarrow \text{lower cut-off frequency is given by } 1 = \omega C_1 R_1 \rightarrow f_1 = \frac{1}{2\pi C_1 R_1}$$

$$\hookrightarrow \text{upper cut-off frequency is given by } 1 = \omega C_2 R_2 \rightarrow f_2 = \frac{1}{2\pi C_2 R_2}$$

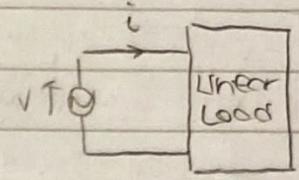
## AC Power

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### AC POWER

AC power supplied to a linear load.

- consider a general linear load connected to a sinusoidal voltage source  $V$ . This voltage causes a sinusoidal current  $i$  to flow in the load.



- Mathematically,

$$v(t) = \hat{V} \cos(\omega t + \alpha) \quad [V = V e^{j\alpha}] \quad i(t) = \hat{I} \cos(\omega t + \beta) \quad [I = I e^{j\beta}]$$

- Instantaneous power  $p(t)$  is defined as  $p(t) = v(t)i(t)$ , so

$$\text{for a linear circuit, } p(t) = \hat{V} \cos(\omega t + \alpha) \hat{I} \cos(\omega t + \beta)$$

$$= \hat{V} \hat{I} \cdot \frac{1}{2} [\cos(2\omega t + \alpha + \beta) + \cos(\alpha - \beta)]$$

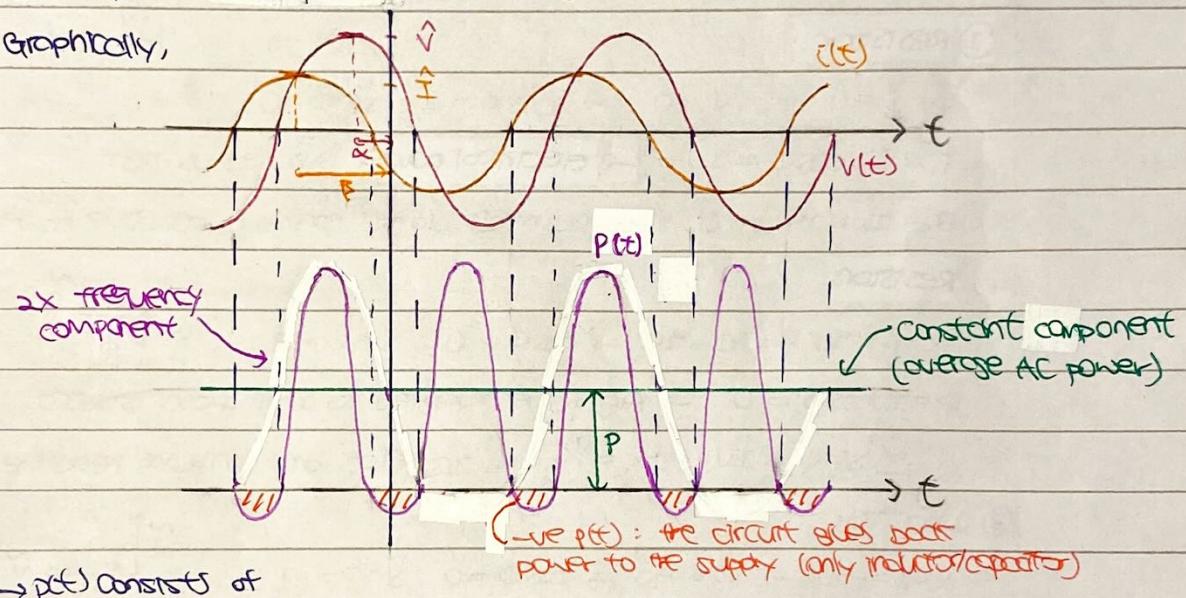
$$= \frac{\hat{V}}{2} \frac{\hat{I}}{2} [\cos(\omega t + \alpha + \beta) + \cos(\alpha - \beta)]$$

$$= VI [\cos(\omega t + \alpha + \beta) + \cos(\alpha - \beta)]$$

where  $V$  is the rms voltage and  $I$  is the rms current  $[V = \frac{\hat{V}}{\sqrt{2}}, I = \frac{\hat{I}}{\sqrt{2}}]$ .

- In AC power, if unspecified, the values given are always rms.

- Graphically,



$\rightarrow p(t)$  consists of

(i) 2x frequency component [average value zero].

(ii) constant component

∴ the constant component is the average AC power. (Real power).

- Real power is given by

$$P = VI \cos(\alpha - \beta) = VI \cos\phi.$$

where we define  $\phi$  to be the angle of the voltage wrt current. ( $\phi = \alpha - \beta$ ).

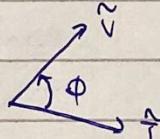
- $\phi$  is the load angle and  $\cos\phi$  is the power factor.

↳  $\phi > 0 \rightarrow$  lagging power factor [inductive loads]

↳  $\phi < 0 \rightarrow$  leading power factor [capacitive loads]

↳  $\phi = 0 \rightarrow$  unity power factor [resistive loads]

\*  $\phi$  opposite sign of phase angle of  $I$  (wrt.  $V$ ).



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Real power and reactive power

- resolve the phasor current  $\tilde{I}$  into 2 components:

(i)  $\tilde{I}_d$  - in phase w/ the voltage

(ii)  $\tilde{I}_q$  - 90° out of phase w/ the voltage (quadrature)

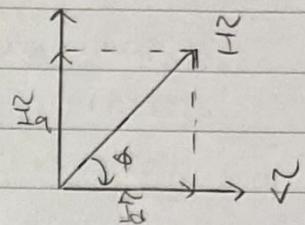
$$\rightarrow I_d = I \cos \phi, I_q = I \sin \phi.$$

- we define real power  $P = V I_d = V I \cos \phi$

[units: W]

reactive power  $Q = V I_q = V I \sin \phi$

[units: VAR].

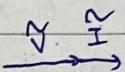


- while real power is the power dissipated and converted into another form in the load, reactive power is the power that travels between the supply and the load (but is never dissipated)

\* Although P and Q are dimensionally identical, they cannot be simply added together  $\rightarrow$  we give them different units.

Power of passive components.

## ① Resistor



$$\alpha - \beta = 0^\circ \rightarrow \phi = 0^\circ \rightarrow \cos \phi = 1, \sin \phi = 0.$$

$$P = IV \cos \phi = IV = I^2 R = \frac{V^2}{R} \rightarrow \text{Power dissipated as heat.}$$

$$Q = IV \sin \phi = 0. \rightarrow \text{Resistor do not consume reactive power.}$$

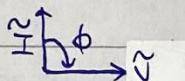
## ② Inductor

$$\alpha - \beta = 90^\circ \rightarrow \phi = 90^\circ \rightarrow \cos \phi = 0, \sin \phi = 1.$$

$$P = IV \cos \phi = 0 \rightarrow \text{Avg. power supplied to an inductor is zero}$$

$$Q = IV \sin \phi = IV = I^2 X_L = \frac{V^2}{X_L} \rightarrow \text{Inductors only consume reactive power}$$

## ③ Capacitor



$$\alpha - \beta = -90^\circ \rightarrow \phi = -90^\circ \rightarrow \cos \phi = 0, \sin \phi = -1,$$

$$P = IV \cos \phi = 0 \rightarrow \text{Avg. power supplied to a capacitor is zero.}$$

$$Q = IV \sin \phi = -IV = -I^2 X_C = -\frac{V^2}{X_C} \rightarrow \text{Capacitors only generate reactive power}$$

- Given a load with impedance  $Z_1 = R + jX$ , (R, X connected in series)

$$P = I^2 R, \quad Q = I^2 X.$$

- Given a load with impedance  $Z_2 = R // jX$ , (R, X connected in parallel)

$$P = \frac{V^2}{R}, \quad Q = \frac{V^2}{X}.$$

\* Remember to check the sign of Q. If the load is inductive  $\rightarrow$  +ve Q;

If the load is capacitive  $\rightarrow$  -ve Q.

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Apparent power and power triangle

- consider  $\bar{S} = \bar{V}\bar{I}$   
 $= VI e^{j(\alpha+\beta)}$ .

- $= VI [\cos(\alpha+\beta) + j\sin(\alpha+\beta)]$

- $= VI \cos\phi + jVI \sin\phi = P + jQ$ .

\*  $\bar{V}\bar{I}$  would give us  $P - Q$  instead.

We define apparent power  $S$  as  $|S| = |\bar{V}\bar{I}| = \sqrt{P^2 + Q^2}$ . [Currents: VA].

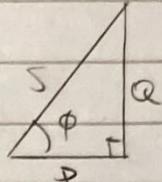
- We can construct the power triangle using  $P, Q, S, \phi$ .

- $\hookrightarrow \sin\phi = \frac{Q}{S}$

- $\hookrightarrow \cos\phi = \frac{P}{S}$

- $\hookrightarrow \tan\phi = \frac{Q}{P}$

- $\hookrightarrow S = \sqrt{P^2 + Q^2}$



- The apparent power  $S$  is simply  $S = VI$  → useful for finding  $V$  or  $I$ .

loads in series:  $\bar{V} = \sum \bar{V}_i$  so  $\bar{V}\bar{I}^* = \sum \bar{V}_i \bar{I}^*$

Conservation of  $P$  and  $Q$ .

loads in parallel:  $\bar{I} = \sum \bar{I}_i$  →  $\bar{I}^* = \sum \bar{I}_i^*$  so  $\bar{V}\bar{I}^* = \sum \bar{V}_i \bar{I}^*$

- By consu. of energy,  $\boxed{\bar{S} = \sum \bar{S}_i} \Rightarrow \boxed{\bar{V}\bar{I}^* = \sum (\bar{V}_i \bar{I}_i^*)}$

- $\hookrightarrow$  Equating real parts:  $\operatorname{Re}(\bar{S}) = \sum \operatorname{Re}(\bar{S}_i) \rightarrow \boxed{P = \sum P_i}$

- $\hookrightarrow$  Equating imaginary parts:  $\operatorname{Im}(\bar{S}) = \sum \operatorname{Im}(\bar{S}_i) \rightarrow \boxed{Q = \sum Q_i}$

- Although  $\bar{S} = \sum \bar{S}_i$ ,  $S = \sum S_i$  is only true iff  $\bar{S}_i$  are in phase.

- Consu. of  $P$  and  $Q$  is useful for finding the circuit's  $P$  and  $Q \rightarrow$  find  $S$ .

Engineering significance of power factor and correcting it

- Although no power is dissipated (lost) directly through the reactive power (as it is the power transferred between the supply and the load), there are indirect (real) power losses in the transmission lines.

- Having a reactive power means there is a larger current drawn → greater power loss (due to resistance) in the transmission lines.

- We can add a capacitor/inductor to obtain a unity power factor.

- To find the capacitance/inductance req., we set the total reactive power  $Q$  to be 0, i.e.  $Q = \sum Q_i = 0$

$\hookrightarrow$  If the original load was inductive ( $Q > 0$ ), we add a capacitor ( $Q < 0$ ).

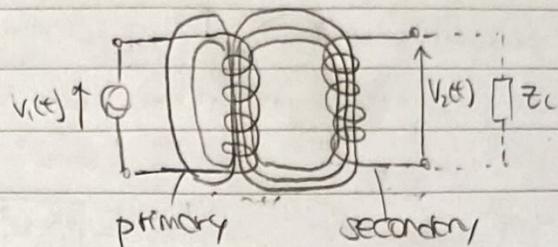
$\hookrightarrow$  If the original load was capacitive ( $Q < 0$ ), we add an inductor ( $Q > 0$ ).

- \* The newly added capacitor/inductor can be connected in series or in parallel to the original load, but the capacitance/inductance req. may be different.

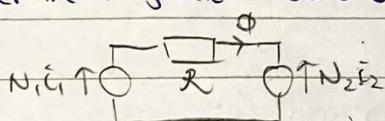
## Transformers

Basic principles of transformers.

- Transformers are used to convert electrical power from one voltage and current level to another.
- The simplest possible transformer consists of 2 coils of wire in close proximity.



- Primary connected to voltage supply  $\rightarrow$  current  $\rightarrow$  magnetic flux. The magnetic flux links the primary and partly links the secondary.  $V_1(t) \rightarrow I_1(t) \rightarrow \Phi(t)$
- If the primary voltage varies w/ time, magnetic flux varies w/ time so there is an emf induced in the secondary.  $e_2(t) = N \frac{d\Phi}{dt}$
- To improve the basic transformer, we can wind the primary and secondary coils around on iron core. (The iron core consists of many thin sheets of iron, i.e. lamination, to reduce the induced eddy currents in the core  $\rightarrow$  reduce core power losses).
- Consider the magnetic circuit of the transformer (flow of magnetic flux).



magnetic circuit	electric circuit
flux $\Phi$	current $I$
ampereturns (mmf) $NI$	voltage $V$
reluctance $R$	resistance $R$

$$\text{KVL (magnetic)} : N_1 i_1(t) = N_2 i_2(t) + R \Phi(t).$$

\* We use an iron core as iron is a good conductor of magnetic flux  $\rightarrow$  low reluctance.

Ideal transformer.

- There are 4 properties of an ideal transformer:

① Iron is a perfect conductor of magnetic flux  $\rightarrow R=0$ .

$$N_1 i_1 = N_2 i_2 + R \Phi^0.$$

$$\boxed{\frac{i_2}{i_1} = \frac{N_1}{N_2}} \quad \text{where } \frac{N_1}{N_2} \text{ is the turn ratio.}$$

As  $\frac{N_1}{N_2} \text{ eff}$ ,  $\frac{i_2}{i_1} \text{ eff}$ , i.e.  $i_1$  and  $i_2$  are in phase.

② All the flux linking primary also links secondary.  $\rightarrow \Phi = \Phi_1 = \Phi_2$ .

By Faraday's law,  $e_1 = N_1 \frac{d\Phi}{dt}$ ;  $e_2 = N_2 \frac{d\Phi}{dt}$

$$\therefore \frac{e_1}{N_1} = \frac{d\Phi}{dt} = \frac{d\Phi}{dt} = \frac{d\Phi}{dt} = \frac{e_2}{N_2}.$$

$$\rightarrow \boxed{\frac{e_1}{N_1} = \frac{e_2}{N_2}},$$

where  $e_1, e_2$  are the emf induced across the primary and secondary coils respectively.

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③ Winding resistances are negligible  $\rightarrow e_1 = v_1, e_2 = v_2$ .

\*  $e_1$  is the emf induced by the changing magnetic flux,  $v_1$  is the "terminal" p.d. across the coil. [ $v_1 = e_1 + iR_{\text{coil}}$ ].

As  $\frac{e_1}{N_1} = \frac{e_2}{N_2}$ , we get  $\frac{v_1}{N_1} = \frac{v_2}{N_2}$

$$\boxed{\frac{v_1}{v_2} = \frac{N_1}{N_2}} \quad \text{where } \frac{N_1}{N_2} \text{ is the turns ratio.}$$

As  $\frac{N_1}{N_2} \in \mathbb{R}$ ,  $\frac{v_1}{v_2} \in \mathbb{R}$ , i.e.  $v_1$  and  $v_2$  are in phase.

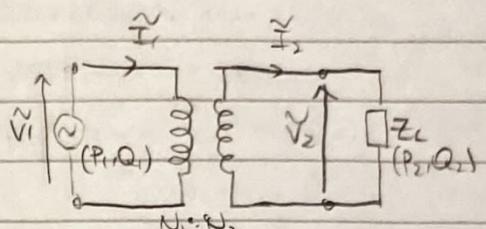
④ NO power losses occur in the iron core of the ideal transformer  $\rightarrow P_1 = P_2, Q_1 = Q_2$ .

\* consequence of properties ①, ②, ③.

$$\bar{s}_2 = P_2 + jQ_2 = \tilde{V}_2 \tilde{I}_2^* = \frac{N_2}{N_1} \tilde{V}_1 \cdot \frac{N_1}{N_2} \tilde{I}_1^* = \tilde{V}_1 \tilde{I}_1^* = \bar{s}_1$$

$$\rightarrow \boxed{\bar{s}_1 = \bar{s}_2}$$

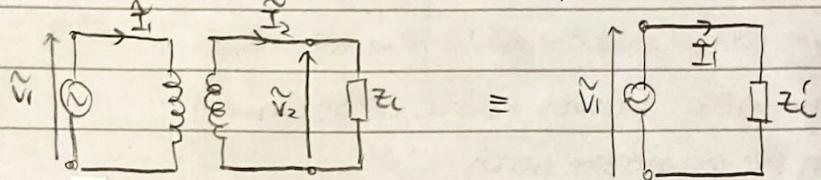
$$\therefore \text{Re: } P_1 = P_2 ; \text{Im: } Q_1 = Q_2$$



i.e. Ideal transformer does not consume any real or reactive power.

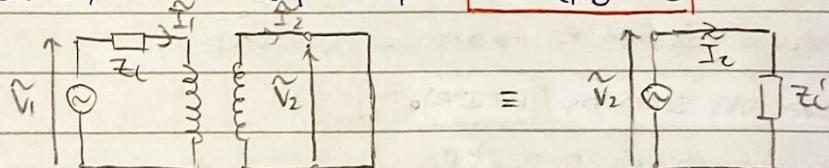
Impedance referral.

- We can refer impedance between the primary and the secondary.



$$Z'_1 = \frac{\tilde{V}_1}{\tilde{I}_1} = \frac{N_1^2 \tilde{V}_2}{N_1 N_2 \cdot \tilde{I}_2} = \left(\frac{N_1}{N_2}\right)^2 \cdot \frac{\tilde{V}_2}{\tilde{I}_2} = \left(\frac{N_1}{N_2}\right)^2 Z_L$$

$$\rightarrow \text{Secondary referred to primary: } \boxed{Z'_1 = \left(\frac{N_1}{N_2}\right)^2 Z_L}$$

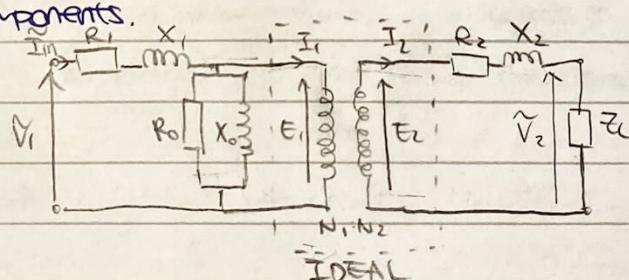


$$Z'_2 = \frac{\tilde{V}_2}{\tilde{I}_2} = \frac{N_2^2 \tilde{V}_1}{N_1 N_2 \cdot \tilde{I}_1} = \left(\frac{N_2}{N_1}\right)^2 \cdot \frac{\tilde{V}_1}{\tilde{I}_1} = \left(\frac{N_2}{N_1}\right)^2 Z_L$$

$$\rightarrow \text{Primary referred to secondary: } \boxed{Z'_2 = \left(\frac{N_2}{N_1}\right)^2 Z_L}$$

real transformer.

- To model a real transformer, we use an ideal transformer connected to additional components.



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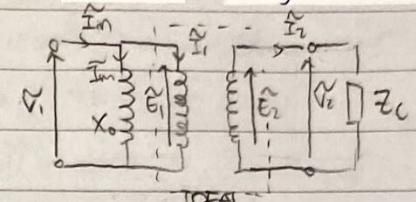
① Iron is not a perfect conductor of magnetic flux  $\rightarrow \mu \neq \infty$ .

consider the case where the secondary is not connected to a load. (i.e. an open-circuited transformer).  $\tilde{I}_2 = 0 \Rightarrow \tilde{I}_1 = \frac{N_2}{N_1} \tilde{I}_2 = 0$ .

Although  $\tilde{I}_1 = 0$ ,  $\tilde{I}_{m1} \neq 0$ . We have a magnetizing current  $I_m$  that produces a magnetizing flux  $\phi_m$  that opposes the input voltage, given by  $N_1 \tilde{V}_1 = R \tilde{\Phi}_m$ .

By Faraday's law,  $\tilde{E} = N_1 \frac{d\tilde{\Phi}_m}{dt} = N_1 j\omega \tilde{\Phi}_m = j \frac{WN^2}{R} I_m$  ( $\tilde{\Phi}_m = \phi_m e^{j\omega t}$ )  
 $\rightarrow \tilde{E} = jX_0 \tilde{I}_m$ , where  $X_0 = \frac{WN^2}{R}$

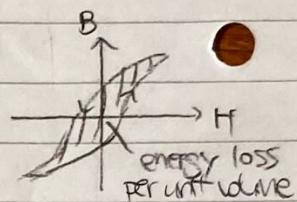
$\therefore$  we add an impedance  $jX_0$  in parallel with the primary.  
 $(X_0$  is the magnetizing reactance) (not series as  $I_1 = 0$ )



② There are power losses in the iron core due to

i. Hysteresis

$\rightarrow$  Energy loss when magnetizing/demagnetizing,  $\propto \phi_m^2 \propto E_1^2$   
(area under B-H curve x slug energy loss per unit volume).

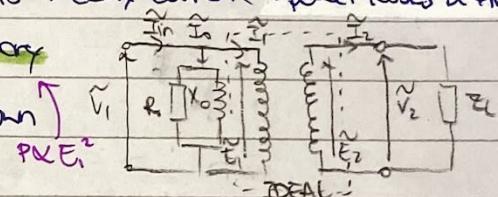


ii. Eddy current loss.

$\rightarrow$  Alternating flux induces emf in laminations  $\rightarrow$  eddy current  $\rightarrow$  power losses  $\propto \phi_m^2 \propto E_1^2$

$\therefore$  we add a resistance  $R_0$  in parallel with the primary

$\rightarrow$  the parallel branches  $R_0$  and  $X_0$  are known  
 as the magnetizing branch.



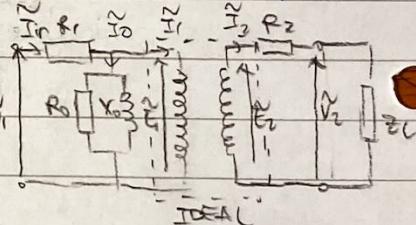
③ The windings in the primary/secondary have resistances  $R_1, R_2$  respectively.

$\therefore$  we add a resistance  $R_1$  in series with the primary

and a resistance  $R_2$  in series with the secondary

Primary power loss  $P_1 = I_{m1}^2 R_1$

Secondary power loss  $P_2 = I_{m2}^2 R_2$



④ Not all primary flux links secondary  $\rightarrow$  leakage flux  $\rightarrow$  additional voltage drop. main flux  $\phi_m$

$$\tilde{V}_{e1} = N_1 \frac{d\tilde{\Phi}_1}{dt} = j\omega N_1 \tilde{\Phi}_{e1} = j\omega N_1 L_{e1} \tilde{I}_{m1}$$

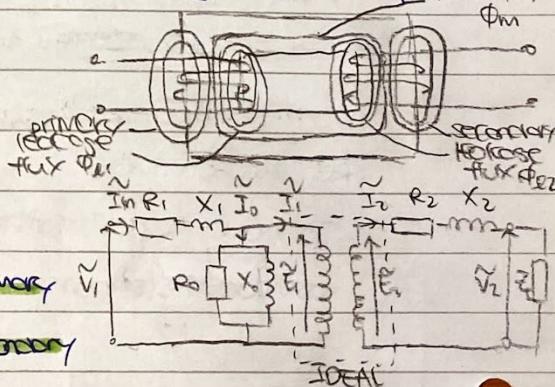
$$\rightarrow \tilde{V}_{e1} = jX_1 \tilde{I}_{m1} \quad \text{where } X_1 = \omega N_1 L_{e1}$$

$$\tilde{V}_{e2} = N_2 \frac{d\tilde{\Phi}_{e2}}{dt} = j\omega N_2 \tilde{\Phi}_{e2} = j\omega N_2 L_{e2} \tilde{I}_{m2}$$

$$\rightarrow \tilde{V}_{e2} = jX_2 \tilde{I}_{m2} \quad \text{where } X_2 = \omega N_2 L_{e2}$$

$\therefore$  we add an impedance  $jX_1$  in series with the primary

and an impedance  $jX_2$  in series with the secondary



\* For an ideal transformer,  $R_1, R_2, X_1, X_2 \rightarrow 0$ ;  $R_0, X_0 \rightarrow \infty$ .

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Simplifications on the equivalent circuit parameters

- We can refer  $R_2, X_2$  to the primary and add to  $R_1, X_1$ .

$$\hookrightarrow R'_2 = \left(\frac{N_1}{N_2}\right)^2 R_2$$

$$\therefore R_{\text{eq}} = R_1 + R'_2 = R_1 + \left(\frac{N_1}{N_2}\right)^2 R_2$$

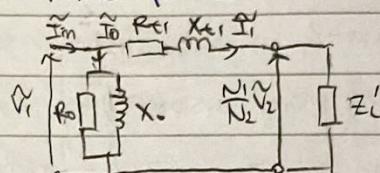
$$\hookrightarrow X'_2 = \left(\frac{N_1}{N_2}\right)^2 X_2$$

$$\therefore X_{\text{eq}} = X_1 + X'_2 = X_1 + \left(\frac{N_1}{N_2}\right)^2 X_2$$

- We can refer  $Z_L$  to the primary

$$\hookrightarrow Z'_L = \left(\frac{N_1}{N_2}\right)^2 Z_L$$

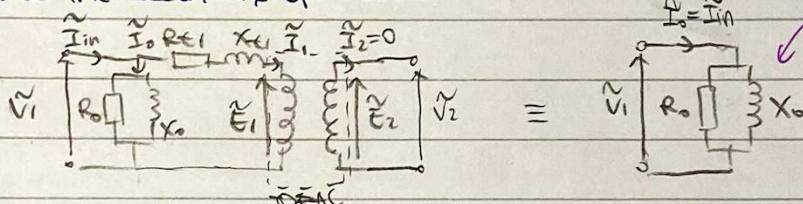
- Since the voltage drop across  $R_{\text{eq}}$  &  $X_{\text{eq}}$  is very small compared to  $R_0 \parallel jX_0$  (magnetizing branch), we can swap their places.



Determination of equivalent circuit parameters / turns ratio

## ① Open circuit test

- We have the secondary open-circuited.



parallel  $\rightarrow \frac{V^2}{R}$  or  $\frac{V^2}{X}$

$$\hookrightarrow \text{Open circuit} \Rightarrow I_2 = 0. \text{ Since } I_1 = \frac{N_2}{N_1} I_2, I_1 = 0. \rightarrow V_1 = E_1 \text{ and } V_2 = E_2.$$

$\therefore \frac{N_1}{N_2} = \frac{E_1}{E_2} = \frac{V_1}{V_2}$  i.e. turns ratio is the ratio of terminal voltages (open circuit).

↳ Referring to the equivalent circuit.

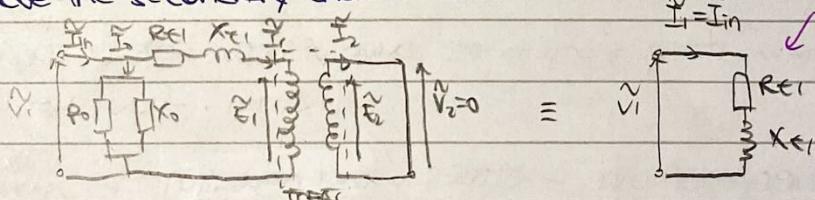
$$\text{Real power only consumed in } R_0: P = \frac{V_1^2}{R_0} \rightarrow R_0 = \frac{V_1^2}{P}$$

$$\text{Reactive power only consumed in } X_0: Q = \frac{V_1^2}{X_0} \rightarrow X_0 = \frac{V_1^2}{Q}$$

Find S  $\rightarrow$  find Q  
using  $Q = \sqrt{S^2 - P^2}$

## ② Short circuit test

- We have the secondary short-circuited.



series  $\rightarrow I^2 R$  or  $I^2 X$

$$\hookrightarrow \text{Short circuit} \Rightarrow V_2 = E_2 = 0. \text{ Since } E_1 = \frac{N_1}{N_2} E_2, E_1 = 0 \rightarrow R_{\text{eq}} + X_{\text{eq}} \parallel R_0, \parallel X_0.$$

As  $R_0, X_0 \gg R_{\text{eq}} + X_{\text{eq}}$ , we can ignore the magnetizing branch.

↳ Referring to the equivalent circuit.

$$\text{Real power only consumed in } R_{\text{eq}}: P = I_1^2 R_{\text{eq}} \rightarrow R_{\text{eq}} = \frac{P}{I_1^2}$$

Find S  $\rightarrow$  find Q  
using  $Q = \sqrt{S^2 - P^2}$

$$\text{Reactive power only consumed in } X_{\text{eq}}: Q = I_1^2 X_{\text{eq}} \rightarrow X_{\text{eq}} = \frac{Q}{I_1^2}$$

$$\therefore R_{\text{eq}} = \left(\frac{N_1}{N_2}\right)^2 R_2, X_{\text{eq}} = \left(\frac{N_1}{N_2}\right)^2 X_2$$

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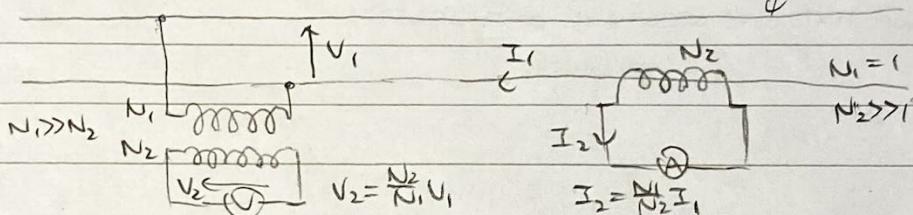
## Construction of transformers.

- Transformers are built differently depending on the frequency used.
    - ↳ Low frequency (e.g.: Power transformers) : laminated iron cores
    - ↳ High frequency (e.g.: Audio transformers) : powdered iron, ferrite or air core.
- eddy current losses increases w/  
frequency → avoid laminated iron cores.

## Uses of transformers.

- 1) To change AC voltage/current levels.
  - ↳ i. In power systems to improve efficiency of transmission  
(high voltage → low current → small power losses)  $240V \rightarrow 3.3V / 5V$
  - ↳ ii. In electronic equipment to transform mains voltage to a suitable voltage.
- 2) To provide circuit isolation — primary and secondary winding are only connected by flux → protect low voltage side from high voltage side.
- 3) Instrumentation — measurement of high voltages/currents (w/o a transformer, the voltmeter/ammeter would break).

↓ transmission line.



## Transformer rating.

- Transformers are limited by
  - ↳ Windings currents : Excessive current → large copper loss → winding becomes hot due to eddy currents + hysteresis
  - ↳ Windings voltages : Excessive voltage → large iron loss → iron core becomes hot.
- Transformers are given a volt-amp rating : Rating (in VA) =  $V_{rated} I_{rated} = V_{2rated} I_{2rated}$   
(heating effect depends only on current/voltage magnitude, not on the angle between them)
- The volt-amp rating is prop. to the volume of active material (i.e. copper and iron)

high efficiency → low power losses → good.

## Transformer performance - efficiency

- Efficiency  $\eta$  is defined as 
$$\eta = \frac{\text{output power}}{\text{input power}} = \frac{P_{out}}{P_{in}}$$
- By conservation of power,  $P_{in} = P_{out} + P_{losses}$ .
- Power losses in iron core are iron losses / fixed losses : 
$$P_{Fe} = \frac{V^2}{R_0}$$
 Independent on the connected load → variable losses.
- Power losses in windings are copper losses / variable losses : 
$$P_{Cu} = I^2 R_{Fe} + I^2 R_{Copper}$$
- The total power loss is given by  $P_{loss} = P_{Fe} + P_{Cu}$  due to resistive heating of the windings.
- \* Ideal efficiency is 100% ( $\eta = 0.78 - 0.97$  is good)

small regulation  $\rightarrow$  load voltage independent of load current  $\rightarrow$  good

### Transformer performance - regulation

- Regulation measures change in load voltage from open-circuit voltage due to load current  $i_N$  is defined as 
$$\text{Regulation} = \frac{V_{2oc} - V_2}{V_{2oc}}$$
- The numerator is the voltage drop across parasitic  $R_{K2}, X_{K2}$ .
- \* Total regulation is 0% (Regulation = 0.03-0.05 is good).