Multi-Stage Tuned Amplifier

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Contents

1 Objective

To compare the operation of common-emitter and common-base tuned amplifier stages, and to design and characterize a multi-stage, high-gain IF amplifier for 10 MHz operation with 50Ω input and output impedances.

2 Principles of Operation

Tuned amplifiers are critical for electronic communications because they increase the power of desired signal but reject other frequencies as noise. At 10 MHz, a tuned amplifier could be used with an antenna to recieve HF amateur radio from the other side of the world [1], or could be used in a computer to recieve 10Base-T ethernet.

There are three possible circuit configurations for bipolar junction transistors (BJT) biased in forward-active mode, based on which terminals are used for input, output, and common reference.

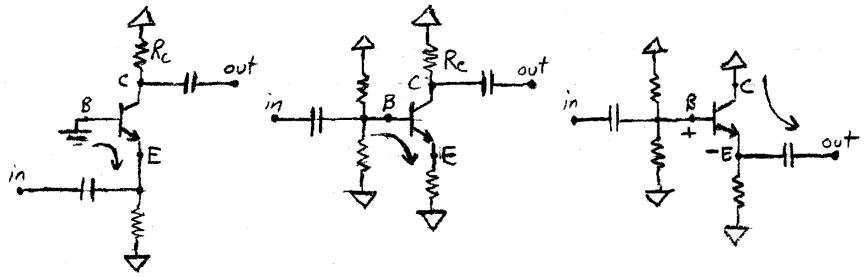

Figure 1: Common-base (left), common-emitter (middle), and common-collector (right) configurations for BJT amplifiers.

Each configuration has its tradeoffs. The common-base (CB) configuration is a good current buffer, with $A_i \approx 1$ and low input impedance. The common-emitter (CE) configuration offers the best overall power gain, but A_v and A_i may vary with loadings. The common-collector configuration is a good voltage buffer ($A_v \approx 1$) with low output impedance.

The three configurations can be cascaded together to gain the benefits of each. If cascaded in the order shown in figure 1, from left-to-right, the resulting 3-stage broadband amplifier would have low input impedance, good power gain, and minimal output impedance.

A slight modification to the CE and CB configurations in figure 1 can apply a filter to the broadband amplifier; tuning the gain to a narrow frequency set by a tank circuit.

Because BJTs are minority carrier devices, they act as current amplifiers without being strongly affected by voltage. For the two configurations where the output is at the collector (CB and CE), the BJT acts like a dependent current source feeding the output load and the biasing resistance R_C. As a result, the voltage gain for these configurations is determined primarily by how difficult it is for the collector current to reach ground; $A_v \propto R_C||R_L$.

One can take advantage of the collector current's obstinance by replacing R_C with an impedance that varies with frequency. Using an inductor and a capacitor in parallel provides a short circuit to ground for both DC and high frequency currents. Additionally, at the LC circuit's resonant frequency, the net impedance $\to \infty$ due to power oscillating between the two. [2] The result is a narrow bandpass filter at the resonant frequency, where $Z_C \to \infty$.

[1] 10 MHz waves can traverse the curve of the earth because they get reflected by charged particles in the ionosphere, called ionospheric skip propagation.

[2] For this reason, an $L||C$ circuit is called a tank circuit.

3 Theory

3.1 Tank Circuits

No inductor is ideal. The quality of an inductor is defined by the ratio of the impedance and resistance of the discrete element.

$$Q = \frac{X_L}{R_S} \qquad \text{where} \qquad Z_L = R_S + jX_L$$

The series resistance R_S is due to the resistivity of the wire and the length used to wrap the coil. Furthermore, the impedance X_L is not 100% inductive; there is a distributed capacitance C_D between the surfaces of the tightly wrapped wire. The circuit model for an inductor is shown in the left pane of figure 2.

As a consequence of the distributed capacitance, every inductor will have a self resonant frequency f_0, at which the energy entering the tank will oscillate between the inductor and capacitor instead of passing through.

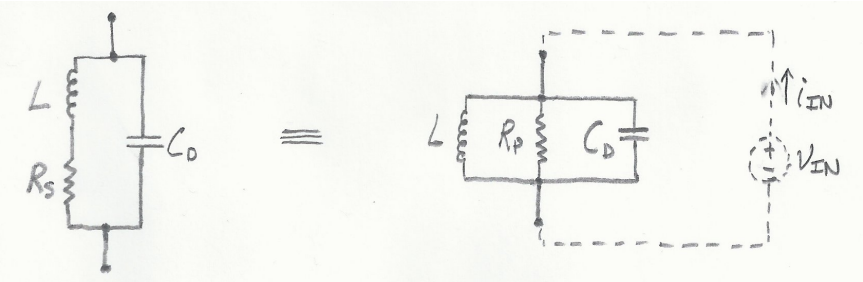

Figure 2: Circuit model for a non-ideal inductor (left) and its parallel equivalent circuit (right).

Sometimes the parallel equivalent of the imperfect L model is more convenient. If the quality is greater than 5 the conversion is easy:

$$Q = \frac{X_L}{R_S} = \frac{R_P}{X_L} \tag{1}$$

The self resonance frequency occurs when the net impedance is greatest. Applying Kirchoff's current law to the parallel model...

$$|I_{in}| = \frac{|V_{in}|}{\sqrt{(j\omega L + 1/j\omega C)^2 + R_P^2}}$$

$$|Z_L| = \sqrt{R_P^2 - \left(\omega L - \frac{1}{\omega C}\right)^2} \tag{2}$$

One can see that Z_L will reach its peak when:

$$\left(\omega L - \frac{1}{\omega C}\right) = 0$$

Therefore, the maximum impedance of a tank circuit is:

$$|Z_L|_{max} = R_P \qquad \text{when} \qquad f_0 = \frac{1}{2\pi\sqrt{LC}} \tag{3}$$

More generally than non-ideal inductors; the resonant frequency, bandwidth, and quality of a parallel RLC circuit are related to L, C, and R.

$$Q = \frac{\omega_0}{B} = \omega_0 RC = \frac{R}{\omega_0 L} \tag{4}$$

3.2 Common-Base Broadband Amplifier

The basic circuit for an single stage, common-base (CB) amplifier is shown in figure 3. The base terminal is grounded and the input signal passes through the BJT from emitter to collector. In this configuration, the BJT acts like a current buffer, where the input current is repeated at the output regardless of the load.

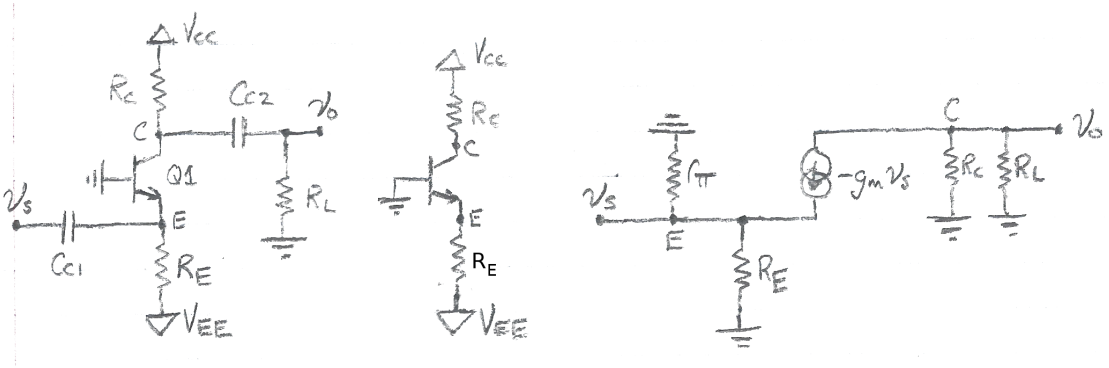

Figure 3: Basic circuit for a common-base broadband amplifier (left), its DC large signal (middle) equivalent, and AC small signal equivalent (right).

Two DC power rails are needed to bias the BJT in forward-active mode. A positive supply holds the collector reverse biased relative to the base which, at ground, is forward biased relative to the negative supplied emitter. Quiescent point analysis of the common-base is easy because the voltage is pinned at every node.

$$I_{EQ} = \frac{-V_{BE(on)} - V_{EE}}{R_E} \tag{5}$$

$$r_\pi = \frac{V_{th}}{I_{BQ}} = \frac{V_{th}(\beta+1)R_E}{-V_{BE(on)} - V_{EE}} \tag{6}$$

$$g_m = \frac{\beta}{r_\pi} = \frac{\alpha(-V_{BE(on)} - V_{EE})}{V_{th}R_E} \tag{7}$$

The hybrid-π model for small signal AC modeling is shown in the right pane of figure 3. Applying Kirchoff's current law at node E can be used to find the input resistance.

$$\text{KCL @ E:} \qquad i_S - \frac{v_s}{r_\pi} - \frac{v_s}{R_E} - g_m v_s = 0$$

$$i_s = v_s \left[\frac{1}{R_\pi} + \frac{1}{R_E} + g_m \right]$$

$$i_s = v_s \left[\frac{R_E + r_\pi + g_m r_\pi R_E}{r_\pi R_E} \right]$$

$$\frac{v_s}{i_s} = \frac{r_\pi R_E}{R_E + r_\pi + g_m r_\pi R_E}$$

$$R_{in} = \frac{r_\pi}{\beta + 1 + \frac{r_\pi}{r_E}} \tag{8}$$

Applying KCL at the collector can be used to calculate the voltage gain of a single common-base stage.

$$-g_m v_s + \frac{v_o}{R_L} + \frac{v_o}{R_C} = 0$$

$$v_o \left[\frac{R_L + R_C}{R_L R_C} \right] = g_m v_s$$

$$A_v = \frac{g_m R_L R_C}{R_L + R_C} \tag{9}$$

3.3 Common-Emitter Broadband Amplifier

The basic circuit for an single stage, common-emitter (CE) amplifier is shown in figure 4. The DC equivalent circuit is shown in the left pane of figure 5; the AC in the right.

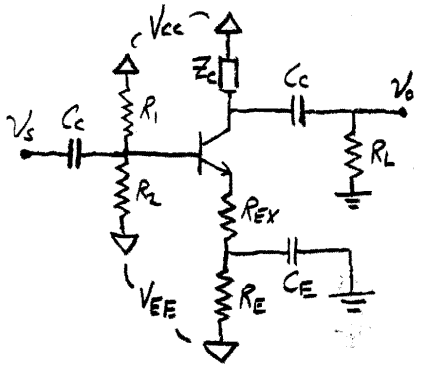

Figure 4: Broadband Common-Emitter Stage

The DC equivalent circuit, shown in figure 5, used a thevenin source conversion from the base bias resistors R_1 and R_2. The thevenin equivalent's parameters are found by

$$R_{TH} = R_1 || R_2 = \frac{R_1 R_2}{R_1 + R_2} \tag{10}$$

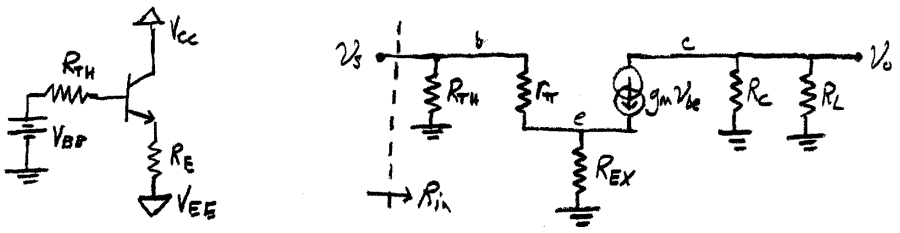

Figure 5: Common-emitter equivalent circuits: DC (left), AC (right).

and

$$V_{BB} = V_{EE} + \frac{R_2}{R_1 + R_2}(V_{CC} - V_{EE}) \tag{11}$$

The same thevenin conversion was used for the AC circuit in figure 5 for R_{TH}. The other parameters in the AC equivalent circuit come from the hybrid-π model:

$$r_\pi = \frac{V_{thermal}}{I_{BQ}} = \frac{V_{th}(\beta + 1)}{I_{EQ}} \tag{12}$$

$$g_m = \frac{\beta}{r_\pi} \tag{13}$$

The DC loading characteristics are easily found by using KVL on the collector-emitter loop.

$$V_{CC} - V_{CE} - R_E I_{EQ} - V_{EE} = 0$$

$$I_E = \frac{V_{CC} - V_{EE}}{R_E} - \frac{V_{CE}}{R_E} \tag{14}$$

The AC characteristics require a little more algebra. We are interested in the small signal voltage gain and input resistance for a CE stage. Kirchoff's current law at the emitter node of the AC equivalent circuit (figure 5, right pane) can be written:

$$\frac{v_e - v_s}{r_\pi} + \frac{v_e}{R_{EX}} + g_m(v_e - v_s) = 0$$

Collecting terms and separating variables gives:

$$v_e \left[\frac{1}{r_\pi} + \frac{1}{R_{EX}} + g_m\right] = v_s \left[\frac{1}{r_\pi} + g_m\right]$$

Multiplying both sides by r_π and R_{EX} gives:

$$v_e[R_{EX}(1 + \beta) + r_\pi] = v_s(1 + \beta)R_{EX}$$

So the ratio between ve and v_s is:

$$\frac{v_e}{v_s} = \left[\frac{(1 + \beta)R_{EX}}{(1 + \beta)R_{EX} + r_\pi}\right]$$

Looking ahead, in the interest of saving paper, it would be better to have an expression for $v_s - v_e$ as a function of v_s.

$$v_s - v_e = v_s \left[1 - \frac{v_e}{v_s}\right] = v_s \left[1 - \frac{(1+\beta)R_{EX}}{(1+\beta)R_{EX} + r_\pi}\right]$$

$$v_s - v_e = \left[\frac{r_\pi}{(1+\beta)R_{EX} + r_\pi}\right] v_s \tag{15}$$

The small signal voltage gain can be found from Ohm's law, applied across the resistors between the output and ground.

$$v_o = (R_C || R_L) * g_m(v_s - v_e)$$

Substituting equation 15 for the voltage difference and then recognizing that $r_\pi g_m = \beta$...

$$v_o = (R_C || R_L) \left[\frac{\beta}{(1+\beta)R_{EX} + r_\pi}\right] v_s$$

Dividing both sides by v_s and pulling α out of the bracket gives us the magnitude of the transfer function in generic form.

$$A_v = \frac{(R_C || R_L)}{R_{EX}} * \frac{\beta}{\beta + 1} * \frac{1}{1 + {r_\pi}/{(\beta+1)R_{EX}}} \tag{16}$$

Now for the small-signal input resistance; the ratio between v_s and i_s in for the AC equivalent circuit in figure 5. Writing KCL at the base node yields

$$-i_s + \frac{v_s}{R_{TH}} + \frac{v_s - v_e}{r_\pi} = 0$$

Substituting equation 15 for v_{s-e} eliminates v_e

$$i_s = \frac{v_s}{R_{TH}} + \frac{v_s}{r_\pi}\left[\frac{r_\pi}{(1+\beta)R_{EX} + r_\pi}\right]$$

Dividing both sides by v_s gives the input conductance, but the partial fractions must be prepared for inversion.

$$G_{in} = \left[\frac{1}{R_{TH}} + \frac{1}{(1+\beta)R_{EX} + r_\pi}\right] = \left[\frac{(1+\beta)R_{EX} + r_\pi + R_{TH}}{R_{TH}(R_{EX}(1+\beta) + r_\pi)}\right]$$

Inverting the conductance and pulling $(1+\beta)R_{EX} + r_\pi$ out of both numerator and denominator gives the input resistance in generic form.

$$R_{in} = R_{TH}\left[\frac{1}{1 + {R_{TH}}/{(1+\beta)R_{EX} + r_\pi}}\right]$$

If one assumes that $R_{TH} >> (1+\beta)R_{EX} + r_\pi$, then the +1 term in the denominator is negligible and the input resistance simplifies to

$$R_{in} = (1+\beta)R_{EX} + r_\pi \tag{17}$$

3.4 Voltage Gain and I_{EQ}

Substituting equation 12 for r_π into equation 16 gives the small-signal gain as a function of the quiescent current.

$$A_v = \frac{(R_C||R_L)}{R_{EX}} * \frac{\beta}{\beta+1} * \frac{1}{1+\frac{V_{th}}{R_{EX}I_{EQ}}} \tag{18}$$

3.5 Coupling Capacitors

The coupling capacitors, labeled C_{Cx}, isolate each stage from direct currents but provide a low impedance path for the AC signal. Taken together, they should form a sharp high-pass filter with its corner frequency below 1000 Hz. The 3dB corner occurs when half the signal power is dissipated in the capacitor and half in the stage's input. This occurs when $Z_{Cc} = Z_{in}$.

$$\frac{1}{|j\omega C|} = R_{in}$$

$$C_C \geq \frac{159.15\,\mu F * \Omega}{R_{in}} \tag{19}$$

4 Design and Simulation

4.1 Specifications

The multi-stage amplifier must meet the following specifications in table 1.

Table 1: Lab Specifications

power supply	$\pm 12V$
passband center frequency	$10MHz$
bandwidth	$300kHz$
input impedance	50Ω
ouptut impedance	50Ω
gain at center frequency	$> 60dB$

4.2 Tank Circuits

Two inductors were wound with ˜22 turns. Their inductance and quality were measured using a Hewlett-Packard 4342A Q Meter. An appropriate discrete capacitor and trimming capacitor were selected for both to obtain a tank circuit with resonance at 10 MHz. The fixed capacitors were soldered to their inductors in parallel.

The soldered LC circuit were breadboarded in parallel with a trimming capacitor and tuned. Then, the breadboarded tank circuit was measured for net capacitance, resonance frequency, and quality using the HP Q Meter. The methods for these measurements are attached in appendix 5.1 and the results are shown in table 2.

Table 2: Tank Circuit Design and Measured Characteristics

Parameter	1	2	Description
L	$4.2\mu H$		measured inductor
Q_L			on HP Q Meter
C_{target}	90		from eq. 3.1
C_{fixed}	$33pF$		nominal value
C_{trim}	$5-35pF$		approx. range
C_d	$55pF$		measured LC circuit
f_0	$13.3MHz$		on HP Q Meter,
Q	85.5		see 5.1
R_p	$30k\Omega$		from eq. 4

4.3 Common-Base Stage

The first stage must be a common-base amplifier in order to achieve low input resistance. The emitter resitance must be chosen to achieve desirable input resistance and voltage gain.

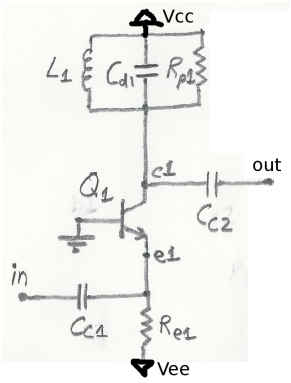

Figure 6: Common-base stage with SPICE netlist labels.

It is clear that R_{in} is strongly related to r_π from equation 8. Substituting equation 6 for r_π into equation 8 yields

$$R_{in} = \frac{-V_{th}R_E}{V_{BE(on)} + V_{EE}} \qquad \text{or} \qquad \left(R_E = \frac{R_{in}(-V_{BE(on)} - V_{EE})}{V_{th}}\right)$$

Using the specified value for V_{EE} and R_{in}, and typical values for V_{th} and $V_{BE(on)}$, the emitter resitance should be

$$R_E = \frac{50\Omega(-0.7V + 12V)}{0.0259V} = 21.8k\Omega$$

With R_E, the quiescent current can be calculated with equation 5; $I_{EQ} = 0.52mA$.

The first BJT was characterized and a DC load line drawn. Because all of the node voltages are pinned, the load line is vertical; V_{CE} is independent of I_{EQ}. It was found that

$$\beta_{Q1} = 176 \qquad V_{AQ1} = 452V$$

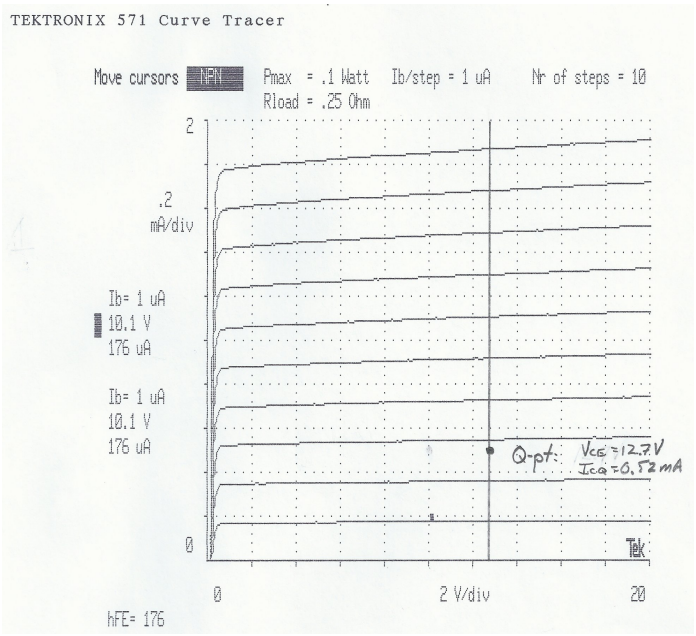

Figure 7: Q1 Current-Voltage Characteristics and DC Load Line

From equation 19 and using $R_{in} = 50\Omega$,

$$C_{C1} \geq 3.183pF$$

At this point, all of the discrete components for the CB stage have been determined. A SPICE simulation was performed to check the performance of the stage. For a load value, the input resistance of the first common emitter stage was used. The netlist used is included in appendix 5.2 and the results are shown in figure 8.

4.4 Common-Emitter Stage

The common-emitter configuration provides the highest overall power gain, compared to CB and CC. This makes it ideal for the middle stages. A single CE stage is shown in figure **??**.

The second BJT was characterized on the Tektronix Curve Tracer using a range of 20V and 2mA (the maximum swing would actually be 24V). The i-v characteristics and the DC load line are shown in figure 9. It was found that

$$\beta_{Q2} = 192 \qquad \text{and} \qquad V_{A(Q2)} = 228V$$

The MATLAB analysis of $A_v(I_{EQ})$ in section 3.4 showed that the gain of a CE amplifier grows proportionally to the quiescent current. Based on this, a relatively large quiescent current was chosen, $1.92mA$.

The Q-point should lie at exactly the middle of the two supplies to allow the maximum possible voltage swing; so $V_{CEQ} = 12V$. Putting the desired Q-pt. into equation 14

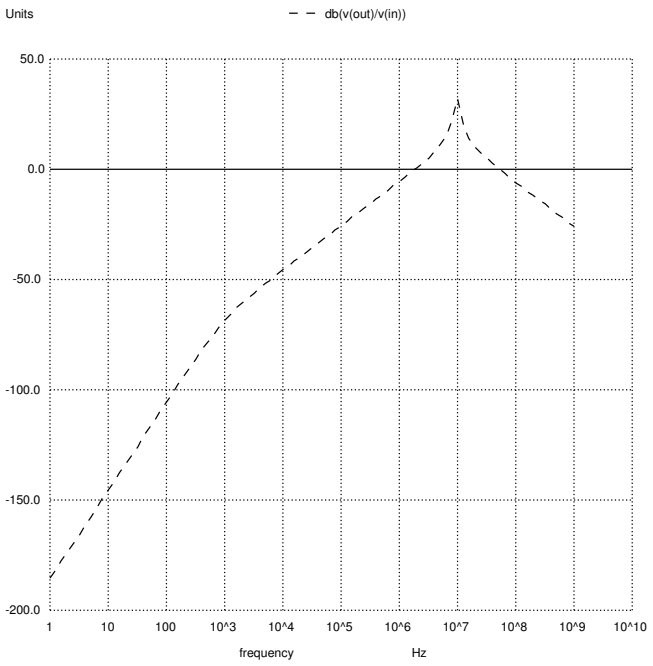

Figure 8: Magnitude Gain of Common-Base Stage, in dB

determined the required emitter resistance.

$$R_{E2} = \frac{V_{CC} - V_{EE} - V_{CEQ}}{I_{EQ}} = \frac{12V}{1.92mA} = 6.25k\Omega$$

The value of R_{TH} should be at least 10 times the emitter resistance to ensure a stiff base bias. [3] Therefore,

$$R_{TH} = 62.5k\Omega = R_1||R_2$$

If V_{CEQ} is 12V, then the base must be biased at +0.7V to forward bias the base-emitter junction. The base resistors form a voltage divider between V_{CC} and V_{EE} to achieve this.

$$0.7V = \frac{R_2}{R_1 + R_2}(24V) - 12V$$

Solving the voltage divider equation with the definintion of R_{TH} gives us values for R_1 and R_2.

$$R_1 = 177.2k\Omega \qquad\qquad R_2 = 96.6k\Omega$$

[3] A stiff base means that R_1 and R_2 behave like a voltage divider, with negligible current being diverted into the base.

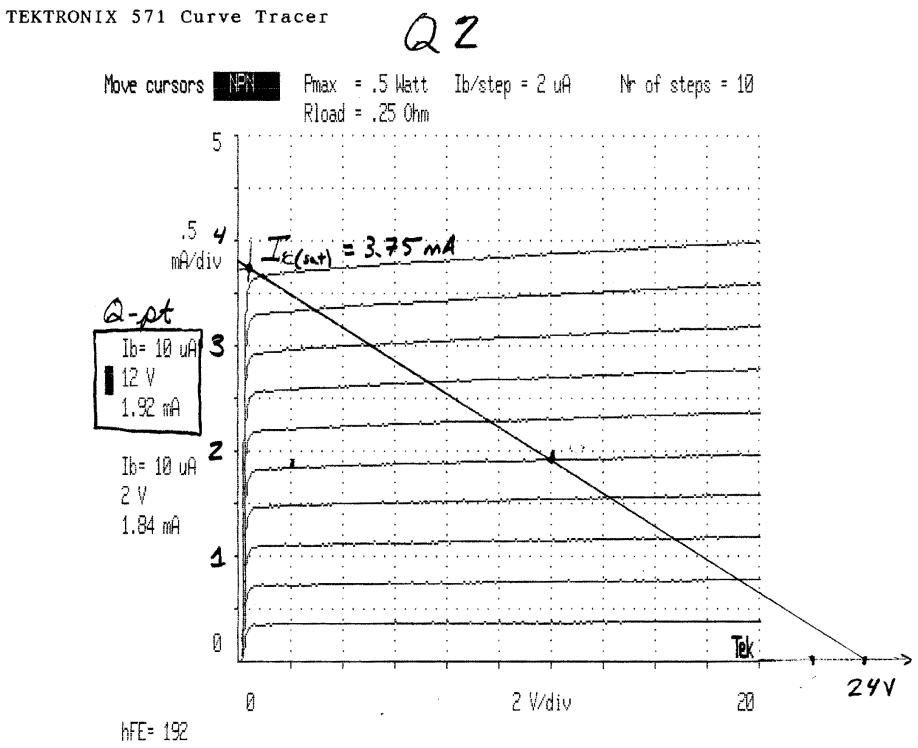

Figure 9: Q2 Current-Voltage Characteristics and DC Load Line

5 Appendices

5.1 HP 4342A Q Meter

The following 3 pages are taken from the HP 4342A Q Meter Operating and Service Manual, pages 35-37.

3-39. Inductance Measurement (at a desired frequency).

3-40. Occasionally it may be necessary to measure inductance at frequencies other than the specific "L" frequencies. The frequency characteristic measurements of an inductor or of an inductor core are representative examples. In such instances, the inductance may be measured as follows:

a. Connect unknown inductor and resonate it using the procedure same as described in Q Measurement (para. 3-34) steps a through e.

b. Note FREQUENCY dial, L/C dial C scale and ΔC dial readings. Substitute these values in the following equation:

$$L = 1/\omega^2 C \approx 0.0253/f^2 C \quad \text{..... (eq. 3-5)}$$

Where, L: inductance value (indicated L) of sample in henries.
f: measurement frequency in hertz.
ω: 2π times the measurement frequency.
C: sum of C and ΔC dial readings in farads.

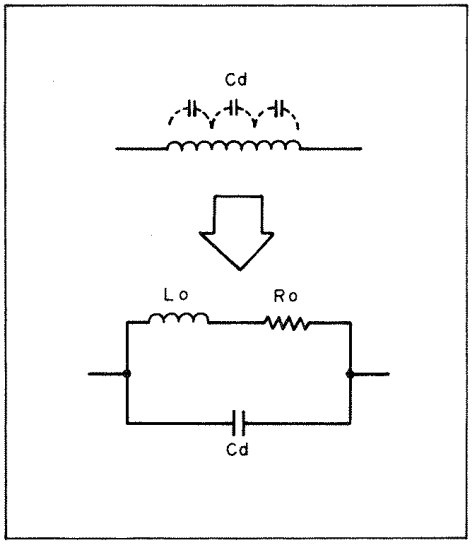

Figure 3-8. Distributed Capacitance Circuit Model.

3-41. MEASUREMENTS REQUIRING CORRECTIONS.

3-42. Effects of Distributed Capacitance.

3-43. The presence of distributed capacitances in a sample influences Q meter indications with a factor that is related to both its capacity and the measurement frequency. Considerations for the distributed capacitances in an inductor may be equivalently expressed as shown in Figure 3-8. In the low frequency region, the impedance of the distributed capacitance Cd is extremely high and has negligible effect on the resonating circuit. Thus, the sample measured has an inductance of Lo, an equivalent series resistance of Ro, and a Q value of ωLo/Ro (where, ω is 2π times the measurement frequency). In the high frequency region, the inductor develops a parallel resonance with the distributed capacitance and the impedance of the sample increases at frequencies near the resonant frequency. Therefore, readings for measured inductances will be higher as the measurement frequency gets closer to the self-resonant frequency. Additionally, at parallel resonance, the equivalent series resistance is substantially increased (this is because, at resonance, the impedance of the sample changes from reactive to resistive because of the phase shift in the measurement current) and the measured Q value reading is lower than that determined by ωLo/Ro. Typical variations of Q and inductance values under these conditions are given in Figure 3-9.

3-44. Ratio of the measurement frequency and the self-resonant frequency can be converted to a distributed capacitance and tuning capacitance relationship with the following equation:

$$f_1/fo = \sqrt{Cd/(C + Cd)} \quad \text{..... (eq. 3-6)}$$

Where, f_1: measurement frequency.
fo: self-resonant frequency of sample.
Cd: distributed capacitance of sample.
C: tuning capacitance of Q meter.

Figure 3-10 graphically shows the variation of measured Q and inductance as capacitance is taken for the parameter. The ideal inductance and Q values in the presence of no distributed capacitance (or when it is negligible) are correlated with the actually measured values by correction factors which correspond to readings along the vertical axis scales in Figures 3-9 and 3-10.

Measurements Requiring Corrections

3-45. Measuring Distributed Capacitance (Preferred Method).

3-46. The impedance of a coil at its self-resonant frequency is resistive and usually high. This characteristic may be utilized for measuring distributed capacitance. Proceed as follows:

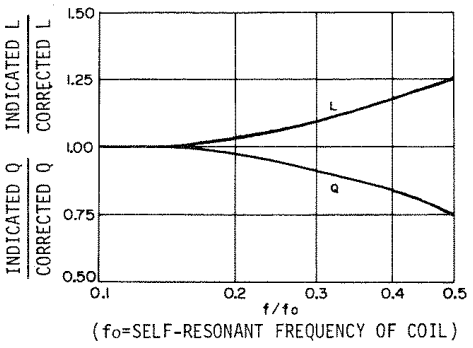

Figure 3-9. Typical Variation of Effective Q and Inductance with Frequency.

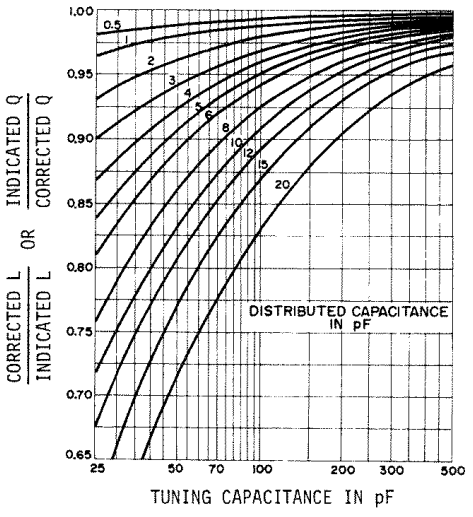

Figure 3-10. Correction Chart for Distributed Capacitance.

a. Connect inductor sample to be tested to the 4342A measurement COIL (HI and LO) terminals.

b. Set L/C dial control to approximately 400pF and ΔC dial control to 0pF. Note C dial reading as C_1.

c. Depress a trial FREQUENCY RANGE button and rotate FREQUENCY dial to search for the frequency at which panel Q meter shows a maximum deflection. If no peak deflection can be observed, change FREQUENCY RANGE setting and repeat the procedure.

d. Adjust FREQUENCY dial control for maximum Q meter deflection. Note the dial frequency reading as f_1.

e. Set measurement frequency to approximately ten times the frequency f_1 noted in step d.

f. Replace the inductor sample with a stable coil (16470 series supplemental inductor) capable of resonating in the measuring circuit at this higher frequency.

g. Adjust the L/C dial control for maximum Q meter deflection.

h. Connect the test inductor to the measurement CAPACITOR (HI and GND) terminals.

i. Adjust the L/C dial control for again obtaining maximum Q meter deflection. If the L/C dial control has to be rotated in the direction of higher capacitance, increase the measurement frequency. If it has to be rotated towards a lower capacitance, decrease the frequency.

j. Alternately connect and disconnect the test inductor to/from the CAPACITOR terminals and adjust the FREQUENCY dial control (if necessary, change FREQUENCY RANGE setting) until the influence of the test inductor to tuning conditions is non-existent (indicated Q value may change). Note dial frequency reading as fo. This frequency is identical with the self resonant frequency of the inductor.

k. Distributed capacitance of the inductor sample is given by the following equation. Substitute measured values of C_1, fo, and f_1 in the equation:

$$Cd = \frac{C_1}{\left(\frac{f_0}{f_1}\right)^2 - 1} \quad \ldots\ldots\ldots\ldots \text{(eq. 3-7)}$$

Where, Cd: distributed capacitance in farads.
C_1: C dial reading (farads) noted in step h.
f_0: measurement frequency (hertz) noted in step j.
f_1: measurement frequency (hertz) noted in step d.

Note

If $f_0 \gg f_1$, the eq. 3-7 is simplified as follows:

$$Cd = \left(\frac{f_1}{f_0}\right)^2 C_1 \quad \ldots\ldots\ldots\ldots \text{(eq. 3-7)}$$

3-47. Measuring Distributed Capacitance (Approximate Method, Cd≥10pF).

3-48. A distributed capacitance more than approximately 10pF may be measured with the simplified procedure described below (this procedure is useful for obtaining approximate values of distributed capacitance with an accuracy which serves practical purposes):

a. Connect inductor sample to the measurement COIL (HI and LO) terminals.

b. Set L/C dial control to approximately 50pF and ΔC dial control to 0pF. Note the C dial reading as C_1.

c. Depress a trial FREQUENCY RANGE button and rotate FREQUENCY dial control to search for the frequency at which panel Q meter shows a maximum deflection. If no peak deflection can be observed, change FREQUENCY RANGE setting and repeat the procedure.

d. Adjust FREQUENCY dial control for maximum panel Q meter deflection. Note this frequency as f_1.

e. Change FREQUENCY dial setting to f_2 equal to f_1/n (n should be a selected integer, e.g. 2 or 3).

f. Adjust L/C dial and ΔC dial controls for again obtaining maximum meter deflection. Note the sum of C dial and ΔC dial readings as C_2.

g. Distributed capacitance is given by the following equation. Substitute measured values of C_1, C_2, f_1 and f_2 in the equation:

$$Cd = \frac{(C_2 - n^2 C_1)}{n^2 - 1} \quad \ldots\ldots\ldots \text{(eq. 3-9)}$$

$$n = \frac{f_1}{f_2}$$

Where, Cd: distributed capacitance in farads.
C_1: C dial reading (farads) noted in step b.
C_2: C dial reading (farads) noted in step f.
f_1: measurement frequency (hertz) noted in step d.
f_2: measurement frequency (hertz) given in step e.

Note

If f_2 is exactly one half of f_1, then

$$Cd = \frac{C_2 - 4C_1}{3} \quad \ldots\ldots\ldots \text{(eq. 3-10)}$$

An average of several measurements using different values of C_1 will improve the results of this measurement. The best accuracy to be expected with this method, however, is in the range of ±2pF.

3-49. CORRECTION FOR Q.

3-50. To use the indicated Q for the purpose of calculating L and Rs (in determining the actual equivalent circuit), it must be corrected for the effects of the distributed capacitance. The corrected Q and the Q value measured by the Q meter can be obtained from the following equation:

$$Qt = Qi \frac{C + Cd}{C} \quad \ldots\ldots\ldots \text{(eq. 3-11)}$$

Then,

$$\text{Correction factor} = \frac{C + Cd}{C} = 1 + \frac{Cd}{C} \quad \ldots\ldots\ldots \text{(eq. 3-12)}$$

Where, Qt: corrected Q value.
Qi: indicated Q value.
C: sum of C and ΔC dial readings.
Cd: distributed capacitance of sample.

5.2 Common-Base SPICE Netlist

The following netlist was used to simulate the CB stage. The labeling in the netlist corresponds to the circuit in figure 6.

```
*** CBstage.cir ***
* Nodes:
* gnd, cc (+12V), ee (-12V), s, in, e1, c1, out

Vcc cc gnd dc 12V ac 0V
Vee ee gnd dc -12V ac 0V
Vs s gnd dc 0V ac 10mV
Rs in s 50
Cc1 in e1 3.183uF
Re1 e1 ee 21.8k
Q1 c1 gnd e1 model1
L1 c1 cc 4.2uH
Cd1 c1 cc 55pF
Rp1 c1 cc 2.18k
Cc2 c1 out 3.183uF
Rld out gnd 9999k

* .model <name> <type> (par1=value1 par2=value2 ...)
* VAF = forward Early voltage
* BF = forward beta; forward common-emitter gain
* CJE = base-emitter zero-bias junction capacitance
* CJC = base-collector zero-bias junction capacitance
* TS = transport saturation current
* NF = forward mode ideality factor

.model model1 npn (BF=176 CJC=20pf CJE=20pf IS=1E-16 VAF=452V NF=1)

.control
set filetype=ascii
ac dec 10 1Hz 1GHz
plot db(v(out)/v(in))
plot ph(v(out))-ph(v(in))
write CBstage.txt db(v(output)/v(input)) ph(v(output))-ph(v(input))
```