

# Multi-Stage Tuned Amplifier

Author: Ben Lorenzetti

Team Member: Francois Nyamsi

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## 1 Objective

To compare the operation of common-emitter and common-base tuned amplifier stages, and to design and characterize a multi-stage, high-gain IF amplifier for 10 MHz operation with  $50\Omega$  input and output impedances.

## 2 Principles of Operation

Tuned amplifiers are critical for electronic communications because they increase the power of desired signal but reject other frequencies as noise. At 10 MHz, a tuned amplifier could be used with an antenna to receive HF amateur radio from the other side of the world <sup>1</sup>, or could be used in a computer to receive 10Base-T ethernet.

There are three possible circuit configurations for bipolar junction transistors (BJT) biased in forward-active mode, based on which terminals are used for input, output, and common reference.

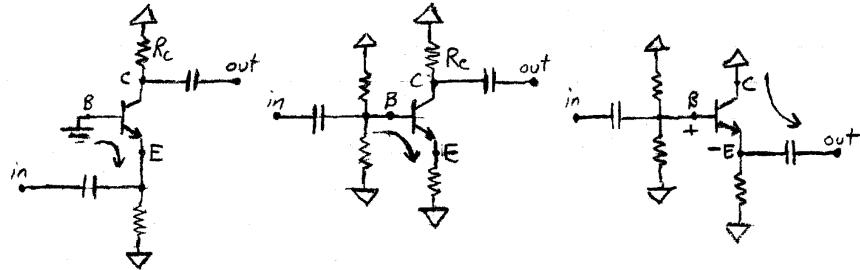


Figure 1: Common-base (left), common-emitter (middle), and common-collector (right) configurations for BJT amplifiers.

Each configuration has its tradeoffs. The common-base (CB) configuration is a good current buffer, with  $A_i \approx 1$  and low input impedance. The common-emitter (CE) configuration offers the best overall power gain, but  $A_v$  and  $A_i$  may vary with loadings. The common-collector configuration is a good voltage buffer ( $A_v \approx 1$ ) with low output impedance.

The three configurations can be cascaded together to gain the benefits of each. If cascaded in the order shown in figure 1, from left-to-right, the resulting 3-stage broadband amplifier would have low input impedance, good power gain, and minimal output impedance.

A slight modification to the CE and CB configurations in figure 1 can apply a filter to the broadband amplifier; tuning the gain to a narrow frequency set by a tank circuit.

Because BJTs are minority carrier devices, they act as current amplifiers without being strongly affected by voltage. For the two configurations where the output is at the collector (CB and CE), the BJT acts like a dependent current source feeding the output load and the biasing resistance  $R_C$ . As a result, the voltage gain for these configurations is determined primarily by how difficult it is for the collector current to reach ground;  $A_v \propto R_C \| R_L$ .

One can take advantage of the collector current's obstinance by replacing  $R_C$  with an impedance that varies with frequency. Using an inductor and a capacitor in parallel provides a short circuit to ground for both DC and high frequency currents. Additionally, at the LC circuit's resonant frequency, the net impedance  $\rightarrow \infty$  due to power oscillating between the two. <sup>2</sup> The result is a narrow bandpass filter at the resonant frequency, where  $Z_C \rightarrow \infty$ .

<sup>1</sup>10 MHz waves can traverse the curve of the earth because they get reflected by charged particles in the ionosphere, called ionospheric skip propagation.

<sup>2</sup>For this reason, an  $L\|C$  circuit is called a tank circuit.

### 3 Theory

#### 3.1 Tank Circuits

No inductor is ideal. The quality of an inductor is defined by the ratio of the impedance and resistance of the discrete element.

$$Q = \frac{X_L}{R_S} \quad \text{where} \quad Z_L = R_S + jX_L$$

The series resistance  $R_S$  is due to the resistivity of the wire and the length used to wrap the coil. Furthermore, the impedance  $X_L$  is not 100% inductive; there is a distributed capacitance  $C_D$  between the surfaces of the tightly wrapped wire. The circuit model for an inductor is shown in the left pane of figure 2.

As a consequence of the distributed capacitance, every inductor will have a self resonant frequency  $f_0$ , at which the energy entering the tank will oscillate between the inductor and capacitor instead of passing through.

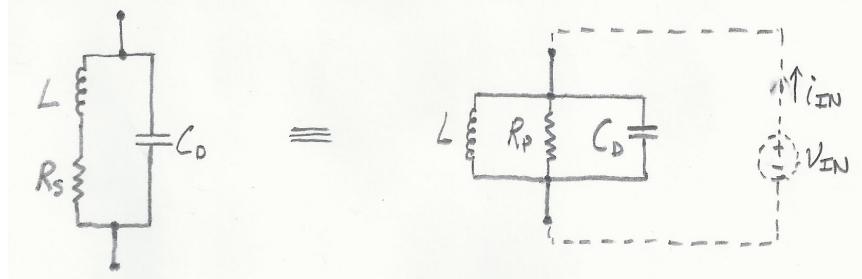


Figure 2: Circuit model for a non-ideal inductor (left) and its parallel equivalent circuit (right).

Sometimes the parallel equivalent of the imperfect L model is more convenient. If the quality is greater than 5 the conversion is easy:

$$Q = \frac{X_L}{R_S} = \frac{R_P}{X_L} \quad (1)$$

The self resonance frequency occurs when the net impedance is greatest. Applying Kirchoff's current law to the parallel model...

$$\begin{aligned} I_{in} &= V_{in} \left[ \frac{1}{R} + \frac{-j}{\omega L} + j\omega C \right] \\ Z_{in} &= \frac{1}{1/R + j(\omega C - 1/\omega L)} \\ |Z_L| &= \frac{R}{\sqrt{1 + R^2(\omega C - 1/\omega L)}} \end{aligned} \quad (2)$$

One can see that  $Z_L$  will reach its peak when:

$$\left( \omega C - \frac{1}{\omega L} \right) = 0$$

Therefore, the maximum impedance of a tank circuit is:

$$|Z_L|_{max} = R_P \quad \text{when} \quad f_0 = \frac{1}{2\pi\sqrt{LC}} \quad (3)$$

More generally than non-ideal inductors; the resonant frequency, bandwidth, and quality of a parallel RLC circuit are related to L, C, and R.

$$Q = \frac{\omega_0}{B} = \omega_0 RC = \frac{R}{\omega_0 L} \quad (4)$$

### 3.2 Common-Base Broadband Amplifier

The basic circuit for a single stage, common-base (CB) amplifier is shown in figure 3. The base terminal is grounded and the input signal passes through the BJT from emitter to collector. In this configuration, the BJT acts like a current buffer, where the input current is repeated at the output regardless of the load.

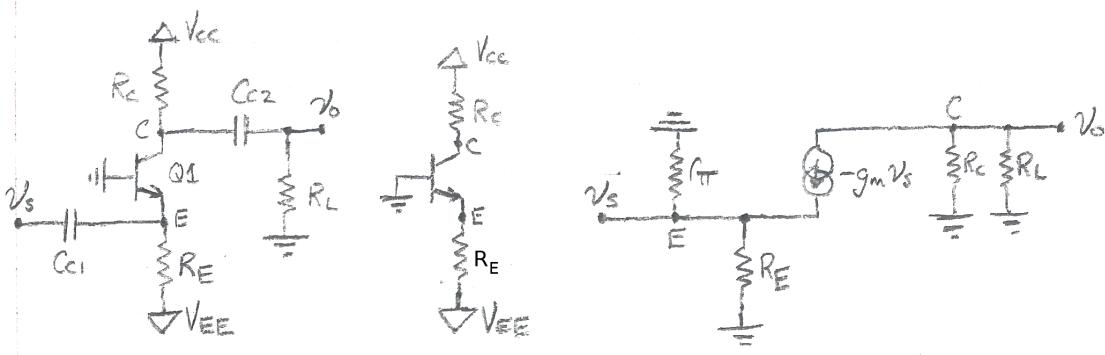


Figure 3: Basic circuit for a common-base broadband amplifier (left), its DC large signal (middle) equivalent, and AC small signal equivalent (right).

Two DC power rails are needed to bias the BJT in forward-active mode. A positive supply holds the collector reverse biased relative to the base which, at ground, is forward biased relative to the negative supplied emitter. Quiescent point analysis of the common-base is easy because the voltage is pinned at every node.

$$I_{EQ} = \frac{-V_{BE(on)} - V_{EE}}{R_E} \quad (5)$$

$$r_\pi = \frac{V_{th}}{I_{BQ}} = \frac{(\beta + 1)V_{th}}{I_{EQ}} \quad (6)$$

$$g_m = \frac{\beta}{r_\pi} = \frac{\alpha I_{EQ}}{V_{th}} \quad (7)$$

The hybrid- $\pi$  model for small signal AC modeling is shown in the right pane of figure 3. Applying Kirchoff's current law at node E can be used to find the input resistance.

$$\text{KCL @ E: } i_S - \frac{v_s}{r_\pi} - \frac{v_s}{R_E} - g_m v_s = 0$$

$$i_s = v_s \left[ \frac{1}{R_\pi} + \frac{1}{R_E} + g_m \right]$$

$$i_s = v_s \left[ \frac{R_E + r_\pi + g_m r_\pi R_E}{r_\pi R_E} \right]$$

$$\begin{aligned}
\frac{v_s}{i_s} &= \frac{r_\pi R_E}{R_E + r_\pi + g_m r_\pi R_E} \\
R_{in} &= \frac{r_\pi}{\beta + 1 + \frac{r_\pi}{r_E}} \\
R_{in} &= \frac{r_\pi}{\beta + 1} \left[ \frac{1}{1 + r_\pi / (\beta + 1) R_E} \right]
\end{aligned} \tag{8}$$

Applying KCL at the collector can be used to calculate the voltage gain of a single common-base stage.

$$\begin{aligned}
\text{KCL @ C: } g_m v_s + \frac{v_o}{R_L} + \frac{v_o}{R_C} &= 0 \\
v_o \left[ \frac{R_L + R_C}{R_L R_C} \right] &= g_m v_s \\
A_v &= \frac{g_m R_L R_C}{R_L + R_C}
\end{aligned} \tag{9}$$

### 3.3 Common-Emitter Broadband Amplifier

The basic circuit for a single stage, common-emitter (CE) amplifier is shown in figure 4. The DC equivalent circuit is shown in the left pane of figure 5; the AC in the right.

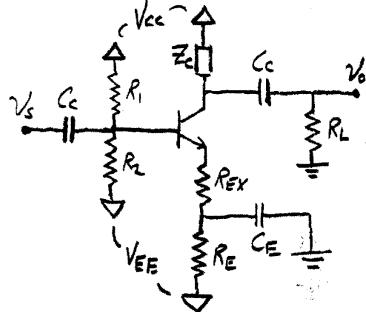


Figure 4: Broadband Common-Emitter Stage

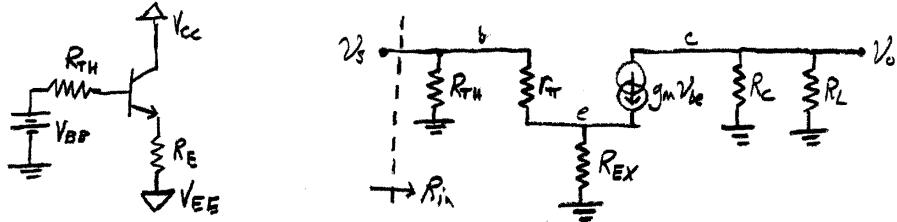


Figure 5: Common-emitter equivalent circuits: DC (left), AC (right).

The DC equivalent circuit, shown in figure 5, used a thevenin source conversion from the base bias resistors  $R_1$  and  $R_2$ . The thevenin equivalent's parameters are found by

$$R_{TH} = R_1 \parallel R_2 = \frac{R_1 R_2}{R_1 + R_2} \tag{10}$$

and

$$V_{BB} = V_{EE} + \frac{R_2}{R_1 + R_2} (V_{CC} - V_{EE}) \quad (11)$$

The same thevenin conversion was used for the AC circuit in figure 5 for  $R_{TH}$ . The other parameters in the AC equivalent circuit come from the hybrid- $\pi$  model, defined previously in equations 6 and 7.

The DC loading characteristics are easily found by using KVL on the collector-emitter loop.

$$V_{CC} - V_{CE} - R_E I_{EQ} - V_{EE} = 0$$

$$I_E = \frac{V_{CC} - V_{EE}}{R_E} - \frac{V_{CE}}{R_E} \quad (12)$$

The AC characteristics require a little more algebra. We are interested in the small signal voltage gain and input resistance for a CE stage. Kirchoff's current law at the emitter node of the AC equivalent circuit (figure 5, right pane) can be written:

$$\frac{v_e - v_s}{r_\pi} + \frac{v_e}{R_{EX}} + g_m(v_e - v_s) = 0$$

Collecting terms and separating variables gives:

$$v_e \left[ \frac{1}{r_\pi} + \frac{1}{R_{EX}} + g_m \right] = v_s \left[ \frac{1}{r_\pi} + g_m \right]$$

Multiplying both sides by  $r_\pi$  and  $R_{EX}$  gives:

$$v_e [R_{EX}(1 + \beta) + r_\pi] = v_s (1 + \beta) R_{EX}$$

So the ratio between  $v_e$  and  $v_s$  is:

$$\frac{v_e}{v_s} = \left[ \frac{(1 + \beta)R_{EX}}{(1 + \beta)R_{EX} + r_\pi} \right]$$

Looking ahead, in the interest of saving paper, it would be better to have an expression for  $v_s - v_e$  as a function of  $v_s$ .

$$\begin{aligned} v_s - v_e &= v_s \left[ 1 - \frac{v_e}{v_s} \right] = v_s \left[ 1 - \frac{(1 + \beta)R_{EX}}{(1 + \beta)R_{EX} + r_\pi} \right] \\ v_s - v_e &= \left[ \frac{r_\pi}{(1 + \beta)R_{EX} + r_\pi} \right] v_s \end{aligned} \quad (13)$$

The small signal voltage gain can be found from Ohm's law, applied across the resistors between the output and ground.

$$v_o = (R_C || R_L) * g_m(v_s - v_e)$$

Substituting equation 13 for the voltage difference and then recognizing that  $r_\pi g_m = \beta \dots$

$$v_o = (R_C || R_L) \left[ \frac{\beta}{(1 + \beta)R_{EX} + r_\pi} \right] v_s$$

Dividing both sides by  $v_s$  and pulling  $\alpha$  out of the bracket gives us the magnitude of the transfer function in generic form.

$$A_{v(CE)} = \frac{(R_C || R_L)}{R_{EX}} * \frac{\beta}{\beta + 1} * \frac{1}{1 + r_\pi / (\beta + 1) R_{EX}} \quad (14)$$

Now for the small-signal input resistance; the ratio between  $v_s$  and  $i_s$  in for the AC equivalent circuit in figure 5. Writing KCL at the base node yields

$$-i_s + \frac{v_s}{R_{TH}} + \frac{v_s - v_e}{r_\pi} = 0$$

Substituting equation 13 for  $v_{s-e}$  eliminates  $v_e$

$$i_s = \frac{v_s}{R_{TH}} + \frac{v_s}{r_\pi} \left[ \frac{r_\pi}{(1+\beta)R_{EX} + r_\pi} \right]$$

Dividing both sides by  $v_s$  gives the input conductance, but the partial fractions must be prepared for inversion.

$$G_{in} = \left[ \frac{1}{R_{TH}} + \frac{1}{(1+\beta)R_{EX} + r_\pi} \right] = \left[ \frac{(1+\beta)R_{EX} + r_\pi + R_{TH}}{R_{TH}(R_{EX}(1+\beta) + r_\pi)} \right]$$

Inverting the conductance and pulling  $(1+\beta)R_{EX} + r_\pi$  out of both numerator and denominator gives the input resistance in generic form.

$$R_{in} = R_{TH} \left[ \frac{1}{1 + \frac{R_{TH}}{(1+\beta)R_{EX} + r_\pi}} \right]$$

If one assumes that  $R_{TH} \gg (1+\beta)R_{EX} + r_\pi$ , then the +1 term in the denominator is negligible and the input resistance simplifies to

$$R_{in(CE)} = (1+\beta)R_{EX} + r_\pi \quad (15)$$

### 3.4 Common-Collector Broadband Amplifier

When the BJT is configured such that the collector is common to both input and output, the amplifier acts like a voltage buffer; providing current gain as necessary and having low output impedance. The common-collector circuit is shown in figure 6. The right pane is the AC equivalent circuit. The DC equivalent circuit is identical to that of the CE amplifier, shown in the left pane of figure 5.

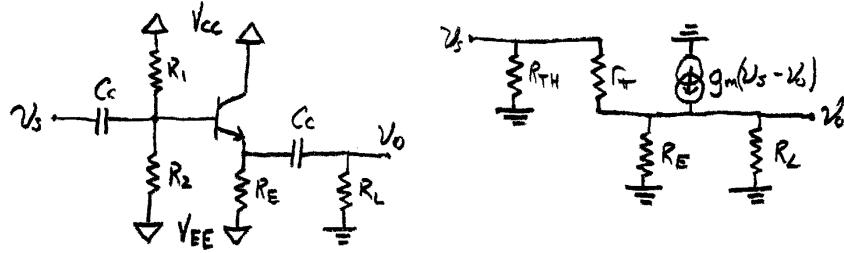


Figure 6: Basic circuit for a common-collector broadband amplifier (left) and its AC equivalent circuit (right).

The small-signal voltage gain should be close to unity, but this can be shown by taking KCL at the emitter node in the AC model in figure 6.

$$\frac{v_o - v_s}{r_\pi} + \frac{v_o}{R_E} + \frac{v_o}{R_L} - g_m(v_s - v_o) = 0$$

Multiplying through by  $r_\pi$  and separating variables cleans this up somewhat,

$$v_o \left[ 1 + \beta + \frac{r_\pi}{R_E} + \frac{r_\pi}{R_L} \right] = v_s [1 + \beta]$$

The coefficients must be prepared for inversion.

$$v_o \left[ \frac{(1 + \beta)R_E R_L + r_\pi(R_E + R_L)}{R_E R_L} \right] = v_s[1 + \beta]$$

So the voltage gain of the common-collector is

$$A_v = \frac{(1 + \beta)R_E R_L}{(1 + \beta)R_E R_L + r_\pi(R_E + R_L)}$$

This can be rewritten in generic transfer form.

$$A_{v(CC)} = \frac{1}{1 + r_\pi/(1+\beta)(R_E||R_L)} \quad (16)$$

The voltage gain is observed to be  $1/2$  when the load resistance is equal to the output impedance. This is the case if the ratio term in the generic form equation is unity. Mathematically, this is expressed as

$$\frac{r_\pi}{(\beta + 1)(R_E||R_o)} = 1$$

Substituting equation 6 in place of  $r_\pi$  and assuming that  $R_E \gg R_o$  yields a surprisingly simple equation for output impedance.

$$R_{o(CC)} = \frac{V_{thermal}}{I_{EQ}} \quad (17)$$

### 3.5 Voltage Gain and $I_{EQ}$

Substituting equation 7 for  $g_m$  into equation 9 gives voltage gain of a CB amplifier as a function of quiescent current. Similaryly, substituting equation 6 for  $r_\pi$  into equation 14 gives the small-signal gain of a CE amplifier.

$$A_{v(CB)} = \frac{\alpha(R_L||R_C)I_{EQ}}{V_{th}} \quad (18)$$

$$A_{v(CE)} = \frac{\alpha(R_C||R_L)}{R_{EX}} \left[ \frac{1}{1 + V_{th}/R_{EX}I_{EQ}} \right] \quad (19)$$

Using typical resistor values, the small-signal gain of broadband common-base and common-emitter amplifiers was plotted as a function of DC biasing. The MATLAB script used to generate plot 7 is included in appendix 7.5.

### 3.6 Tuning a Broadband Amplifier

The broadband amplifier stages described above have a wide bandpass range in the midband. For the CB and CE configurations, the magnitude gain was strongly dependent on the collector and load resistance. If the collector resistance could be modulated based on frequency, then a tuned amplifier could be built.

One way to modulate an impedance element is replacing it with a tank circuit, which are described in section 3.1.

The frequency response of such a tuned amplifier can be modeled by substituting the expression for parallel RLC impedance into the gain equations for CB and CE amplifiers. Equation 2 was substituted into equation 14 and the result was plotted over a range of frequencies in MATLAB. The result of this simulation is shown in figure 8. The MATLAB script is included in appendix 7.6.

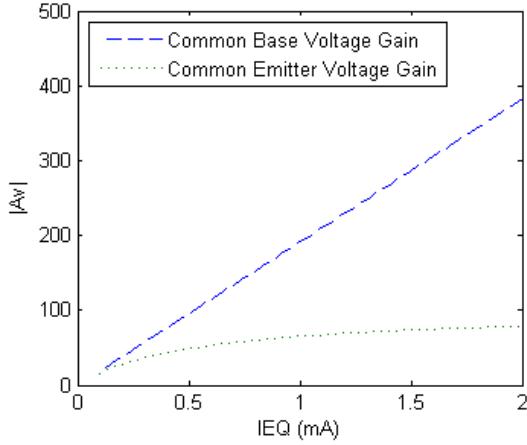


Figure 7: Relationship Between AC Voltage Gain and DC Biasing for CB and CE Amplifier

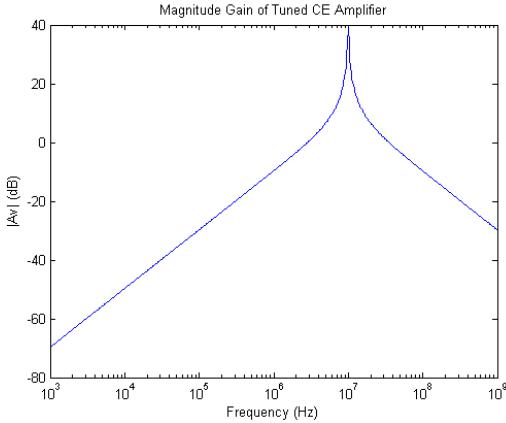


Figure 8: Magnitude Gain of CE Amplifier with 10 MHz Tuned Tank

### 3.7 Coupling Capacitors

The coupling capacitors, labeled  $C_{Cx}$ , isolate each stage from direct currents but provide a low impedance path for the AC signal. Taken together, they should form a sharp high-pass filter with its corner frequency below 1000 Hz. The 3dB corner occurs when half the signal power is dissipated in the capacitor and half in the stage's input. This occurs when  $Z_{Cc} = Z_{in}$ .

$$\frac{1}{|j\omega C|} = R_{in}$$

$$C_C \geq \frac{159.15 \mu F * \Omega}{R_{in}} \quad (20)$$

## 4 Design and Simulation

### 4.1 Specifications

The multi-stage amplifier must meet the following specifications in table 1.

Table 1: Lab Specifications

power supply	$\pm 12V$
passband center frequency	$10MHz$
bandwidth	$300kHz$
input impedance	$50\Omega$
output impedance	$50\Omega$
gain at center frequency	$> 60dB$

## 4.2 BJT Characterization

Four npn 2N2904 BJTs were characterized using the Tektronix curve tracer and an HP LCR meter. The results are shown in table 2. The current amplification factors ( $\beta$  or  $h_{fe}$ ) were taken with DC biasing close to their designed use; the actual  $I_C - V_{CE}$  characteristic curves appear later, as the DC design is described.

Table 2: Measured BJT Characteristics

	Q1	Q2	Q3	Q4
$\beta$	181	191	189	189
$V_A$	260V	273V	273V	224V
$C_{CB}^3$	5.1pF	5.19pF	5.18pF	5.23pF
$C_{BE}$	3.26pF	3.28pF	3.30pF	3.24pF

## 4.3 Tank Circuit Characterization

Two inductors were wound with  $\sim 22$  turns. Their inductance and quality were measured using a Hewlett-Packard 4342A Q Meter. An appropriate discrete capacitor and trimming capacitor were selected for both to obtain a tank circuit with resonance at  $10$  MHz. The fixed capacitors were soldered to their inductors in parallel.

The soldered LC circuit were breadboarded in parallel with a trimming capacitor and tuned. Then, the breadboarded tank circuit was measured for net capacitance, resonance frequency, and quality using the HP Q Meter. The methods for these measurements are attached in appendix 7.1 and the results are shown in table 3.

Table 3: Tank Circuit Design and Measured Characteristics

Parameter	1	2	3	Description
$L$	$3.0\mu H$	$4.2\mu H$	$4.4\mu H$	measured inductor
$Q_L$	250	90	65	on HP Q Meter
$C_{target}$	84.0pF	60.3pF	57.6pF	from eq. 3.1
$C_{fixed}$	55.6pF	33pF	34.1pF	nominal value
$C_{trim}$	27.2pF	31pF	30.1pF	approx
$C_d$	80pF	61.7pF	64.3pF	measured LC circuit
$f_0$	12.8MHz	13.9MHz	13.8MHz	on HP Q Meter,
$Q$	90	110	80	see 7.1
$R_p$	$21.7k\Omega$	$40.3k\Omega$	$30.4k\Omega$	from eq. 4

<sup>3</sup>measurement taken at  $10MHz$

## 4.4 Common-Base Stage I

The first stage must be a common-base amplifier in order to achieve low input resistance. The emitter resistance must be chosen to achieve desirable input resistance and voltage gain.

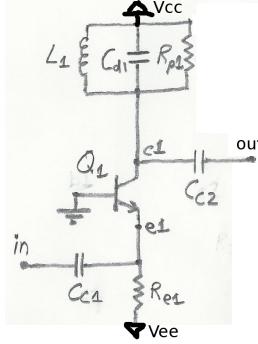


Figure 9: Common-base stage with SPICE netlist labels.

It is clear that  $R_{in}$  is strongly related to  $r_\pi$  from equation 8. If one assumes that  $r_\pi \ll (\beta+1)R_E$ , then the generic form fraction becomes one and the input resistance becomes

$$R_{in}|_{r_\pi/(\beta+1)R_E \rightarrow 0} = \frac{r_\pi}{\beta + 1}$$

The value of  $r_\pi$  varies depending on the quiescent operating point. To achieve an input resistance of  $50\Omega$ , the quiescent current  $I_{EQ}$  must be chosen such that  $r_\pi/\beta + 1$  is 50. Luckily it is easy to design  $I_{EQ}$  for the CB stage; equation 5 shows that it is determined by  $R_E$ . Substituting equations 6 and 5 into the expression for  $R_{in}$  gives

$$R_{in} = \frac{(\beta + 1)V_{th}}{(\beta + 1)I_{EQ}} = \frac{V_{th}}{I_{EQ}} = \frac{V_{th}}{-V_{BE(on)} - V_{EE}} R_E$$

By solving this expression, the designed value for  $R_{E1}$  is

$$R_{E1} = \frac{-0.7V + 12V}{0.0259V} * 50\Omega = 21.814\text{ k}\Omega$$

With  $R_E$ , the quiescent current is known from equation 5;  $I_{EQ} = 0.52mA$ . Armed with this knowledge, the first BJT was characterized and a DC load line drawn. Because all of the node voltages are pinned, the load line is vertical;  $V_{CE}$  is independent of  $I_{EQ}$ .

From equation 20 and using  $R_{in} = 50\Omega$ ,

$$C_{C1} \geq 3.183\text{ pF}$$

At this point, all of the discrete components for the CB stage have been determined. A SPICE simulation was performed to check the performance of the stage. For a load value, the input resistance of the first common emitter stage was used. The netlist used is included in appendix 7.2 and the results are shown in figure 11.

The CB stage was assembled on the breadboard and tested for its frequency response. A load resistor of  $12.5\text{k}\Omega$  was included. The results are shown in figure 11.

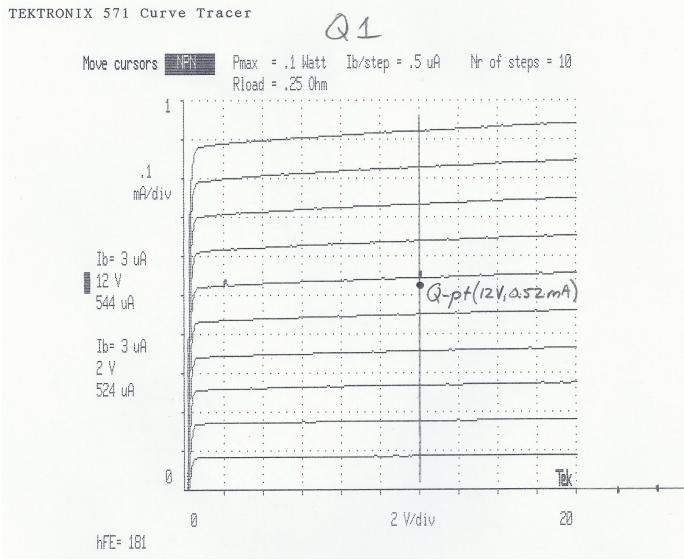


Figure 10: Q1 Current-Voltage Characteristics and DC Load Line

#### 4.5 Common-Emitter Stage II

The common-emitter configuration provides the highest overall power gain, compared to CB and CC. This makes it ideal for the middle stages. A single CE stage is shown in figure 12.

The MATLAB analysis of  $A_v(I_{EQ})$  in section 3.5 showed that the gain of a CE amplifier grows with increasing quiescent current up to a certain point. Based on this,  $I_{EQ}$  was designed to be near 1 mA.

The exact value for  $I_{EQ}$  was chosen based on the closest cursor position to 1 mA when the BJT was characterized on the Tektronix curve tracer. To allow for maximum swing between the  $\pm 12V$  rails,  $V_{EQ}$  was chosen to be 12 V. The I-V characteristics and DC load line are shown in figure 13. The load line was drawn using the chosen Q-pt and a cutoff of 24 V.

Putting the desired Q-pt. into equation 12 determined the required emitter resistance.

$$R_{E2} = \frac{V_{CC} - V_{EE} - V_{CEQ}}{I_{EQ}} = \frac{12V}{1.14mA} = 10.5k\Omega$$

The value of  $R_{TH}$  should be at least 10 times the emitter resistance to ensure a stiff base bias.<sup>4</sup> Therefore,

$$R_{TH} = 105 k\Omega = R_1 \parallel R_2$$

If  $V_{CEQ}$  is 12V, then the base must be biased at +0.7V to forward bias the base-emitter junction. The base resistors form a voltage divider between  $V_{CC}$  and  $V_{EE}$  to achieve this.

$$0.7V = \frac{R_2}{R_1 + R_2}(24V) - 12V$$

Solving the voltage divider equation with the definition of  $R_{TH}$  gives us values for  $R_1$  and  $R_2$ .

$$R_1 = 198.4 k\Omega \quad R_2 = 223.0 k\Omega$$

---

<sup>4</sup>A stiff base means that  $R_1$  and  $R_2$  behave like a voltage divider, with negligible current being diverted into the base.

### Common-Base Stage Frequency Response

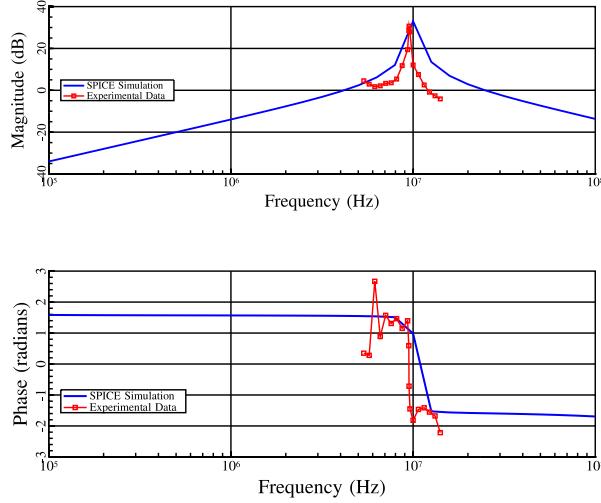


Figure 11: Magnitude Gain of Common-Base Stage, in dB

With DC biasing set, the input resistance of the CE stage is found from equation 15.

$$R_{in2} = (1 + \beta)R_{EX} + r_\pi = (1 + \beta)(R_{EX} + V_{th}/I_{EQ})$$

The partial bypass resistance is arbitrarily chosen to be  $50\Omega$ , based on prior experience and the CE voltage gain (equation 14). Therefore,

$$R_{in2} = 192(50 + 0.0259V/1.14mA) = 14.0\text{ k}\Omega$$

From equation 20 and using  $R_{in2}$ ,

$$C_{C2} \geq 11.4\text{ nF}$$

At this point, all of the discrete components for this CE stage have been determined. A SPICE simulation was performed to check the performance of the stage. The netlist used is included in appendix 7.3 and the results are shown in figure 14.

The CE stage was assembled on the breadboard and tested for its frequency response. The results are superimposed on the graph of the SPICE simulation in figure 14.

## 4.6 Common-Emitter Stage III

Another common-emitter stage was needed to increase the overall voltage gain. The resistor and capacitor values for this stage were designed using the same procedure as section ??.

The I-V characteristics for Q3 are shown in figure 15.

Astonishingly conveniently <sup>5</sup>, the Q-pt curser for Q3 was identical to Q2. Therefore, the discrete resistors and capacitors needed for stage 3 are the same as stage 2.

---

<sup>5</sup>or perhaps astonishingly cleverly

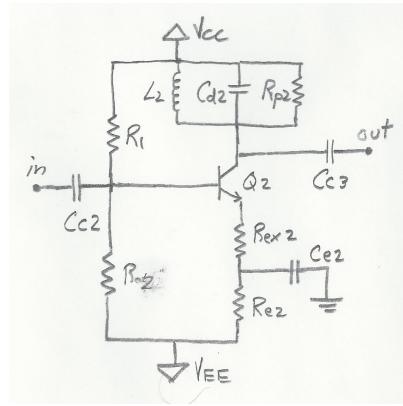


Figure 12: Common-emitter stage with SPICE netlist labels.

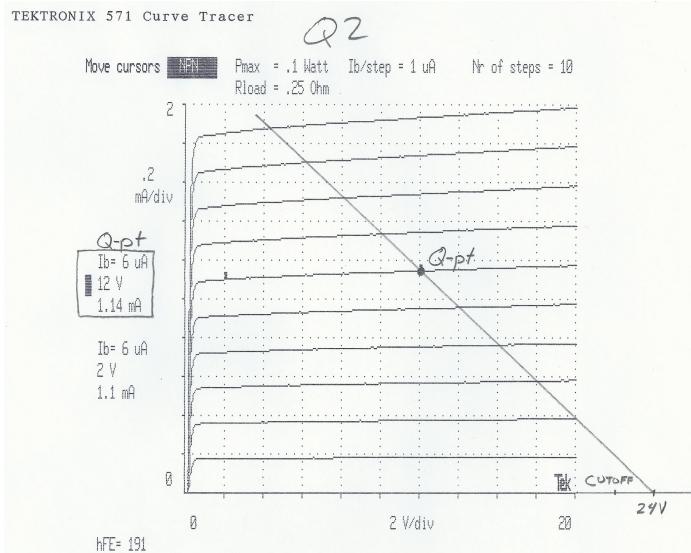


Figure 13: Q2 Current-Voltage Characteristics and DC Load Line

#### 4.7 Common-Collector Stage IV

The Q-pt. of the common-collector stage must be chosen to achieve the specified output impedance of 50 ohms. The relationship between the two was found in equation 17.

$$50 \Omega = R_o = \frac{V_{th}}{I_{EQ}} \quad \rightarrow \quad I_{EQ(Q4)} = 5.2 \text{ mA}$$

The quiescent collector-emitter voltage is chosen to be 12 V to split the power supplies evenly. Ohms law is used to calculate an emitter resistance that will limit  $I_{EQ}$  given a potential difference of 12 V.

$$R_{E4} = \frac{V_{CC} - V_{EE} - V_{CEQ}}{I_{EQ}} = 23.2k \Omega$$

There is not really a point in plotting a load line because the load on the collector is zero. Nevertheless, it has been plotted on the I-V characteristics shown in figure 16.

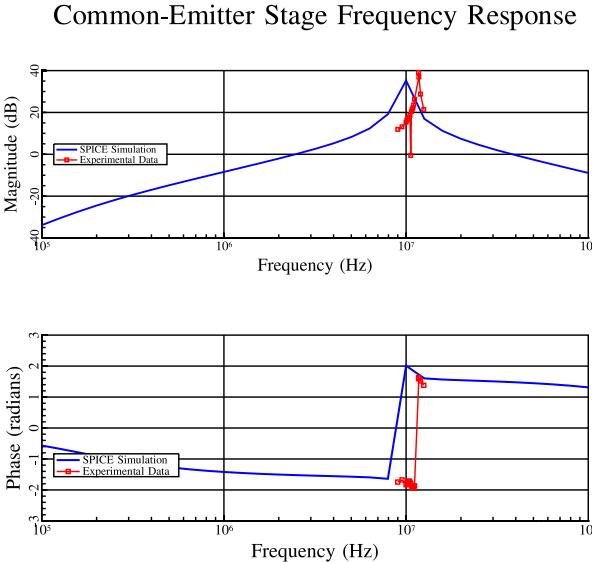


Figure 14: Magnitude Gain of Common-Emitter Stage, in dB

To hold a stiffly biased base at 0.7 V, the thevenin equivalent resistance should be 1/10 the reflected base-emitter resistance.

$$R_{TH} = 0.1(\beta + 1)R_E = 0.1(190)(23.2k) = 440.8 \text{ k}\Omega$$

Solving the thevenin resistance equation and a voltage divider for +0.7 volts simultaneously designates values for  $R_5$  and  $R_6$ .

$$R_5 = 833 \text{ k}\Omega \quad \text{and} \quad R_6 = 936.2 \text{ k}\Omega$$

It is probably safe to copy coupling capacitor values from elsewhere in the circuit. The output coupling should be identical to the input coupling because they are both look out on as little as 50 ohms external impedance.

$$C_{c4} = 11.4 \text{ nF} \quad \text{and} \quad C_{c5} = C_{c1} = 3.18 \mu\text{F}$$

## 4.8 Passive Components Summary Table

In the preceeding sections, the values for biasing resistors and coupling capacitors were designed for the entire circuit. Their actual values are summarized together in table 4.

## 4.9 Building the Amplifier

The four amplifier stages designed above were cascaded together according the circuit shown in figure 17.

Rather than assembling the components together on a breadboard; with noisy jumper antennae and side-by-side strip capacitance, a printed circuit board (PCB) was used.

The PCB was designed using CADSOFT Eagle and was manufactured by OSH Park. It features a top layer with traces corresponding to the circuit diagram in figure 17 (there are no crossing nets in the design), and a bottom layer with power and ground planes. There are vias for a coax cable

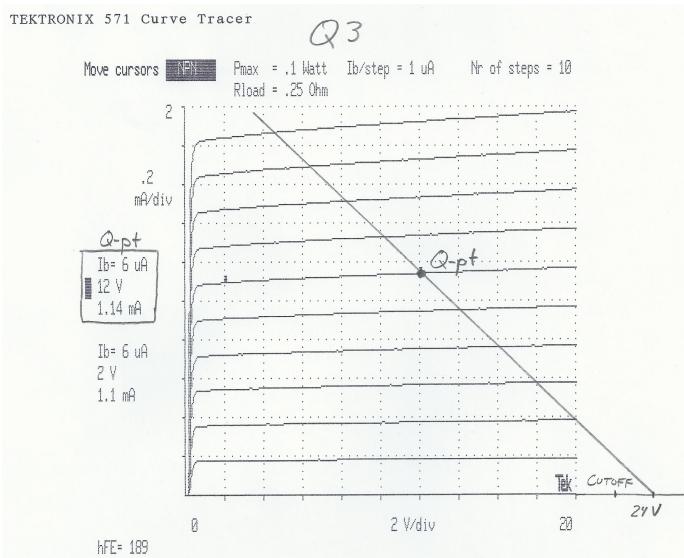


Figure 15: Q3 Current-Voltage Characteristics and DC Load Line

connector for the input signal and banana plug vias for the DC supply and the output signal. The design for the PCB board is included in appendix 7.7.

The super-awesome-but-sadly-difficult-to-modify amplifier is shown in figure 18.

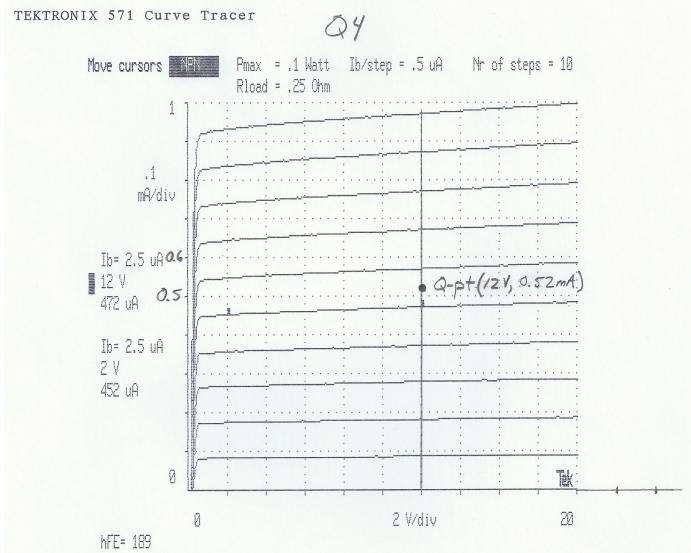


Figure 16: Q4 Current-Voltage Characteristics and DC Load Line

Table 4: Summary of Passive Component Values

Stage	Component	Designed Value	Measured Value
1	$C_{C1}$	$3.18 \mu\text{F}$	$3.19 \mu\text{F}$
	$R_{E1}$	$21.8 \text{ k}\Omega$	$19.2 \text{ k}\Omega$
2	$C_{C2}$	$11.4 \text{ nF}$	$1.7 \text{ nF}$
	$R_1$	$379 \text{ k}\Omega$	$385 \text{ k}\Omega$
	$R_2$	$426 \text{ k}\Omega$	$465 \text{ k}\Omega$
	$R_{EX2}$	$50 \Omega$	$46.5 \Omega$
	$R_{E2}$	$10.5 \text{ k}\Omega$	$9.58 \text{ k}\Omega$
	$C_{E2}$	$25.5 \text{ nF}$	$26.5 \text{ nF}$
3	$C_{C3}$	$11.4 \text{ nF}$	$14.3 \text{ nF}$
	$R_3$	$379 \text{ k}\Omega$	$387 \text{ k}\Omega$
	$R_4$	$426 \text{ k}\Omega$	$483 \text{ k}\Omega$
	$R_{EX3}$	$50 \Omega$	$46.45 \Omega$
	$R_{E3}$	$10.5 \text{ k}\Omega$	$9.75 \text{ k}\Omega$
	$C_{E3}$	$25.5 \text{ nF}$	$25.8 \text{ nF}$
4	$C_{C4}$	$11.4 \text{ nF}$	$14.6 \text{ nF}$
	$R_5$	$833 \text{ k}\Omega$	$823 \text{ k}\Omega$
	$R_6$	$936 \text{ k}\Omega$	$991 \text{ k}\Omega$
	$R_{E4}$	$23.2 \text{ k}\Omega$	$20.8 \text{ k}\Omega$
	$C_{C5}$	$3.18 \mu\text{F}$	$320 \text{ nF}$

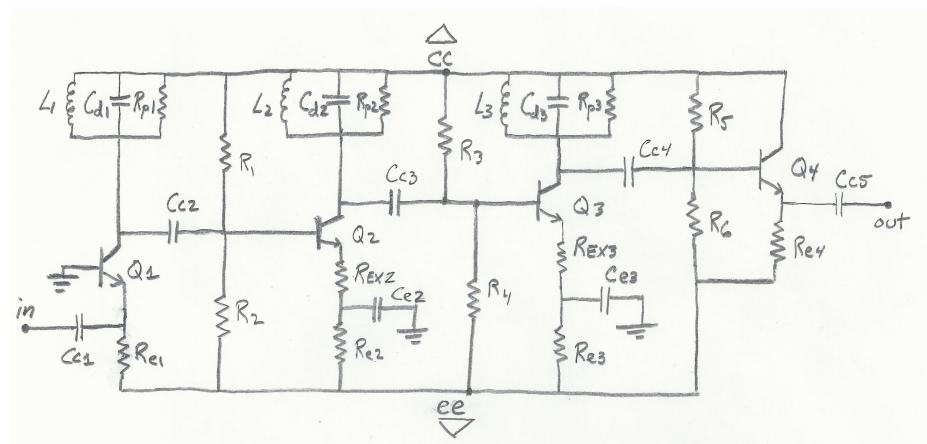


Figure 17: Circuit Layout for the Multi-Stage Amplifier

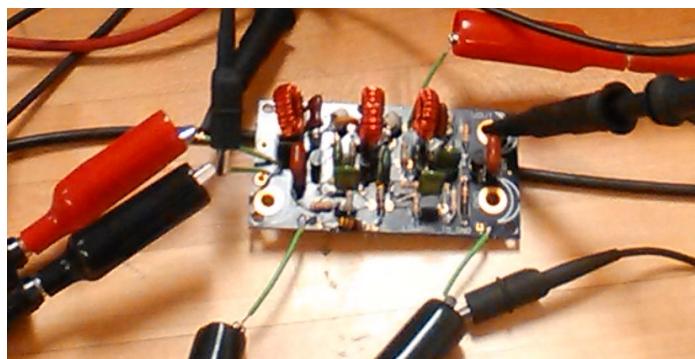


Figure 18: Multi-Stage Tuned Amplifier Assembly

## 5 Test Results

### 5.1 Modifications Made

Although the individual stages worked in isolation on the breadboard, they did not work when cascaded together on the PCB. When the PCB was connected to the DC supply, the output oscillated from  $\pm 11\text{ V}$  at  $23\text{ MHz}$ , regardless of any applied input signal.

Somewhere along the line there must have been resonant feedback, probably through the miller capacitance between the collector and base junctions.

We attempted to add negative feedback to solve this problem. We tried adding a resistive connection between the output of stage 3 and the input of stage 2, but to no avail. We tried winding a second wire on the tank coils to get inductively coupled feedback, but it was just flying in the dark.

Finally in frustration, we removed the capacitor from stage two's tank impedance and the oscillations disappeared.<sup>6</sup> The trimming capacitor was still in place so the net change was decreasing  $C_{d2}$  from  $61.7\text{ pF}$  to  $31\text{ pF}$ .

$$C_{d1} = 61.7\text{ pF} \rightarrow 31\text{ pF}$$

### 5.2 Frequency Response

After the circuit was modified to prevent self oscillation, the amplifier was measured for its frequency response and input impedance. We had difficulty measuring the output impedance. The results of the frequency response measurements are shown in plots 19 and 20.

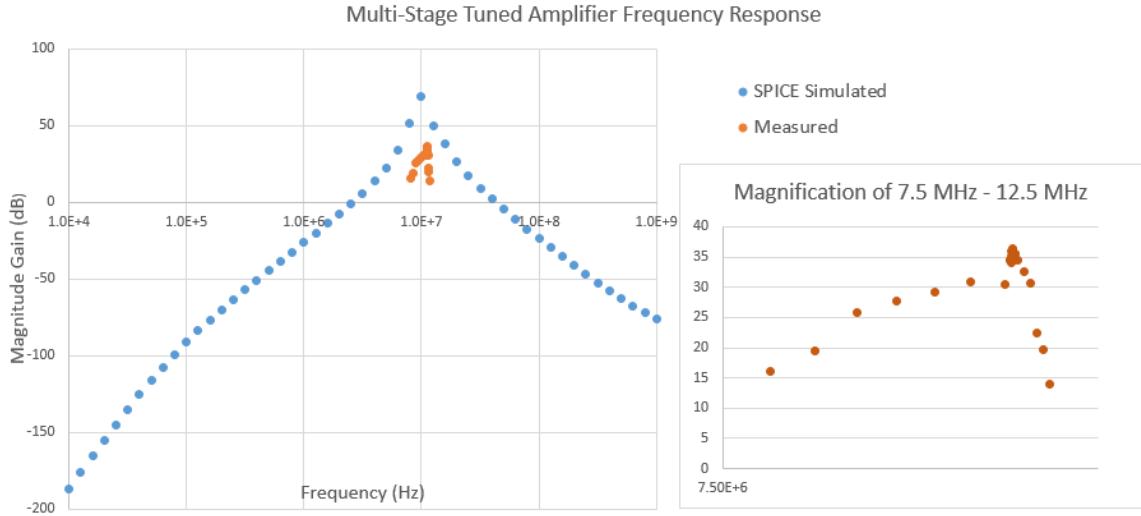


Figure 19: Magnitude Gain of Multi-Stage Tuned Amplifier

For comparison, the frequency response results shown in figures 19 and 20 were plotted against a simulated response from SPICE. The SPICE netlist used to simulate the entire multi-stage circuit is included in appendix 7.4.

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<sup>6</sup>along with most of our gain

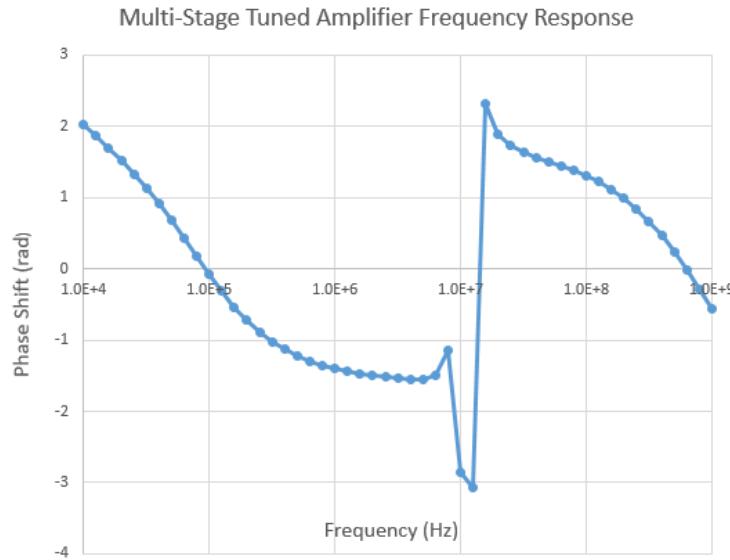


Figure 20: Phase Shift of Multi-Stage Tuned Amplifier

### 5.3 Results Summary Table

The overall characteristics of the multi-stage amplifier are summarized in table 5. Note that the square- bracketed numbers indicate footnotes for additional description.

Table 5: Multi-Stage Tuned Amplifier Results

Parameter	Designed	Simulated	Measured
$R_{in}$	50 $\Omega$	50 $\Omega$	[ <sup>7</sup> ]
$ A_v $	i60 dB	68 dB	36.4 dB
$\angle A_v$	-	$-\pi$	[ <sup>8</sup> ]
$f_0$	10 MHz	10 MHz	11.1 MHz
$B$	300 kHz	[ <sup>9</sup> ]	200 kHz
$R_o$	50 $\Omega$	100 $\Omega$ [ <sup>10</sup> ]	134 $\Omega$

<sup>7</sup>noise interference prevented measurement

<sup>8</sup>oops, forgot to measure this.

<sup>9</sup>there is probably a way to make SPICE tell this...?

<sup>10</sup>I think this was due the lack of non-polar,  $\mu F$  range capacitors for  $C_{C5}$ .

## 6 Conclusions

A cursory glance at the frequency response results in figure 19 tells that the circuit did not function as designed. The magnitude gain falls short by a factor of 20, the center frequency is slightly off, the output resistance is too large, and overall the circuit was very noisy.

I think that the design work that was done was correct; resistors were chosen intelligently based on quiescent point analysis and desired AC parameters, like gain and input resistance. However, the design did not take into account feedback from later stages—which could occur through power supply, the miller effect of the BJT, EMI coupling, and potentially other sources. These effects were not considered in the design, nor accounted for in SPICE (except for the Miller effect). Consequently, we were blindsided by oscillations and noise when physically constructing the circuit.

In the end we had to incapacitate <sup>11</sup>one of our amplifier stages to prevent self-oscillation. This is obviously not acceptable for any real use of a 10 MHz amplifier.

If I were to design this circuit again, I would try to model the feedback using distributed resistance in the power supplies and small line capacitors where signals physically cross. Instead of using capacitors for coupling the various stages, I would use inductive coupling. Inductive coupling provides an advantage in this case because it produces a signal that is  $180^\circ$  out of phase from the input; this can be routed back as negative feedback for each stage.

The two biggest lessons I took away from this lab were: (1) the advantages of the 3 different BJT configurations and (2) The importance accounting for noise and distributed feedback when operating at high frequencies. Unfortunately I am not confident in my theoretical knowledge for this kind of accounting.

## 7 Appendices

### 7.1 HP 4342A Q Meter

The following 3 pages are taken from the HP 4342A Q Meter Operating and Service Manual, pages 35-37.

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<sup>11</sup>literally incapacitate—English though.

3-39. Inductance Measurement (at a desired frequency).

3-40. Occasionally it may be necessary to measure inductance at frequencies other than the specific "L" frequencies. The frequency characteristic measurements of an inductor or of an inductor core are representative examples. In such instances, the inductance may be measured as follows:

- Connect unknown inductor and resonate it using the procedure same as described in Q Measurement (para. 3-34) steps a through e.
- Note FREQUENCY dial, L/C dial C scale and  $\Delta C$  dial readings. Substitute these values in the following equation:

$$L = 1/\omega^2 C \approx 0.0253/f^2 C \dots \text{ (eq. 3-5)}$$

Where, L: inductance value (indicated L) of sample in henries.

f: measurement frequency in hertz.

$\omega$ :  $2\pi$  times the measurement frequency.

C: sum of C and  $\Delta C$  dial readings in farads.

### 3-41. MEASUREMENTS REQUIRING CORRECTIONS.

#### 3-42. Effects of Distributed Capacitance.

3-43. The presence of distributed capacitances in a sample influences Q meter indications with a factor that is related to both its capacity and the measurement frequency. Considerations for the distributed capacitances in an inductor may be equivalently expressed as shown in Figure 3-8. In the low frequency region, the impedance of the distributed capacitance  $C_d$  is extremely high and has negligible effect on the resonating circuit. Thus, the sample measured has an inductance of  $L_0$ , an equivalent series resistance of  $R_0$ , and a Q value of  $\omega L_0/R_0$  (where,  $\omega = 2\pi$  times the measurement frequency). In the high frequency region, the inductor develops a parallel resonance with the distributed capacitance and the impedance of the sample increases at frequencies near the resonant frequency. Therefore, readings for measured inductances will be higher as the measurement frequency gets closer to the self-resonant frequency. Additionally, at parallel resonance, the equivalent series resistance is substantially increased (this is because, at resonance, the impedance of the sample changes from reactive to resistive because of the phase shift in the measurement current) and the measured Q value reading is lower than that determined by  $\omega L_0/R_0$ . Typical variations of Q and inductance values under these conditions are given in Figure 3-9.

3-44. Ratio of the measurement frequency and the self-resonant frequency can be converted to a distributed capacitance and tuning capacitance relationship with the following equation:

$$f_1/f_0 = \sqrt{C_d/(C + C_d)} \dots \text{ (eq. 3-6)}$$

Where,  $f_1$ : measurement frequency.  
 $f_0$ : self-resonant frequency of sample.  
 $C_d$ : distributed capacitance of sample.  
 $C$ : tuning capacitance of Q meter.

Figure 3-10 graphically shows the variation of measured Q and inductance as capacitance is taken for the parameter. The ideal inductance and Q values in the presence of no distributed capacitance (or when it is negligible) are correlated with the actually measured values by correction factors which correspond to readings along the vertical axis scales in Figures 3-9 and 3-10.

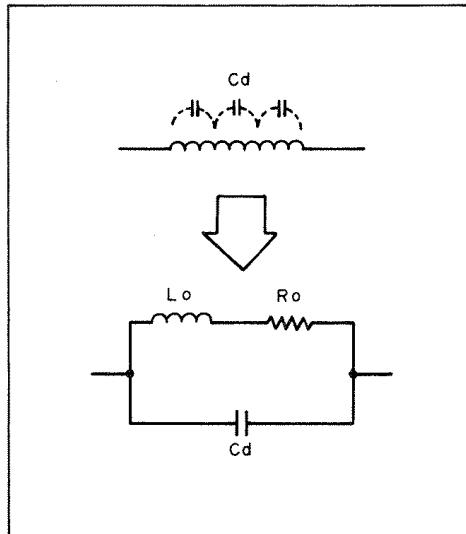


Figure 3-8. Distributed Capacitance Circuit Model.

Measurements Requiring Corrections

3-45. Measuring Distributed Capacitance  
(Preferred Method).

3-46. The impedance of a coil at its self-resonant frequency is resistive and usually high. This characteristic may be utilized for measuring distributed capacitance. Proceed as follows:

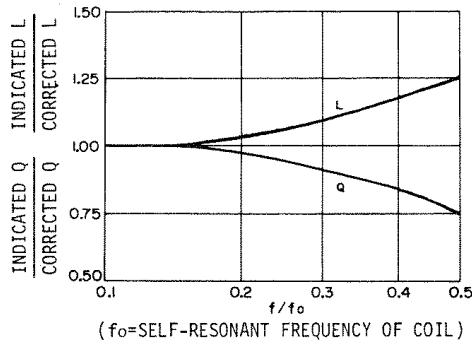


Figure 3-9. Typical Variation of Effective Q and Inductance with Frequency.

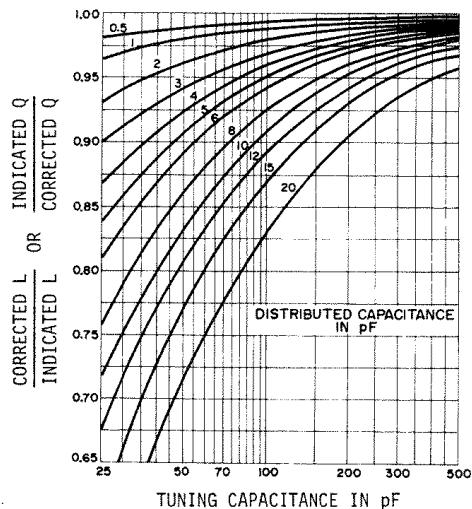


Figure 3-10. Correction Chart for Distributed Capacitance.

- a. Connect inductor sample to be tested to the 4342A measurement COIL (HI and LO) terminals.
- b. Set L/C dial control to approximately 400pF and  $\Delta C$  dial control to 0pF. Note C dial reading as  $C_1$ .
- c. Depress a trial FREQUENCY RANGE button and rotate FREQUENCY dial to search for the frequency at which panel Q meter shows a maximum deflection. If no peak deflection can be observed, change FREQUENCY RANGE setting and repeat the procedure.
- d. Adjust FREQUENCY dial control for maximum Q meter deflection. Note the dial frequency reading as  $f_1$ .
- e. Set measurement frequency to approximately ten times the frequency  $f_1$  noted in step d.
- f. Replace the inductor sample with a stable coil (16470 series supplemental inductor) capable of resonating in the measuring circuit at this higher frequency.
- g. Adjust the L/C dial control for maximum Q meter deflection.
- h. Connect the test inductor to the measurement CAPACITOR (HI and GND) terminals.
- i. Adjust the L/C dial control for again obtaining maximum Q meter deflection. If the L/C dial control has to be rotated in the direction of higher capacitance, increase the measurement frequency. If it has to be rotated towards a lower capacitance, decrease the frequency.
- j. Alternately connect and disconnect the test inductor to/from the CAPACITOR terminals and adjust the FREQUENCY dial control (if necessary, change FREQUENCY RANGE setting) until the influence of the test inductor to tuning conditions is non-existent (indicated Q value may change). Note dial frequency reading as  $f_0$ . This frequency is identical with the self resonant frequency of the inductor.
- k. Distributed capacitance of the inductor sample is given by the following equation. Substitute measured values of  $C_1$ ,  $f_0$ , and  $f_1$  in the equation:

## Measurements Requiring Corrections

$$Cd = \frac{C_1}{\left(\frac{f_0}{f_1}\right)^2 - 1} \quad \text{(eq. 3-7)}$$

Where, Cd: distributed capacitance in farads.  
 C<sub>1</sub>: C dial reading (farads) noted in step b.  
 f<sub>0</sub>: measurement frequency (hertz) noted in step j.  
 f<sub>1</sub>: measurement frequency (hertz) noted in step d.

Note

If  $f_0 \gg f_1$ , the eq. 3-7 is simplified as follows:

$$Cd = \left(\frac{f_1}{f_0}\right)^2 C_1 \quad \text{(eq. 3-7)}$$

### 3-47. Measuring Distributed Capacitance (Approximate Method, Cd ≥ 10pF).

3-48. A distributed capacitance more than approximately 10pF may be measured with the simplified procedure described below (this procedure is useful for obtaining approximate values of distributed capacitance with an accuracy which serves practical purposes):

- a. Connect inductor sample to the measurement COIL (H1 and L1) terminals.
- b. Set L/C dial control to approximately 50pF and AC dial control to 0pF. Note the C dial reading as C<sub>1</sub>.
- c. Depress a trial FREQUENCY RANGE button and rotate FREQUENCY dial control to search for the frequency at which panel Q meter shows a maximum deflection. If no peak deflection can be observed, change FREQUENCY RANGE setting and repeat the procedure.
- d. Adjust FREQUENCY dial control for maximum panel Q meter deflection. Note this frequency as f<sub>1</sub>.
- e. Change FREQUENCY dial setting to f<sub>2</sub> equal to f<sub>1</sub>/n (n should be a selected integer, e.g. 2 or 3).
- f. Adjust L/C dial and AC dial controls for again obtaining maximum meter deflection. Note the sum of C dial and AC dial readings as C<sub>2</sub>.

g. Distributed capacitance is given by the following equation. Substitute measured values of C<sub>1</sub>, C<sub>2</sub>, f<sub>1</sub> and f<sub>2</sub> in the equation:

$$Cd = \frac{(C_2 - n^2 C_1)}{n^2 - 1} \quad \text{(eq. 3-9)}$$

$$n = \frac{f_1}{f_2}$$

Where, Cd: distributed capacitance in farads.

C<sub>1</sub>: C dial reading (farads) noted in step b.

C<sub>2</sub>: C dial reading (farads) noted in step f.

f<sub>1</sub>: measurement frequency (hertz) noted in step d.

f<sub>2</sub>: measurement frequency (hertz) given in step e.

Note

If f<sub>2</sub> is exactly one half of f<sub>1</sub>, then

$$Cd = \frac{C_2 - 4C_1}{3} \quad \text{(eq. 3-10)}$$

An average of several measurements using different values of C<sub>1</sub> will improve the results of this measurement. The best accuracy to be expected with this method, however, is in the range of ±2pF.

### 3-49. CORRECTION FOR Q.

3-50. To use the indicated Q for the purpose of calculating L and R<sub>s</sub> (in determining the actual equivalent circuit), it must be corrected for the effects of the distributed capacitance. The corrected Q and the Q value measured by the Q meter can be obtained from the following equation:

$$Qt = Qi \frac{C + Cd}{C} \quad \text{(eq. 3-11)}$$

Then,

$$\text{Correction factor} = \frac{C + Cd}{C} = 1 + \frac{Cd}{C} \quad \text{(eq. 3-12)}$$

Where, Qt: corrected Q value.

Qi: indicated Q value.

C: sum of C and AC dial readings.

Cd: distributed capacitance of sample.

## 7.2 Common-Base SPICE Netlist

The following netlist was used to simulate the CB stage. The labeling in the netlist corresponds to the circuit in figure 9.

```
*** CBstage.cir ***
* Nodes:
* gnd, cc (+12V), ee (-12V), s, in, e1, c1, out

Vcc cc gnd dc 12V ac 0V
Vee ee gnd dc -12V ac 0V
Vs s gnd dc 0V ac 10mV
Rs in s 50
Cc1 in e1 3.19uF
Re1 e1 ee 19.2k
Q1 c1 gnd e1 model1
L1 c1 cc 3.0uH
Cd1 c1 cc 80pF
Rp1 c1 cc 21.7k
Cc2 c1 out 14.7nF
Rld out gnd 12.25k

* .model <name> <type> (par1=value1 par2=value2 ...)
* VAF = forward Early voltage
* BF = forward beta; forward common-emitter gain
* CJE = base-emitter zero-bias junction capacitance
* CJC = base-collector zero-bias junction capacitance
* TS = transport saturation current
* NF = forward mode ideality factor

.model model1 npn (BF=176 CJC=3.26pf CJE=5.1pf IS=1E-16 VAF=452V NF=1)

.control
set filetype=ascii
ac dec 10 1Hz 1GHz
plot db(v(out)/v(s))
plot ph(v(out))-ph(v(s))
write CBstage.txt db(v(out)/v(s)) ph(v(out))-ph(v(s))
```

### 7.3 Common-Emitter SPICE Netlist

```
*** CEstage.cir ***
* Nodes:
* gnd, cc (+12V), ee (-12V), s, in, b2, e2, e22, c2, out

Vcc cc gnd dc 12V ac 0V
Vee ee gnd dc -12V ac 0V
Vs s gnd dc 0V ac 10mV
Rs in s 50
Cc2 in b2 14.7nF
R1 cc b2 384.7k
R2 b2 ee 465.2k
Q2 c2 b2 e2 model2
Rex e2 e22 46.5
Re2 e22 ee 9.58k
Ce2 e22 gnd 14.7nF
L2 c2 cc 4.2uH
Cd2 c2 cc 61.66pF
Rp2 c2 cc 40.3k
Cc3 c2 out 14.3nF
Rld out gnd 12.5k

* .model <name> <type> (par1=value1 par2=value2 ...)
* VAF = forward Early voltage
* BF = forward beta; forward common-emitter gain
* CJE = base-emitter zero-bias junction capacitance
* CJC = base-collector zero-bias junction capacitance
* TS = transport saturation current
* NF = forward mode ideality factor

.model model2 npn (BF=192 CJC=3.28pf CJE=5.18pf IS=1E-16 VAF=228V NF=1)

.control
set filetype=ascii
ac dec 10 1Hz 1GHz
plot db(v(out)/v(s))
plot ph(v(out))-ph(v(s))
write CEstage.txt db(v(out)/v(s)) ph(v(out))-ph(v(s))
```

## 7.4 Multi-Stage SPICE Netlist

This netlist corresponds to the circuit drawn in figure 17.

```
*** multiStage.cir ***
* Shared nodes: gnd, cc (+12V), ee (-12V), s, in, out
* Stage 1 nodes: e1, c1
* Stage 2 nodes: b2, e2, e22, c2
* Stage 3 nodes: b3, e3, e33, c3
* Stage 4 nodes: b4, e4
*
*POWER SUPPLIES AND SOURCE
Vcc cc gnd dc 12V ac 0V
Vee ee gnd dc -12V ac 0V
Vs s gnd dc 0V ac 10mV
Rs in s 1 ; vary up to ~50 to find Rin
*
*STAGE 1; COMMON BASE
*Cc1 in e1 3.183uF
Cc1 in e1 320nF
Re1 e1 ee 21.8k
Q1 c1 gnd e1 model1
L1 c1 cc 3.0uH
Cd1 c1 cc 80pF
Rp1 c1 cc 21.7k
*
*STAGE 2: COMMON EMITTER
Cc2 c1 b2 11.4nF
R1 cc b2 378.9k
R2 b2 ee 425.8k
Q2 c2 b2 e2 model2
Rex2 e2 e22 50
Re2 e22 ee 10.5k
Ce2 e22 gnd 25.5nF
L2 c2 cc 4.2uH
*Cd2 c2 cc 61.66pF
Cremovefixed c2 cc 31pF
Rp2 c2 cc 40.3k
*
*STAGE 3: COMMON EMITTER
Cc3 c2 b3 11.4nF
R3 cc b3 378.9k
R4 b3 ee 425.8k
Q3 c3 b3 e3 model3
Rex3 e3 e33 50
Re3 e33 ee 10.5k
Ce3 e33 gnd 25.5nF
L3 c3 cc 4.4uH
Cd3 c3 cc 64.33pF
Rp3 c3 cc 30.4k
*
*STAGE 4: COMMON COLLECTOR
```

```

Cc4 c3 b4 13nF
R5 cc b4 833k
R6 b4 ee 936.2k
Q4 cc b4 e4 model4
Re4 e4 ee 23.2k
*
*OUTPUT
Cc5 e4 out 3.18uF
Rload out gnd 100k ; vary down to ~50 to find Rout
*
* .model <name> <type> (par1=value1 par2=value2 ...)
* VAF = forward Early voltage
* BF = forward beta; forward common-emitter gain
* CJE = base-emitter zero-bias junction capacitance
* CJC = base-collector zero-bias junction capacitance
* TS = transport saturation current
* NF = forward mode ideality factor
*
.model model1 npn (BF=181 CJC=5.1pf CJE=3.26pf IS=1E-16 VAF=260V NF=1)
.model model2 npn (BF=191 CJC=5.19pf CJE=3.28pf IS=1E-16 VAF=273V NF=1) ; CJC has large effect on CB
.model model3 npn (BF=189 CJC=5.18pf CJE=3.30pf IS=1E-16 VAF=273V NF=1)
.model model4 npn (BF=189 CJC=5.23pf CJE=3.24pf IS=1E-16 VAF=224V NF=1) ; model2 CJE has effect on CB
*
*OUTPUT CONTROL
.control
.set filetype=ascii
.ac dec 10 10kHz 1GHz
.plot db(v(out)/v(s))
.plot ph(v(out))-ph(v(s))
.write multiStage.txt db(v(out)/v(s)) ph(v(out))-ph(v())

```

## 7.5 MATLAB Script for $A_v(I_{EQ})$

```

clear
% Electronics II Laboratory, Project Two: Multi-stage Tuned Amplifier
% Ben Lorenzetti
% 01/25/2015
%
% Midband Voltage Gain for CB and CE Small Signal, Broadband Amplifiers;
%           As a Function of Q-pt. Emitter Current
%           (small signal broadband--i.e. with purely resistive AC load)
%
% BJT Parameters and Typical Discrete Components
Rc =     10e3;
Rl =     10e3;
Rex =    50;
alpha =  0.99;
Vth =   0.0259;
Req =   (Rc*Rl)/(Rc+Rl);
%
% Calculate Av as a function of IEQ
minIEQ = 0.0001;
maxIEQ = 0.002;
dataPoints = 100;
for i = 1 : dataPoints + 1
    IEQ(i) = minIEQ + ((maxIEQ-minIEQ)/dataPoints) * (i-1);
    CBgain(i) = (alpha*Req*IEQ(i)) / Vth;
    CGain(i) = ((Req/Rex)*alpha) / (1+Vth/(Rex*IEQ(i)));
end
%
% Plot Results
figure
plot((IEQ*1000), CBgain, '--', (IEQ*1000), CGain, ':');
xlabel('IEQ (mA)');
ylabel('|Av|');
legend('Common Base Voltage Gain', 'Common Emitter Voltage Gain', 'Location', 'Northwest');
axis([0,2,0,500]);
%

```

## 7.6 MATLAB Script for $A_{v(CE)}(f)$

```
clear
% Electronics II Laboratory, Project Two: Multi-stage Tuned Amplifier
% Ben Lorenzetti
% 01/25/2015
%
% High Frequency Voltage Gain for Tuned Common-Emitter Amplifiers;
%
% BJT Parameters and Typical Discrete Components
Rp = 30e3;
Cp = 63.6e-12;
Lp = 4e-6;
Rl = 10e3;
Rex = 50;
alpha = 0.99;
Vth = 0.0259;
Ieq = 1e-3;
%
% Calculate Av as a function of frequency
minFreq = 1e3;
maxFreq = 1e9;
pointsPerDecade = 100;
dataPoints = pointsPerDecade*log10(maxFreq/minFreq);
logBase = 10^(1/pointsPerDecade);
for i = 1 : dataPoints + 1
    freq(i) = minFreq * logBase^(i-1);
    omega(i) = 2*pi*freq(i);
    Bc(i) = omega(i)*Cp - 1/(omega(i)*Lp); % susceptanceB = 1/reactanceX
    Zc(i) = Rp/sqrt(1 + Rp^2*Bc(i)^2);
    Av(i) = (alpha/Rex)*((Zc(i)*Rl)/(Zc(i)+Rl))*(1+Vth/(Rex*Ieq))^-1;
    dB(i) = 20*log10(Av(i));
end
%
% Plot Results
figure
semilogx(freq, dB);
xlabel('Frequency (Hz)');
ylabel('|Av| (dB)');
title('Magnitude Gain of Tuned CE Amplifier');
%
```

## 7.7 PCB Board Design

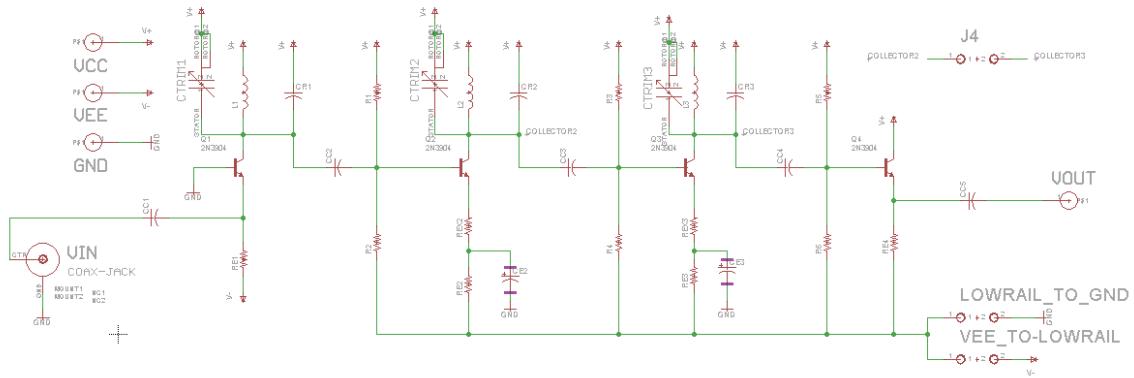


Figure 21: Eagle CAD Circuit Diagram

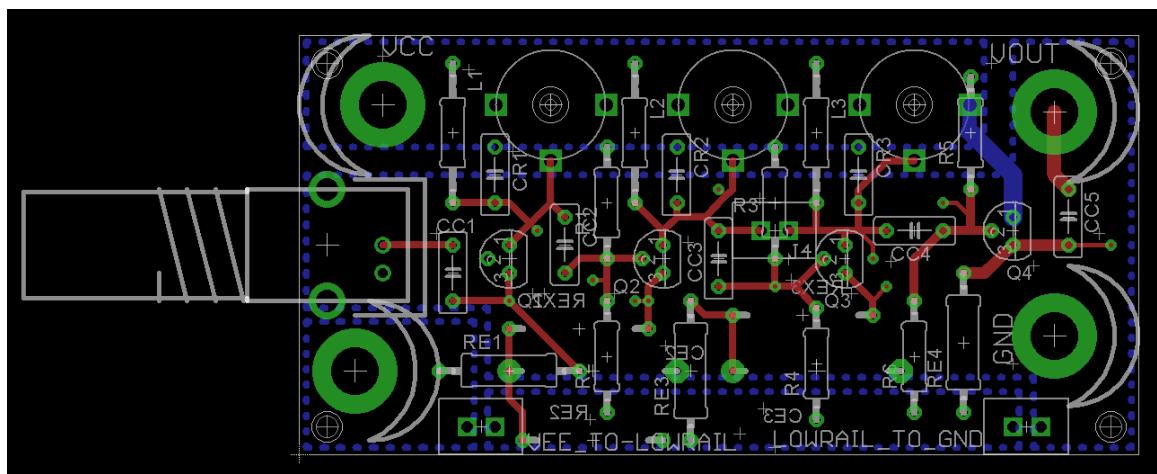


Figure 22: Eagle CAD Physical Board