Emitter-Coupled Oscillator

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Contents

1 Objective

To investigate the design and operation of an emitter-coupled astable multivibrator for 50 MHz operation.

2 Principles of Operation

In analog electronics, a sinusoidal oscillator is sometimes needed, such as for power conversion, driving a motor, or for the carrier frequency in radio transmissions. These can be built from an amplifier with a passive feedback network, where the gain > 1 and the feedback is positive at the frequency of operation [1]. The only other requirement is that the amplifer operates linearly.

In contrast, digital circuits usually require a square wave clock signal. Ironically, a digital oscillator can be built starting from a basic digital component.

A latch is a digital circuit with two stable states, made from two cross-connected amplifiers. It is a fundamental component in digital logic. In fact, when a master and slave latch are connected in series they form a 1-bit, flip-flop register used in CPUs. Usually, the cross-connection between the two amplifiers is resistive and one amplifier will be driven in saturation while the other is in cutoff. Amplifier in digital circuits are usually driven between saturation and cutoff, making them unlinear, binary (two-state) devices.

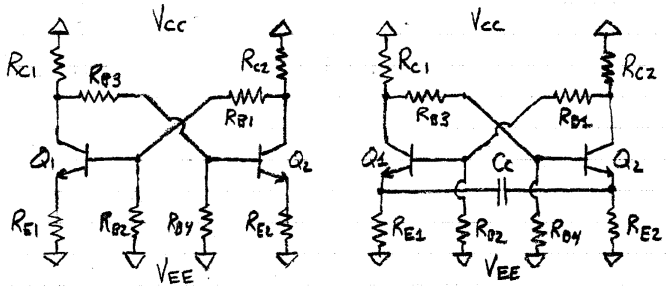

Figure 1: Digial Latch (left) and Latch with Reactive Emitter Coupling (right).

If the cross-connection is made to be reactive, then the latch may not be stable in either state. If it oscillates between the two states and produces a near-square wave, it is called a bistable multivibrator. A capacitor is usually used for the cross-connection because it delays the instantaneous voltage change that would normally occur when a transistor switches between saturation and cutoff.

Analog oscillators produce sinusoids; digital oscillators produce square waves. An analog amplifer oscillates if it has reactive feedback that is positive; a digital flip-flop oscillates if it has reactive cross-connection strong enough to switch states. Analog oscillators use an amplifier in a linear range; digital oscillators use drive amplifier to its two limits. An analog oscillator may form unintentionally through parasitic feedback, such as through the Miller capacitance of a BJT. A digital osciallator may form unintentionally through propagation delay or carry-through logic All of these comparisons between analog and digital oscillators can probably be gleaned from the block-level diagrams in figure 2.

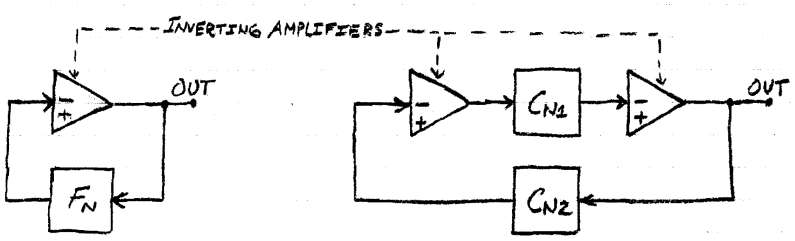

Figure 2: An Analog Feedback Oscillator (left) Compared to Bistable Multivibrator (right)

[1] the Barkhausen Criterion

3 Theory

3.1 Bistable Latch

A digital latch can be built with two cross-connected BJT amplifiers, shown in figure 3. The amplifiers should be nearly mirror images of one another and the coupling networks should be entirely resistive.

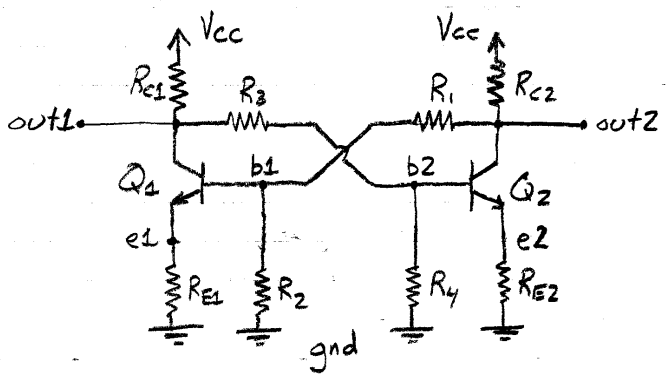

Figure 3: BJT Implementation of a Digital Latch

The latch is bistable, meaning it has two self-sustaining states. Either Q1 is saturated while Q2 is cutoff, or Q1 is cutoff while Q2 is saturated. The circuit is a symmetric loop, so it is not clear where to begin any analysis. Instead of starting at a particular node and time, we will start with some sanity assumptions and determining the conditions that make them true.

If the transistors operate digitally–i.e. either in saturation or cutoff–then the output can have two possible values, the difference between which will be called V_{pkpk}. This difference is set by R_C and the saturation current.

$$R_C = \frac{V_{pkpk}}{I_{C(sat)}} \tag{1}$$

Of course, this assumes that the current through R_1 and R_2 is negligible compared to $I_{C(sat)}$.

$$I_{Bias} << I_{C(sat)}$$

Another design assumption is the stiff base bias. In order to stiffly bias the transistors, the base currents should draw negligible current relative to R_1 and R_2.

$$I_{B(sat)} << I_{Bias}$$

These two biasing network equations compete with each other because the base and collector currents are related by β. The best way to satisfy both is

$$I_{Bias} = \frac{I_{C(sat)}}{\sqrt{\beta}} \tag{2}$$

If the supply voltage is relatively large compared to the output amplitude, then I_{Bias} varies little with binary state and is set by R_1 and R_2.

$$I_{Bias} = \frac{V_{CC}}{R_1 + R_2} \tag{3}$$

Combining equations 2 and 3 helps in designing the bias network.

$$R_1 + R_2 = \frac{\sqrt{\beta} V_{CC}}{I_{C(sat)}} \tag{4}$$

The analysis so far has assumed that the saturation current is fixed, but should it be fixed with R_C or R_E? It makes more sense to limit $I_{C(sat)}$ with R_C because later we will be adding a reactive element to the emitters.

For the transistor to be driven to saturation, V_{CE} is approximately equal to $V_{BE(on)}$ and the collector is equipotential with the base. The collector potential during saturation is the lesser of the two binary outputs, so

$$V_{B(sat)} = V_{CC} - V_{pkpk} \tag{5}$$

For the other transistor to be cutoff, the base-emitter junction must not have achieved the forward bias potential.

$$V_{B(off)} < V_{E(off)} - V_{BE(on)} \tag{6}$$

The transistors are cross-connected from their outputs to the opposite bases, so the base bias is dependent on the opposite transistor's state. The bias networks are voltage dividers and the output has two states, so the base potential is one of the two following values.

$$V_B = \begin{cases} \frac{R_2}{R_1+R_2} V_{CC} & : \text{saturation transistor} \\ \frac{R_2}{R_1+R_2}(V_{CC} - V_{pkpk}) & : \text{cutoff transistor} \end{cases} \tag{7}$$

Combining the required conditions for saturation and cutoff from equations 5 and 6 with the two biasing potentials gives the conditions for stability of the latch.

$$\begin{cases} \frac{R_2}{R_1+R_2} V_{CC} = V_{CC} - V_{pkpk} & : \text{saturation stability} \\ \frac{R_2}{R_1+R_2}(V_{CC} - V_{pk-pk}) < V_{E(off)} + V_{BE(on)} & : \text{cutoff stability} \end{cases}$$

A latch is only useful if the output is self-sustaining, so these two conditions must both be met. The first condition has all fixed values, so the ratio R_2/R_1+R_2 must be chosen there. The second condition can then be rearranged to separate fixed values from as-yet-undetermined values.

$$\begin{cases} \frac{R_2}{R_1+R_2} = \frac{V_{CC}-V_{pkpk}}{V_{CC}} & : \text{saturation stability} \\ V_{E(off)} > \frac{R_2}{R_1+R_2}(V_{CC} - V_{pkpk}) - V_{BE(on)} & : \text{cutoff stability} \end{cases} \tag{8}$$

The stability conditions for both transistors would have to be followed if we were designing digital memory. However, for an oscillator we only want quasi-stable states; in the next section we will violate the stability by adding reative coupling to affect V_E of the off transistor.

3.2 Astable Multivibrator

The simple circuit for an astable multivibrator is shown in figure 4. Topologically it is easy to make–just add a capactitor to a BJT latch.

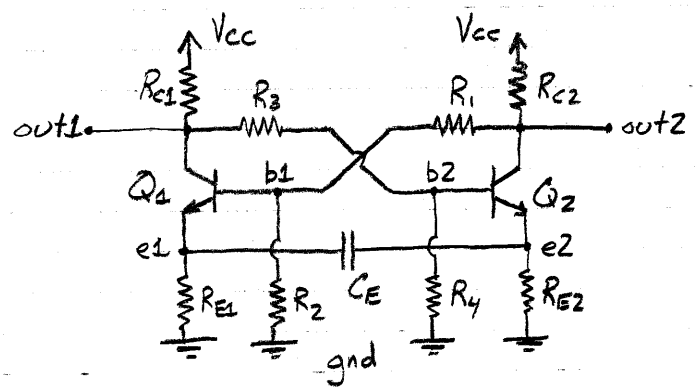

Figure 4: Simple Version of Astable Multivibrator

The top half of the circuit is the same as the latch. The relationships between $I_{C(sat)}$ and V_{pkpk} to R_C, R_1, and R_2 is the same as in equations 1 through 8. Now for the bottom half.

The emitter potential for the saturation transistor is set by the top half because it follow the base. Taking the saturation base voltage from equation 7...

$$V_{E(sat)} = \frac{R_2}{R_1 + R_2} V_{CC} - V_{BE(on)} \tag{9}$$

In a perfect world, this emitter voltage would hold regardless of R_E.[2] However, in the interest of not burning up the base-emitter junction, R_E should probably be just short of becoming the saturation current limiter.

$$R_E = \frac{V_{E(sat)}}{I_{E(sat)}} = \frac{\frac{R_2}{R_1+R_2} V_{CC} - V_{BE(on)}}{I_{C(sat)}} \tag{10}$$

Equation 8 described the stability conditions for the latch. To make an oscillator, the circuit should be quasistable–i.e. it should be stable for some specific length of time. After a period of stable output, an internal trigger cause a change of state. For the emitter-coupled oscillator, the trigger is the emitter potential of the cutoff transistor falling below $V_{E(off)}$. From equation 8, the cutoff state is stable while

$$V_{E(off)} > \frac{R_2}{R_1 + R_2}(V_{CC} - V_{pkpk}) - V_{BE(on)}$$

The capacitor prevents instantaneous voltage changes, so it takes some time for V_E to fall below this trigger threshold. We expect an RC time constant for the discharge to be on order of $\tau = R_E C_E$, but solving for the transient equation may give additional insights.

$$i(t) = C\frac{dv(t)}{dt} \qquad \text{resists instantaneous } \delta V$$

The cross-connected bases make the transistors behave somewhat like a emitter-follower voltage source. If we assume that switching times for the transistors is negligible, then the transient circuit

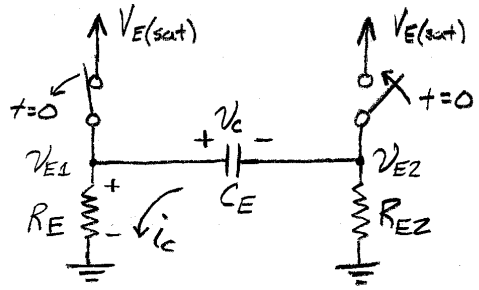

Figure 5: Transient Circuit for Simple Emitter-Coupled Oscillator

is as shown in figure 5. This assumption is true if the base-emitter capacitance is negligible, and so is the delay in the BJT due to the rate of minority carrier diffusion.

At t=0, Q_2 triggers itself on by v_{E2} falling below the threshold. In turn, this forces Q_1 off through the cross connection. This trigger occurs when $v_{E2(off)}$ breaks the stability condition.

$$V_{E(trig)} = \frac{R_2}{R_1 + R_2}(V_{CC} - V_{pkpk}) - V_{BE(on)} \tag{11}$$

Immediately before the trigger occurs, the voltage at E1 is $V_{E(sat)}$ and the voltage at E2 is the trigger voltage $V_{E(trig)}$. So, the initial voltage across the capacitor is

$$v_C(0^-) = V_{E(sat)} - V_{E(trig)} \tag{12}$$

With the initial conditions in hand, we are ready to analyze the transient circuit. After switching, R_{E2} does not matter because Q_2 acts like a voltage source. Consequently there is only one loop to analyze: the v_{E1} discharge loop. The differential equation describing the loop is found from Kirchoff's Voltage Law.

$$v_{E1}(t) := \quad R_E i_C(t) = V_{E(sat)}u(t) + v_C(t) \tag{13}$$

$$R_E\left(-C_E\frac{dv_C(t)}{dt}\right) = V_{E(sat)}u(t) + v_C(t)$$

$$\frac{d}{dt}v_C(t) + \frac{1}{R_E C_E}v_C(t) = \frac{-V_{E(sat)}}{R_E C_E}u(t) \tag{14}$$

The system will be easier to solve in frequency domain. Taking the Laplace transform gives

$$sV_C(s) - v_C(0^-) + \frac{1}{R_E C_E}V_C(s) = \frac{-V_{E(sat)}}{sR_E C_E}$$

$$V_C(s)\left[s^2 + \frac{s}{R_E C_E}\right] = sv_C(0^-) - \frac{V_{E(sat)}}{R_E C_E}$$

$$V_C(s) = \frac{sv_C(0^-) - \frac{V_{E(sat)}}{R_E C_E}}{s(s + \frac{1}{R_E C_E})}$$

$$V_C(s) = [V_{E(sat)} - V_{E(trig)}]\left[\frac{s - \frac{V_{E(sat)}}{R_E C_E(V_{E(sat)} - V_{E(trig)})}}{s(s + \frac{1}{R_E C_E})}\right]$$

[2]Actually in a perfect world, I would have already graduated.

$$V_C(s) = C\frac{s - f_1}{s(s + f_0)} \quad \text{where} \begin{cases} C = V_{E(sat)} - V_{E(trig)} \\ f_0 = \frac{1}{R_E C_E} \\ f_1 = f_0 \frac{V_{E(sat)}}{C} \end{cases} \tag{15}$$

Before converting back to time domain, a partial fraction expansion must be done.

$$\frac{s - f_1}{s(s + f_0)} = \frac{A}{s} + \frac{B}{s + f_0} = \frac{A(s + f_0) + Bs}{s(s + f_0)}$$

$$s - f_1 = A(s + f_0) + Bs$$

Polynomial terms of different order are linearly independent, so this equation can be broken into simultaneous equations.

$$\begin{cases} 1 = A + B \\ -f_1 = Af_0 \end{cases}$$

Solving the simultaneous system gives

$$\begin{cases} A = \frac{-f_1}{f_0} = \frac{-V_{E(sat)}}{C} \\ B = 1 - A = 1 + \frac{V_{E(sat)}}{C} \end{cases} \tag{16}$$

and expanded frequency domain equation is

$$V_C(s) = C\left(\frac{A}{s} + \frac{B}{s - f_0}\right) \tag{17}$$

Converting back to time domain gives

$$v_C(t) = CAu(t) + CBe^{-f_0 t}$$

Substituting values for A, B, and C from equations 15 and 16 describes the voltage across the capacitor as a function of time.

$$v_C(t) = -V_{E(sat)} + (2V_{E(sat)} - V_{E(trig)})e^{-t/R_E C_E}$$

Substituting this description of $v_C(t)$ into the right hand side of the equation 13 gives the final solution for discharging voltage at the off emitter.

$$v_{E(off)}(t) = [2V_{E(sat)} - V_{E(trig)}]e^{-t/R_E C_E} \tag{18}$$

The lifetime of this output state is as long as it takes for $v_{E(off)}$ to reach $V_{E(trig)}$.

$$V_{E(trig)} = [2V_{E(sat)} - V_{E(trig)}]e^{-T_{stability}/R_E C_E}$$

$$T_{stability} = R_E C_E ln\left(\frac{2V_{E(sat)} - V_{E(trig)}}{V_{E(trig)}}\right)$$

There are two stable states per period of the square wave, so the frequency of oscillation is

$$f = \frac{1}{2T_{stability}} = \frac{1}{2R_E C_E ln\left(\frac{2V_{E(sat)} - V_{E(trig)}}{V_{E(trig)}}\right)} \tag{19}$$

$$C_E = \frac{1}{2R_E f * ln\left(\frac{2V_{E(sat)} - V_{E(trig)}}{V_{E(trig)}})\right)} \tag{20}$$

3.3 Frequency Characteristics, Using MATLAB

3.4 Advanced Circuit

The astable multivibrator circuit can be improved by adding voltage buffers into the cross-connections and by replacing the emitter resistors with current mirrors. The improved circuit is shown in figure 6.

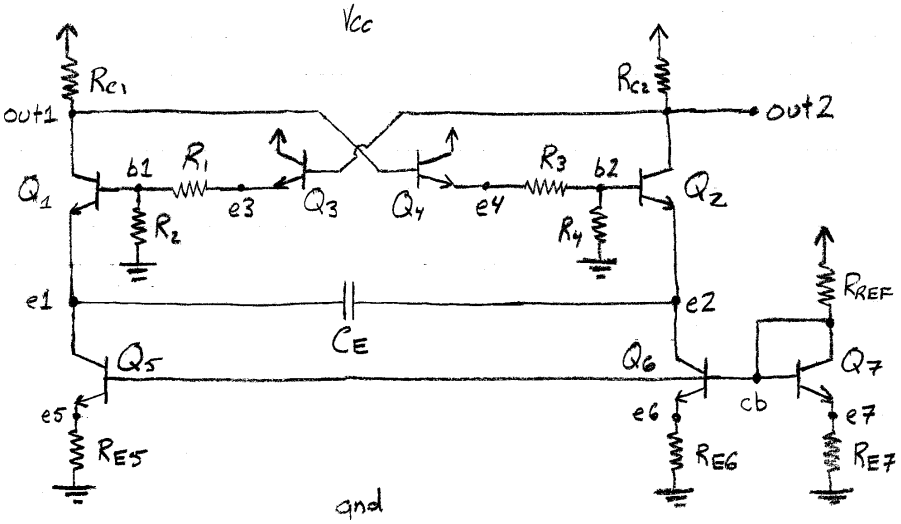

Figure 6: Advanced Version of Astable Multivibrator

The two switching transistors are still labeled Q_1 and Q_2. Transistors Q_3 and Q_4 are emitter-folowers that provided more current to the cross connections. These voltage buffers are an inprovement because R_1 and R_2 can be reduced to inprove the charging time of the parasitic base-emitter junction capacities.

Transistors Q_{5-7} are set up as current mirrors to provide constant current to both of the switching transistors. This is an inprovment because limiting the current with the resistors has unwanted effects on the voltages the cause switching. Additionally, in the simple circuit, the emitter resistors had to be large enough to handle significant power.

The current from the mirrors should be equal to the average transistor current, or half of the saturation current because only one switching transistor is on at any moment.

$$I_{mirror} = I_{C(ave)}$$

For a current mirror, the emitter resistors should be equal and small and the current will be set by the saturation current through R_{REF}.

$$I_{mirror} = \frac{V_{CC} - V_{BE(on)}}{R_{REF} + R_{E7}} \quad \text{or} \quad R_{REF} = \frac{V_{CC} - V_{BE(on)}}{I_{C(ave)}} - R_{E7} \tag{21}$$

After setting up the current mirrors, they can be ignored and replaced by constant current sources. See figure 7.

The amplitude of the output swing and the current from the current mirrors are related by R_C.

$$I_{C(sat)} = 2 * I_{C(ave)} \tag{22}$$

$$R_C = \frac{V_{pkpk}}{I_{C(sat)}} \tag{23}$$

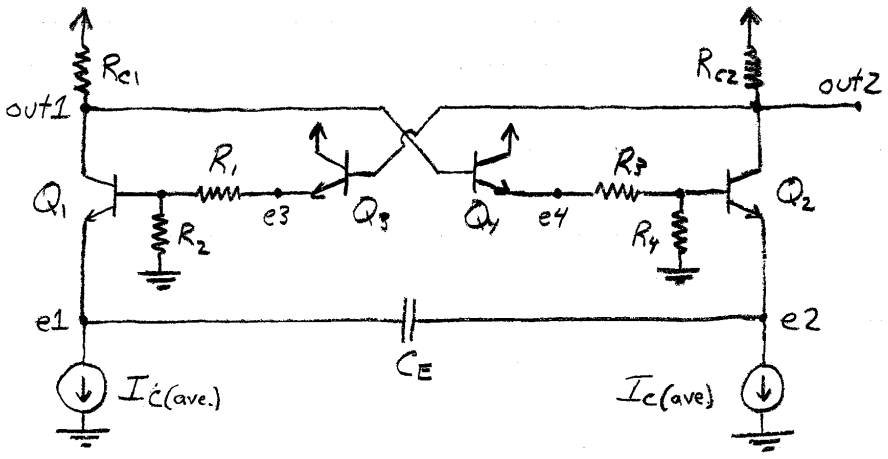

Figure 7: Advanced Circuit with Equivalent Current Sources

The inputs for Q_1 and Q_2 come from the output state of the opposited transistor, after passing through the voltage buffer and a voltage divider.

$$\begin{cases} V_{B(sat)} = \frac{R_2}{R_1+R_2}(V_{CC} - V_{BE(on)}) \\ V_{B(off)} = \frac{R_2}{R_1+R_2}(V_{CC} - V_{pkpk} - V_{BE(on)}) \end{cases}$$

The current state of the switching transistors is stable as long as the potential at the emitter of the off transistor is withing 0.7 V of that transistor's base. The on transistor would remain on indefinitely if the off transistor did not abruptly change the base biasings.

$$\begin{cases} V_{E(sat)} = \frac{R_2}{R_1+R_2}(V_{CC} - V_{BE(on)}) - V_{BE(on)} \\ V_{E(off)} > \frac{R_2}{R_1+R_2}(V_{CC} - V_{pkpk} - V_{BE(on)}) - V_{BE(on)} \end{cases} \tag{24}$$

The top half of the circuit has now been analyzed and equation 24 provide the stability conditions for which we can treat the top half as a black box. To analyze the transient bottom half of the circuit, the top half can be replaced by ideal switches connected to the emitter voltage at saturation from first stability condition. This simplified circuit will remain valid until the emitter voltage at the off switch violates the second stability condition.

$$V_{E(trig)} = \text{Min}(V_{E(off)}) = \frac{R_2}{R_1+R_2}(V_{CC} - V_{pkpk} - V_{BE(on)}) - V_{BE(on)} \tag{25}$$

The equivalent circuit for the transient analysis is shown in figure 8.

At the instant before switching occurs, v_{e1} is shorted to $V_{E(sat)}$ and v_{e2} is approaching $V_{E(trig)}$. So,

$$v_c(0^-) = V_{E(sat)} - V_{E(trig)} \tag{26}$$

The current through the capacitor is fixed by the constant current source of the off transistor's side.

$$i_C(t) = I_{C(ave)}$$

Replacing the capacitor current with the capacitor i-v relationship yields a first order, separable differential equation.

$$-C_E \frac{dv_E}{dt} = I_{C(ave)}$$

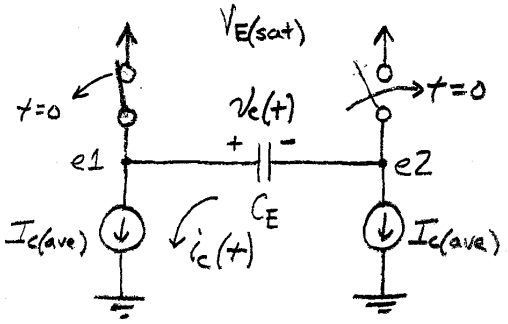

Figure 8: Transient Model for the Advanced Astable Multivibrator

Solving gives an equation for voltage across the capacitor.

$$dv_C = \frac{-I_{C(ave)}}{C_E} dt$$

$$\int 1 * dv_C = \frac{-I_{C(ave)}}{C_E} \int 1 * dt$$

$$v_C(t) = \frac{-I_{C(ave)}}{C_E} t + K$$

The constant from integration should be the initial voltage across the capacitor. Substituting this in from equation 26 gives

$$v_C(t) = \frac{-I_{C(ave)}}{C_E} t + V_{E(sat)} - V_{E(trig)} \tag{27}$$

The voltage across the capacitor is directly related to the off emitter voltage. We are interested in the period of time for which the off emitter voltage is greater than the trigger voltage.

$$v_{E(off)} = V_{E(sat)} + v_C(t)$$

$$v_{E(off)} = V_{E(sat)} + \frac{-I_{C(ave)}}{C_E} t + V_{E(sat)} - V_{E(trig)}$$

$$V_{E(trig)} = V_{E(sat)} + \frac{-I_{C(ave)}}{C_E} T_{stable} + V_{E(sat)} - V_{E(trig)}$$

$$T_{stable} = \frac{2C_{E(trig)}(V_{E(sat)} - V_{E(trig)})}{I_{C(ave)}} \tag{28}$$

The period of stability for one transistor is half of the square wave cycle, so the frequency of oscillation is defined by

$$f = \frac{I_{C(ave)}}{4C_E[V_{E(sat)} - V_{E(trig)}]} \quad , \quad C_E = \frac{I_{C(ave)}}{4f[V_{E(sat)} - V_{E(trig)}]} \tag{29}$$

Table 1: Emitter-Coupled Oscillator Design Specifications

Parameter	Notation	Value
Power Supply	V_{CC}	24 V
Output Signal Amplitude	V_{pkpk}	2 V
Maximum Frequency	f	50 MHz
Average I_C of Switching Transistor	$\frac{I_{C(sat)}}{2}$	6 mA

4 Design and Simulation

4.1 Specifications

For this lab I needed to build a square wave, emitter-coupled oscillator that meets the specifications in table 1.

4.2 BJT Characterization

4.3 Simple Circuit Design

An astable multivibrator was designed with the theory derived in sections 3.1 and 3.2 in order to meet the specifications for the lab in table 1. The circuit diagram is shown again in figure 9.

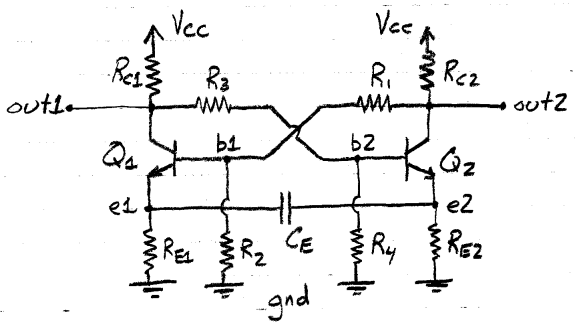

Figure 9: Simple Circuit Diagram

Table 2 shows the values that were calculated while designing the circuit and the corresponding equations used.

When the simple circuit was built according to the original design in table 2, square wave oscillations were observed but the higher frequencies could not be achieved. The most likely cause of this limitation was the delay time associated with charging the parasitic base-emitter junction capacities. Charge has to flow through R_1 and collect on the base for some time. A quick, back-of-the-hand calculation with the junction capacities in table **??** shows this is on the order of 10 ns.

$$\tau = R_1 C_{JE} = 8.9ns \qquad f = 111MHz$$

Table 2: Original Simple Circuit Design

Parameter	Designed Value	Design Method
V_{CC}	24 V	specified
V_{pkpk}	2.4 V	specified +20%
$I_{C(sat)}$	12 mA	$2 * I_{C(ave)}$
$R_1 + R_2$	$20k\Omega$	equation 4
$\frac{R_2}{R_1+R_2}$	0.917	equation 8
$V_{E(sat)}$	21.31 V	equation 9
$V_{E(trig)}$	19.47 V	equation 11
Component	Designed Value	Design Method
R_C	200Ω	equation 1
R_2	$18.3k\Omega$	$R_2 = \frac{R_2}{R_1+R_2}(R_1 + R_2)$
R_1	$1.7k\Omega$	$R_1 = (R_1 + R_2) - R_2$
R_E	$1.7k\Omega$	equation 10
$C_{E(0.1MHz)}$	17,000 pF	equation 20
$C_{E(1MHz)}$	1,700 pF	equation 20
$C_{E(10MHz)}$	170 pF	equation 20
$C_{E(50MHz)}$	17 pF	equation 20

4.4 Simple Circuit Redesign

4.5 Simple Circuit SPICE Simulation

4.6 Advanced Circuit Design

4.7 Advanced Circuit SPICE Simulation

5 Results