Emitter-Coupled Oscillator

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Contents

1 Objective

To investigate the design and operation of an emitter-coupled astable multivibrator for 50 MHz operation.

2 Principles of Operation

In analog electronics, a sinusoidal oscillator is sometimes needed, such as for power conversion, driving a motor, or for the carrier frequency in radio transmissions. These can be built from an amplifier with a passive feedback network, where the gain > 1 and the feedback is positive at the frequency of operation [1]. The only other requirement is that the amplifer operates linearly.

In contrast, digital circuits usually require a square wave clock signal. Ironically, a digital oscillator can be built starting from a basic digital component.

A latch is a digital circuit with two stable states, made from two cross-connected amplifiers. It is a fundamental component in digital logic. In fact, when a master and slave latch are connected in series they form a 1-bit, flip-flop register used in CPUs. Usually, the cross-connection between the two amplifiers is resistive and one amplifier will be driven in saturation while the other is in cutoff. Amplifier in digital circuits are usually driven between saturation and cutoff, making them unlinear, binary (two-state) devices.

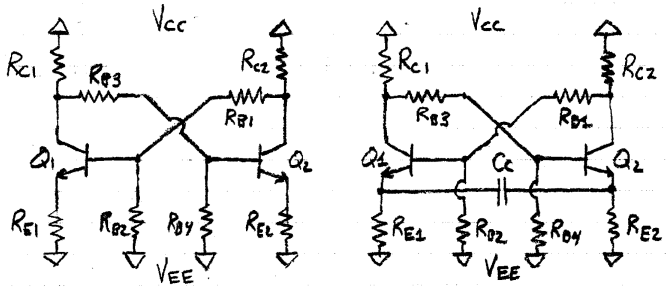

Figure 1: Digial Latch (left) and Latch with Reactive Emitter Coupling (right).

If the cross-connection is made to be reactive, then the latch may not be stable in either state. If it oscillates between the two states and produces a near-square wave, it is called a bistable multivibrator. A capacitor is usually used for the cross-connection because it delays the instantaneous voltage change that would normally occur when a transistor switches between saturation and cutoff.

Analog oscillators produce sinusoids; digital oscillators produce square waves. An analog amplifer oscillates if it has reactive feedback that is positive; a digital flip-flop oscillates if it has reactive cross-connection strong enough to switch states. Analog oscillators use an amplifier in a linear range; digital oscillators use drive amplifier to its two limits. An analog oscillator may form unintentionally through parasitic feedback, such as through the Miller capacitance of a BJT. A digital osciallator may form unintentionally through propagation delay or carry-through logic All of these comparisons between analog and digital oscillators can probably be gleaned from the block-level diagrams in figure 2.

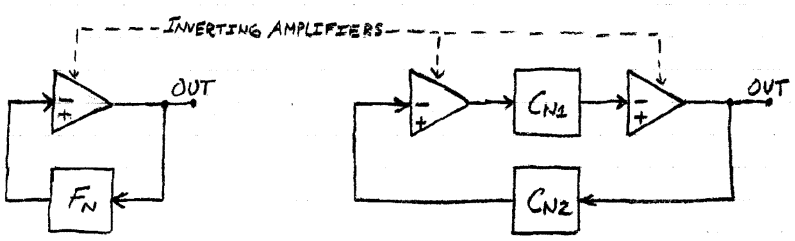

Figure 2: An Analog Feedback Oscillator (left) Compared to Bistable Multivibrator (right)

[1] the Barkhausen Criterion

3 Theory

3.1 Bistable Latch

A digital latch can be built with two cross-connected BJT amplifiers, shown in figure 3. The amplifiers should be nearly mirror images of one another and the coupling networks should be entirely resistive.

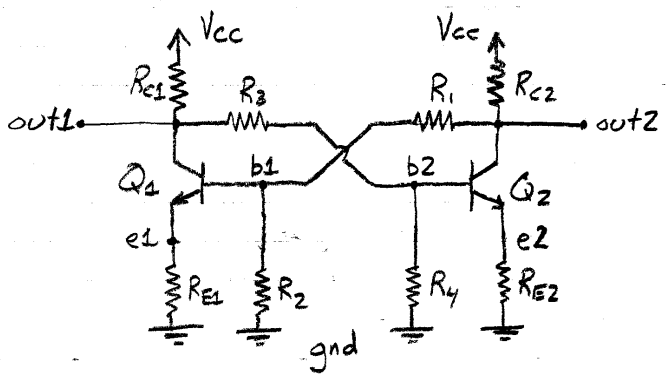

Figure 3: BJT Implementation of a Digital Latch

The latch is bistable, meaning it has two self-sustaining states. Either Q1 is saturated while Q2 is cutoff, or Q1 is cutoff while Q2 is saturated. The circuit is a symmetric loop, so it is not clear where to begin any analysis. Instead of starting at a particular node and time, we will start with some sanity assumptions and determining the conditions that make them true.

If the transistors operate digitally–i.e. either in saturation or cutoff–then the output can have two possible values, the difference between which will be called V_{pkpk}. This difference is set by R_C and the saturation current.

$$R_C = \frac{V_{pkpk}}{I_{C(sat)}} \tag{1}$$

Of course, this assumes that the current through R_1 and R_2 is negligible compared to $I_{C(sat)}$.

$$I_{Bias} << I_{C(sat)}$$

Another design assumption is the stiff base bias. In order to stiffly bias the transistors, the base currents should draw negligible current relative to R_1 and R_2.

$$I_{B(sat)} << I_{Bias}$$

These two biasing network equations compete with each other because the base and collector currents are related by β. The best way to satisfy both is

$$I_{Bias} = \frac{I_{C(sat)}}{\sqrt{\beta}} \tag{2}$$

If the supply voltage is relatively large compared to the output amplitude, then I_{Bias} varies little with binary state and is set by R_1 and R_2.

$$I_{Bias} = \frac{V_{CC}}{R_1 + R_2} \tag{3}$$

Combining equations 2 and 3 helps in designing the bias network.

$$R_1 + R_2 = \frac{\sqrt{\beta} V_{CC}}{I_{C(sat)}} \tag{4}$$

The analysis so far has assumed that the saturation current is fixed, but should it be fixed with R_C or R_E? It makes more sense to limit $I_{C(sat)}$ with R_C because later we will be adding a reactive element to the emitters.

For the transistor to be driven to saturation, V_{CE} is approximately equal to $V_{BE(on)}$ and the collector is equipotential with the base. The collector potential during saturation is the lesser of the two binary outputs, so

$$V_{B(sat)} = V_{CC} - V_{pkpk} \tag{5}$$

For the other transistor to be cutoff, the base-emitter junction must not have achieved the forward bias potential.

$$V_{B(off)} < V_{E(off)} - V_{BE(on)} \tag{6}$$

The transistors are cross-connected from their outputs to the opposite bases, so the base bias is dependent on the opposite transistor's state. The bias networks are voltage dividers and the output has two states, so the base potential is one of the two following values.

$$V_B = \begin{cases} \frac{R_2}{R_1+R_2} V_{CC} & : \text{saturation transistor} \\ \frac{R_2}{R_1+R_2}(V_{CC} - V_{pkpk}) & : \text{cutoff transistor} \end{cases} \tag{7}$$

Combining the required conditions for saturation and cutoff from equations 5 and 6 with the two biasing potentials gives the conditions for stability of the latch.

$$\begin{cases} \frac{R_2}{R_1+R_2} V_{CC} = V_{CC} - V_{pkpk} & : \text{saturation stability} \\ \frac{R_2}{R_1+R_2}(V_{CC} - V_{pk-pk}) < V_{E(off)} + V_{BE(on)} & : \text{cutoff stability} \end{cases}$$

A latch is only useful if the output is self-sustaining, so these two conditions must both be met. The first condition has all fixed values, so the ratio R_2/R_1+R_2 must be chosen there. The second condition can then be rearranged to separate fixed values from as-yet-undetermined values.

$$\begin{cases} \frac{R_2}{R_1+R_2} = \frac{V_{CC}-V_{pkpk}}{V_{CC}} & : \text{saturation stability} \\ V_{E(off)} > \frac{R_2}{R_1+R_2}(V_{CC} - V_{pkpk}) - V_{BE(on)} & : \text{cutoff stability} \end{cases} \tag{8}$$

The stability conditions for both transistors would have to be followed if we were designing digital memory. However, for an oscillator we only want quasi-stable states; in the next section we will violate the stability by adding reative coupling to affect V_E of the off transistor.

3.2 Astable Multivibrator

The simple circuit for an astable multivibrator is shown in figure 4. Topologically it is easy to make–just add a capactitor to a BJT latch.

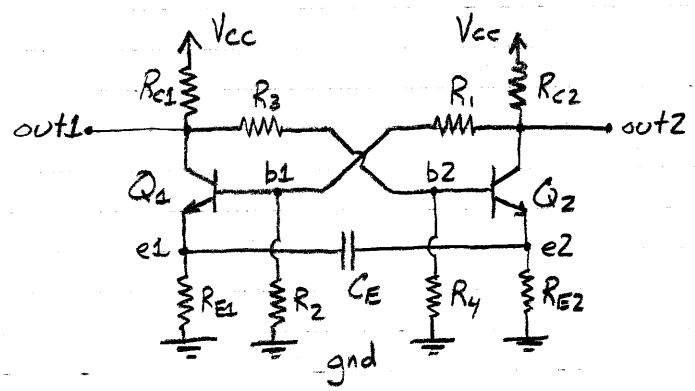

Figure 4: Simple Version of Astable Multivibrator

The top half of the circuit is the same as the latch. The relationships between $I_{C(sat)}$ and V_{pkpk} to R_C, R_1, and R_2 is the same as in equations 1 through 8. Now for the bottom half.

The emitter potential for the saturation transistor is set by the top half because it follow the base. Taking the saturation base voltage from equation 7...

$$V_{E(sat)} = \frac{R_2}{R_1 + R_2} V_{CC} - V_{BE(on)} \tag{9}$$

In a perfect world, this emitter voltage would hold regardless of R_E.[2] However, in the interest of not burning up the base-emitter junction, R_E should probably be just short of becoming the saturation current limiter.

$$R_E = \frac{V_{E(sat)}}{I_{E(sat)}} = \frac{\frac{R_2}{R_1+R_2} V_{CC} - V_{BE(on)}}{I_{C(sat)}} \tag{10}$$

Equation 8 described the stability conditions for the latch. To make an oscillator, the circuit should be quasistable–i.e. it should be stable for some specific length of time. After a period of stable output, an internal trigger cause a change of state. For the emitter-coupled oscillator, the trigger is the emitter potential of the cutoff transistor falling below $V_{E(off)}$. From equation 8, the cutoff state is stable while

$$V_{E(off)} > \frac{R_2}{R_1 + R_2}(V_{CC} - V_{pkpk}) - V_{BE(on)}$$

The capacitor prevents instantaneous voltage changes, so it takes some time for V_E to fall below this trigger threshold. We expect an RC time constant for the discharge to be on order of $\tau = R_E C_E$, but solving for the transient equation may give additional insights.

$$i(t) = C\frac{dv(t)}{dt} \qquad \text{resists instantaneous } \delta V$$

The cross-connected bases make the transistors behave somewhat like a emitter-follower voltage source. If we assume that switching times for the transistors is negligible, then the transient circuit

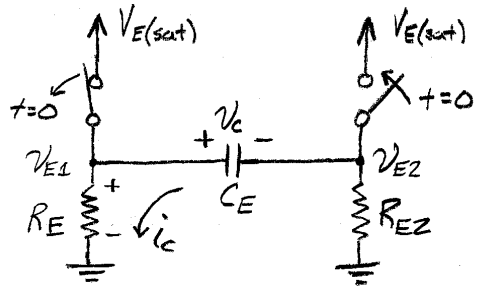

Figure 5: Transient Circuit for Simple Emitter-Coupled Oscillator

is as shown in figure 5. This assumption is true if the base-emitter capacitance is negligible, and so is the delay in the BJT due to the rate of minority carrier diffusion.

At t=0, Q_2 triggers itself on by v_{E2} falling below the threshold. In turn, this forces Q_1 off through the cross connection. This trigger occurs when $v_{E2(off)}$ breaks the stability condition.

$$V_{E(trig)} = \frac{R_2}{R_1 + R_2}(V_{CC} - V_{pkpk}) - V_{BE(on)} \tag{11}$$

Immediately before the trigger occurs, the voltage at E1 is $V_{E(sat)}$ and the voltage at E2 is the trigger voltage $V_{E(trig)}$. So, the initial voltage across the capacitor is

$$v_C(0^-) = V_{E(sat)} - V_{E(trig)} \tag{12}$$

With the initial conditions in hand, we are ready to analyze the transient circuit. After switching, R_{E2} does not matter because Q_2 acts like a voltage source. Consequently there is only one loop to analyze: the v_{E1} discharge loop. The differential equation describing the loop is found from Kirchoff's Voltage Law.

$$v_{E1}(t) := \quad R_E i_C(t) = V_{E(sat)}u(t) + v_C(t) \tag{13}$$

$$R_E\left(-C_E\frac{dv_C(t)}{dt}\right) = V_{E(sat)}u(t) + v_C(t)$$

$$\frac{d}{dt}v_C(t) + \frac{1}{R_E C_E}v_C(t) = \frac{-V_{E(sat)}}{R_E C_E}u(t) \tag{14}$$

The system will be easier to solve in frequency domain. Taking the Laplace transform gives

$$sV_C(s) - v_C(0^-) + \frac{1}{R_E C_E}V_C(s) = \frac{-V_{E(sat)}}{sR_E C_E}$$

$$V_C(s)\left[s^2 + \frac{s}{R_E C_E}\right] = sv_C(0^-) - \frac{V_{E(sat)}}{R_E C_E}$$

$$V_C(s) = \frac{sv_C(0^-) - \frac{V_{E(sat)}}{R_E C_E}}{s(s + \frac{1}{R_E C_E})}$$

$$V_C(s) = [V_{E(sat)} - V_{E(trig)}]\left[\frac{s - \frac{V_{E(sat)}}{R_E C_E(V_{E(sat)} - V_{E(trig)})}}{s(s + \frac{1}{R_E C_E})}\right]$$

[2]Actually in a perfect world, I would have already graduated.

$$V_C(s) = C\frac{s - f_1}{s(s + f_0)} \quad \text{where} \begin{cases} C = V_{E(sat)} - V_{E(trig)} \\ f_0 = \frac{1}{R_E C_E} \\ f_1 = f_0 \frac{V_{E(sat)}}{C} \end{cases} \tag{15}$$

Before converting back to time domain, a partial fraction expansion must be done.

$$\frac{s - f_1}{s(s + f_0)} = \frac{A}{s} + \frac{B}{s + f_0} = \frac{A(s + f_0) + Bs}{s(s + f_0)}$$

$$s - f_1 = A(s + f_0) + Bs$$

Polynomial terms of different order are linearly independent, so this equation can be broken into simultaneous equations.

$$\begin{cases} 1 = A + B \\ -f_1 = Af_0 \end{cases}$$

Solving the simultaneous system gives

$$\begin{cases} A = \frac{-f_1}{f_0} = \frac{-V_{E(sat)}}{C} \\ B = 1 - A = 1 + \frac{V_{E(sat)}}{C} \end{cases} \tag{16}$$

and expanded frequency domain equation is

$$V_C(s) = C\left(\frac{A}{s} + \frac{B}{s - f_0}\right) \tag{17}$$

Converting back to time domain gives

$$v_C(t) = CAu(t) + CBe^{-f_0 t}$$

Substituting values for A, B, and C from equations 15 and 16 describes the voltage across the capacitor as a function of time.

$$v_C(t) = -V_{E(sat)} + (2V_{E(sat)} - V_{E(trig)})e^{-t/R_E C_E}$$

Substituting this description of $v_C(t)$ into the right hand side of the equation 13 gives the final solution for discharging voltage at the off emitter.

$$v_{E(off)}(t) = [2V_{E(sat)} - V_{E(trig)}]e^{-t/R_E C_E} \tag{18}$$

The lifetime of this output state is as long as it takes for $v_{E(off)}$ to reach $V_{E(trig)}$.

$$V_{E(trig)} = [2V_{E(sat)} - V_{E(trig)}]e^{-T_{stability}/R_E C_E}$$

$$T_{stability} = R_E C_E ln\left(\frac{2V_{E(sat)} - V_{E(trig)}}{V_{E(trig)}}\right)$$

There are two stable states per period of the square wave, so the frequency of oscillation is

$$f = \frac{1}{2T_{stability}} = \frac{1}{2R_E C_E ln\left(\frac{2V_{E(sat)} - V_{E(trig)}}{V_{E(trig)}}\right)} \tag{19}$$

$$C_E = \frac{1}{2R_E f * ln\left(\frac{2V_{E(sat)} - V_{E(trig)}}{V_{E(trig)}})\right)} \tag{20}$$

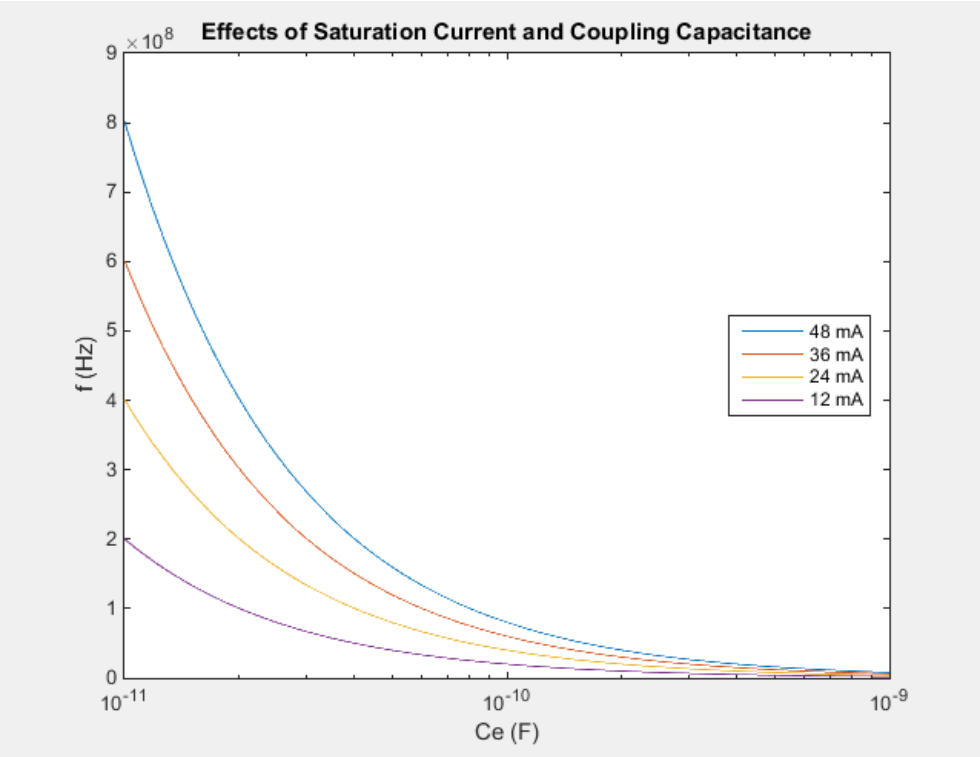

Figure 6: Effects of Varying C_E and $I_{C(sat)}$ on Frequency of Oscillation

3.3 Frequency Characteristics, Using MATLAB

To better visualized the effects of design parameters on the frequency of oscillation, equation 19 was plotted in MATLAB as a function of several parameters. The results are shown in plots 6, 7, and 8. The generic MATLAB script that was used to generate these plots is include in appendix 7.1.

3.4 Advanced Circuit

The astable multivibrator circuit can be improved by adding voltage buffers into the cross-connections and by replacing the emitter resistors with current mirrors. The improved circuit is shown in figure 9.

The two switching transistors are still labeled Q_1 and Q_2. Transistors Q_3 and Q_4 are emitter-folowers that provided more current to the cross connections. These voltage buffers are an inprovement because R_1 and R_2 can be reduced to inprove the charging time of the parasitic base-emitter junction capacities.

Transistors Q_{5-7} are set up as current mirrors to provide constant current to both of the switching transistors. This is an inprovment because limiting the current with the resistors has unwanted effects on the voltages the cause switching. Additionally, in the simple circuit, the emitter resistors had to be large enough to handle significant power.

The current from the mirrors should be equal to the average transistor current, or half of the saturation current because only one switching transistor is on at any moment.

$$I_{mirror} = I_{C(ave)}$$

For a current mirror, the emitter resistors should be equal and small and the current will be set

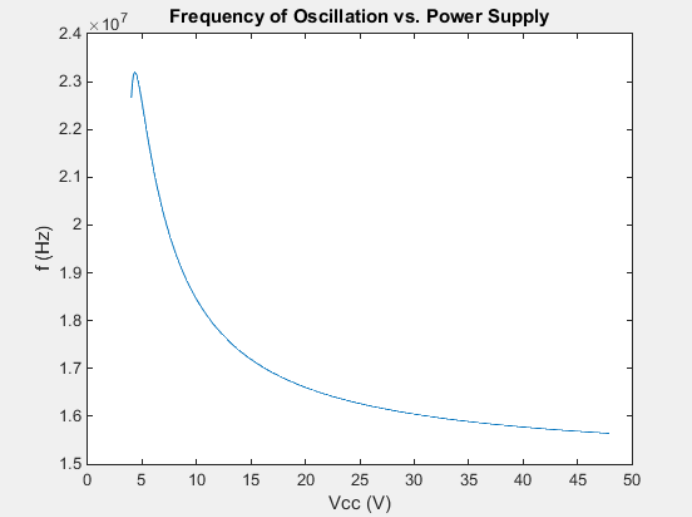

Figure 7: Effect of V_{CC} Design on Frequency of Oscillation

by the saturation current through R_{REF}.

$$I_{mirror} = \frac{V_{CC} - V_{BE(on)}}{R_{REF} + R_{E7}} \quad \text{or} \quad R_{REF} = \frac{V_{CC} - V_{BE(on)}}{I_{C(ave)}} - R_{E7} \tag{21}$$

After setting up the current mirrors, they can be ignored and replaced by constant current sources. See figure 10.

The amplitude of the output swing and the current from the current mirrors are related by R_C.

$$I_{C(sat)} = 2 * I_{C(ave)} \tag{22}$$

$$R_C = \frac{V_{pkpk}}{I_{C(sat)}} \tag{23}$$

The inputs for Q_1 and Q_2 come from the output state of the opposited transistor, after passing through the voltage buffer and a voltage divider.

$$\begin{cases} V_{B(sat)} = \frac{R_2}{R_1+R_2}(V_{CC} - V_{BE(on)}) \\ V_{B(off)} = \frac{R_2}{R_1+R_2}(V_{CC} - V_{pkpk} - V_{BE(on)}) \end{cases}$$

The current state of the switching transistors is stable as long as the potential at the emitter of the off transistor is withing 0.7 V of that transistor's base. The on transistor would remain on indefinitely if the off transistor did not abruptly change the base biasings.

$$\begin{cases} V_{E(sat)} = \frac{R_2}{R_1+R_2}(V_{CC} - V_{BE(on)}) - V_{BE(on)} \\ V_{E(off)} > \frac{R_2}{R_1+R_2}(V_{CC} - V_{pkpk} - V_{BE(on)}) - V_{BE(on)} \end{cases} \tag{24}$$

The top half of the circuit has now been analyzed and equation 24 provide the stability conditions for which we can treat the top half as a black box. To analyze the transient bottom half of the circuit, the top half can be replaced by ideal switches connected to the emitter voltage at saturation from first stability condition. This simplified circuit will remain valid until the emitter voltage at the off switch violates the second stability condition.

$$V_{E(trig)} = \text{Min}(V_{E(off)}) = \frac{R_2}{R_1 + R_2}(V_{CC} - V_{pkpk} - V_{BE(on)}) - V_{BE(on)} \tag{25}$$

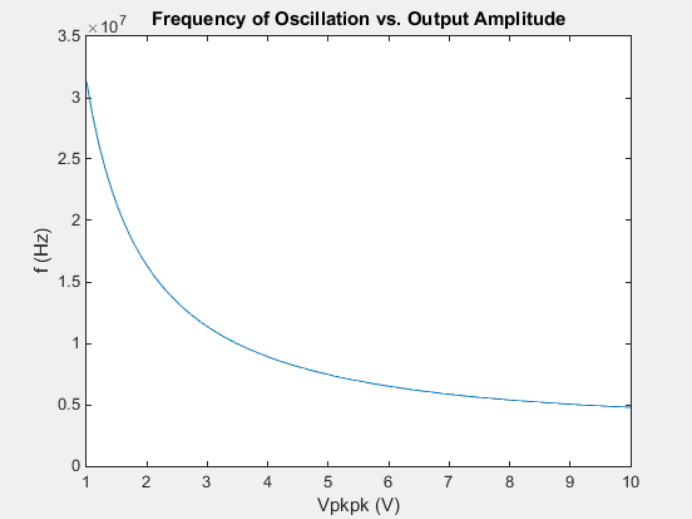

Figure 8: Effect of V_{pkpk} Design on Frequency of Oscillation

The equivalent circuit for the transient analysis is shown in figure 11.

At the instant before switching occurs, v_{e1} is shorted to $V_{E(sat)}$ and v_{e2} is approaching $V_{E(trig)}$. So,

$$v_c(0^-) = V_{E(sat)} - V_{E(trig)} \tag{26}$$

The current through the capacitor is fixed by the constant current source of the off transistor's side.

$$i_C(t) = I_{C(ave)}$$

Replacing the capacitor current with the capacitor i-v relationship yields a first order, separable differential equation.

$$-C_E \frac{dv_E}{dt} = I_{C(ave)}$$

Solving gives an equation for voltage across the capacitor.

$$dv_C = \frac{-I_{C(ave)}}{C_E} dt$$

$$\int 1 * dv_C = \frac{-I_{C(ave)}}{C_E} \int 1 * dt$$

$$v_C(t) = \frac{-I_{C(ave)}}{C_E} t + K$$

The constant from integration should be the initial voltage across the capacitor. Substituting this in from equation 26 gives

$$v_C(t) = \frac{-I_{C(ave)}}{C_E} t + V_{E(sat)} - V_{E(trig)} \tag{27}$$

The voltage across the capacitor is directly related to the off emitter voltage. We are interested in the period of time for which the off emitter voltage is greater than the trigger voltage.

$$v_{E(off)} = V_{E(sat)} + v_C(t)$$

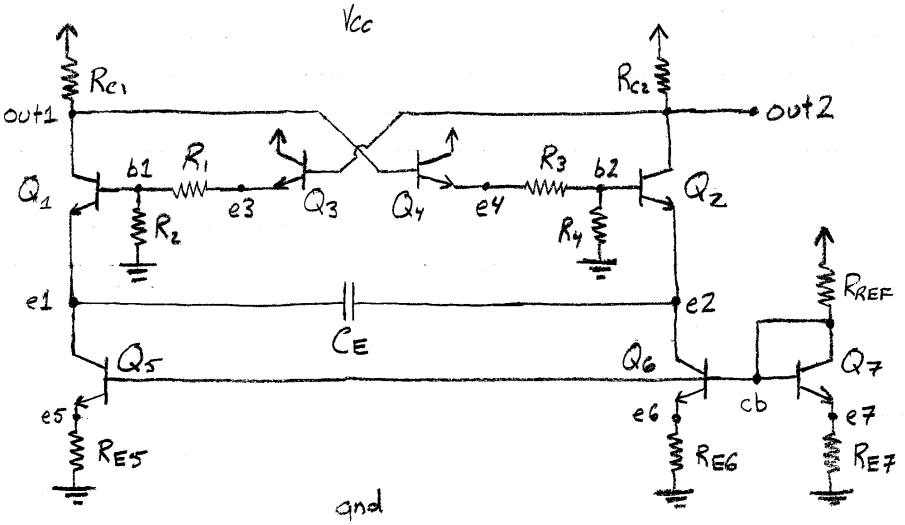

Figure 9: Advanced Version of Astable Multivibrator

$$v_{E(off)} = V_{E(sat)} + \frac{-I_{C(ave)}}{C_E}t + V_{E(sat)} - V_{E(trig)}$$

$$V_{E(trig)} = V_{E(sat)} + \frac{-I_{C(ave)}}{C_E}T_{stable} + V_{E(sat)} - V_{E(trig)}$$

$$T_{stable} = \frac{2C_{E(trig)}(V_{E(sat)} - V_{E(trig)})}{I_{C(ave)}} \tag{28}$$

The period of stability for one transistor is half of the square wave cycle, so the frequency of oscillation is defined by

$$f = \frac{I_{C(ave)}}{4C_E[V_{E(sat)} - V_{E(trig)}]} \quad , \quad C_E = \frac{I_{C(ave)}}{4f[V_{E(sat)} - V_{E(trig)}]} \tag{29}$$

4 Design and Simulation

4.1 Specifications

For this lab I needed to build a square wave, emitter-coupled oscillator that meets the specifications in table 1.

Table 1: Emitter-Coupled Oscillator Design Specifications

Parameter	Notation	Value
Power Supply	V_{CC}	24 V
Output Signal Amplitude	V_{pkpk}	2 V
Maximum Frequency	f	50 MHz
Average I_C of Switching Transistor	$I_{C(ave)}$	6 mA

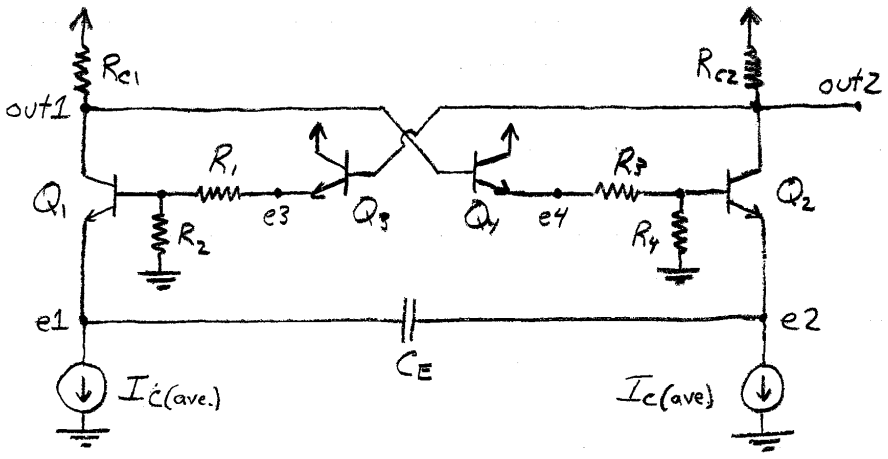

Figure 10: Advanced Circuit with Equivalent Current Sources

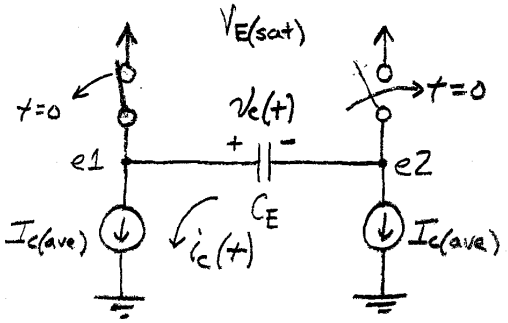

Figure 11: Transient Model for the Advanced Astable Multivibrator

4.2 BJT Characterization

Nine 2N3904 BJTs were characterized on the Tektronix Curve Tracer and HP LCR Meter, for use in the simple and advanced circuits. The important characteristics are summarized in table 2. All nine collector-emitter I-V curves are included in appendix 7.2.

4.3 Simple Circuit Design

An astable multivibrator was designed with the theory derived in sections 3.1 and 3.2 in order to meet the specifications for the lab in table 1. The circuit diagram is shown again in figure 12.

Table 3 shows the values that were calculated while designing the circuit and the corresponding equations used.

When the simple circuit was built according to the original design in table 3, square wave oscillations were observed but the higher frequencies could not be achieved. The most likely cause of this limitation was the delay time associated with charging the parasitic base-emitter junction capacities. Charge has to flow through R_1 and collect on the base for some time. A quick, back-of-the-hand calculation with the junction capacities in table 2 shows this is on the order of 10 ns.

$$\tau = R_1 C_{JE} = 8.9ns \qquad f = 111MHz$$

Table 2: BJT Measured Characteristics

Label	β	C_{JC}	C_{JE}	V_A
Q_1	176	3.291 pF	5.255 pF	121 V
Q_2	153	3.199 pF	5.235 pF	120 V
Q_3	294	4.224 pF	9.605 pF	116 V
Q_4	171	3.304 pF	5.291 pF	118 V
Q_5	171	3.309 pF	5.252 pF	118 V
Q_6	170	3.306 pF	5.213 pF	117 V
Q_7	170	3.288 pF	5.287 pF	117 V
Q_8	175	3.306 pF	5.242 pF	89.5 V
Q_9	201	3.222 pF	4.9464 pF	119 V

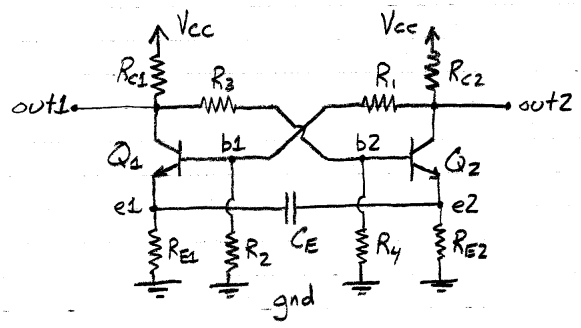

Figure 12: Simple Circuit Diagram

This is definitely in the range that could interfere with 50 MHz oscillation. In order to inprove the oscillator for higher frequencies, the circuit needed to be redesigned.

4.4 Simple Circuit Redesign

The parasitic capacitance of the switching transistors cannot be changed. However, the corresponding RC time constant can be reduced by reducing R_1. Unfortunately, this will violate my biasing assumption that the current through the cross-connections be negligible relative to the saturation current.

The new design decision will be this: the current through the cross-connection networks will be equal to the saturation current through the transistor. Several equations change to accomodate this new design. Equation 4

$$R_1 + R_2 = \frac{V_{CC}}{I_{C(sat)}} \tag{30}$$

equation 8 changes to

$$\begin{cases} \frac{R_2}{R_1+R_2} = \frac{V_{CC}-2V_{pkpk}}{V_{CC}-V_{pkpk}} & \text{: saturation} \\ V_{E(off)} > \frac{R_2}{R_1+R_2}(V_{CC}-2V_{pkpk}) - V_{BE(on)} & \text{: cutoff} \end{cases} \tag{31}$$

equation 9 changes to

$$V_{E(sat)} = \frac{R_2}{R_1+R_2}(V_{CC}-V_{pkpk}) - V_{BE(on)} \tag{32}$$

Table 3: Original Simple Circuit Design

Parameter	Designed Value	Design Method
V_{CC}	24 V	specified
V_{pkpk}	2.4 V	specified +20%
$I_{C(sat)}$	12 mA	$2 * I_{C(ave)}$
$R_1 + R_2$	$20k\Omega$	equation 4
$\frac{R_2}{R_1+R_2}$	0.917	equation 8
$V_{E(sat)}$	21.31 V	equation 9
$V_{E(trig)}$	19.47 V	equation 11
Component	Designed Value	Design Method
R_{C1}, R_{C2}	200Ω	equation 1
R_2, R_4	$18.3k\Omega$	$R_2 = \frac{R_2}{R_1+R_2}(R_1 + R_2)$
R_1, R_3	$1.7k\Omega$	$R_1 = (R_1 + R_2) - R_2$
R_{E1}, R_{E2}	$1.7k\Omega$	equation 10
$C_{E(0.1MHz)}$	17,000 pF	equation 20
$C_{E(1MHz)}$	1,700 pF	equation 20
$C_{E(10MHz)}$	170 pF	equation 20
$C_{E(50MHz)}$	17 pF	equation 20

equation 11 changes to

$$V_{E(trig)} = \frac{R_2}{R_1 + R_2}(V_{CC} - 2V_{pkpk}) - V_{BE(on)} \tag{33}$$

and equation 10 changes to

$$R_E = \frac{\frac{R_2}{R_1+R_2}(V_{CC} - V_{pkpk}) - V_{BE(on)}}{I_{C(sat)}} \tag{34}$$

The simple circuit was redesigned with these new criteria, and this is listed in table 4. In addition to redesigning the current ratio through the cross-connection, I also doubled the saturation current from my original specification to further increase the frequency of oscillation. The idea for doing this came from the theoretical frequency and the MATLAB plot in figure 6.

4.5 Simple Circuit SPICE Simulation

The redesigned simple circuit was simulated in NGSPICE using the design values in table 4 and the BJT parameters from table 2. The netlist used for simulation is include in appendix 7.3.

The results of the transient analysis for the $50.4pF$ coupling capacitance are shown in figures 13 and 14. The simulation showed a frequency of 40 MHz, which was reasonably close to 50 MHz, for which $C_E = 50.4pF$ was calculated.

4.6 Advanced Circuit Design

The advanced circuit, shown in figure 9, was designed according to the theory in section 3.4 in order to meet the specifications in table 1. The values calculated and equations used are collected chronologically (in the order of calculation) in table 5.

[3]doubled the specified current to improve frequency, see plot 6

[4]had to increase $R_1 + R_2$ in order to reduce power to $\frac{1}{4}$ Watt for available resistors.

[5]Reduce R_2 to improve τ_{CJE}, the charging time of the parasitic base-emitter capacitance.

Table 4: Simple Circuit Redesign

Parameter	Designed Value	Design Method	Adjusted Value
V_{CC}	24 V	specified	-
V_{pkpk}	2.4 V	specified +20%	-
$I_{C(sat)}$	12 mA	$2 * I_{C(ave)}$	$[24mA]^3$
$R_1 + R_2$	$1k\Omega$	equation 30	$[2k\Omega]^4$
$\frac{R_2}{R_1+R_2}$	0.909	equation 31	-
$V_{E(sat)}$	19.30 V	equation 32	-
$V_{E(trig)}$	18.11 V	equation 33	-
Component	Designed Value	Design Method	Measured Value
R_{C1}, R_{C2}	200Ω	equation 1	98.6Ω, 98.2Ω
R_2, R_4	1818Ω	$R_2 = \frac{R_2}{R_1+R_2}(R_1 + R_2)$	1791Ω, 1796Ω
R_1, R_3	182Ω	$R_1 = (R_1 + R_2) - R_2$	147.8Ω, 146.5Ω
R_{E1}, R_{E2}	1608Ω	equation 10	899Ω, 899Ω
$C_{E(0.1MHz)}$	25,200 pF	equation 20	25,710 pF
$C_{E(1MHz)}$	2,5200 pF	equation 20	1,922 pF
$C_{E(10MHz)}$	252 pF	equation 20	153.4 pF
$C_{E(50MHz)}$	25 pF	equation 20	14.57 pF

4.7 Advanced Circuit SPICE Simulation

The advanced circuit with designed values was simulated using NGSPICE with the netlist shown in appendix 7.4. The transient simulation using $C_E = 42.9pF$ is shown in figures 15 and 16. The simulated frequency is almost exactly 50 MHz.

5 Results

5.1 Simple Circuit

The simple circuit designed in table 4 was built on a breadboard according to the circuit diagram from figure 4. Different capacitors were inserted for C_E in order to tune the oscillator to 4 different frequencies: 0.1 MHz, 1 MHz, 10 MHz, and 50 MHz.

A screenshot from the oscilloscope was captured for each of the four frequencies and the final capacitors used were measured and recorded in table 4. The screenshots are shown in figures 17, 18, 19, and 20 in order of increasing frequency.

5.2 Advanced Circuit

The advanced circuit designed in table 5 was built on a breadboard according to the circuit diagram from figure 9. Different capacitors were inserted for C_E in order to tune the oscillator to 4 different frequencies: 0.1 MHz, 1 MHz, 10 MHz, and 50 MHz.

A screenshot from the oscilloscope was captured for each of the four frequencies and the final capacitors used were measured and recorded in table 5. The screenshots are shown in figures 21, 22, 23, and 24 in order of increasing frequency.

5.3 Results Summary Table

The measured frequency and capacitance for all 8 experimental waveforms are summarized in table **??** and compared to the designed values. Also included in the table is the output amplitude and a

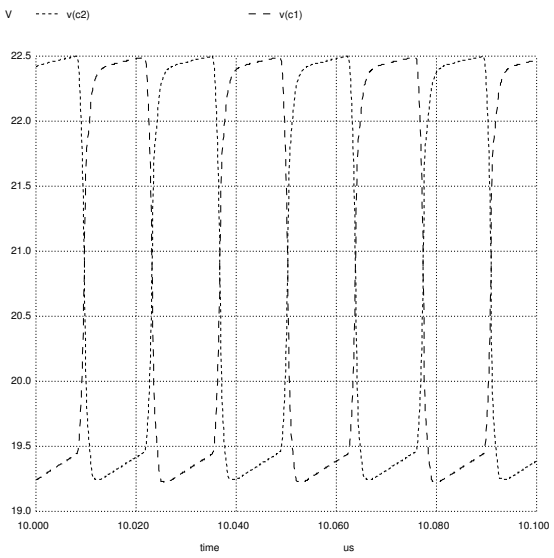

Figure 13: Simulated Ouput Wave of Redesigned Simple Circuit

qualitative description of the waveform.

6 Conclusions

Both the simple circuit and advanced circuits were successful in meeting the specifications outlined for lab. The simple circuit was able to achieve oscillations at 50 MHz, albeit with reduced ouptut voltage. At frequencies below 50 MHz the simple circuit achieved its targeted output voltage of $> 2V_{pkpk}$ and had generally square properties. The advanced circuit produced a near perfect square wave at lower frequencies and was able to oscillate at up to $44MHz$ while still achieving the targeted output voltage. At higher frequencies the square wave morphed into a rounded triagular wave.

The theory sections were able to predict the operation of the circuits very accurately for the lower frequencies. At higher frequencies the results were slightly skewed because parasitic capacitance and minority carrier drift rates were not considered. The simulations also agreed with the results, although they failed to predict the lower limits of the coupling capacitance for which the real circuit would still operate.

The circuits could be further inproved by optimizing the design to reduce R_1 in the cross-connecting voltage dividers. This would reduce the charging delay caused by the parasitic base-emitter junction capacites. Another inprovement would be reducing V_{CC} so that smaller power resistors could still be used. Furthermore, V_{CC} would likely have to be lowered in order to reduce the resistance R_1.

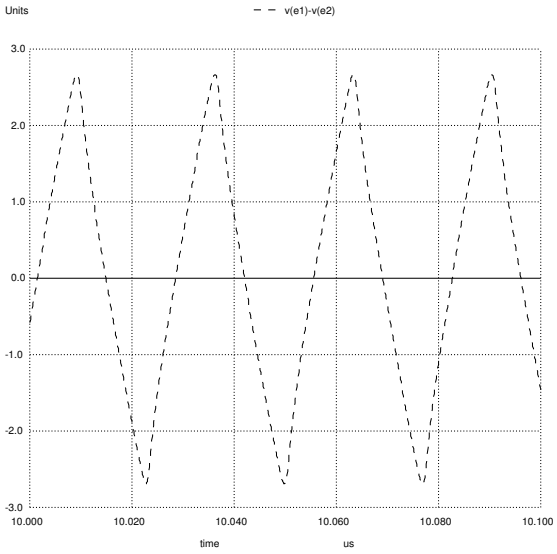

Figure 14: Simulated Voltage Across C_E for Redesigned Simple Circuit

Table 5: Advanced Circuit Design

Parameter	Designed Value	Design Method	Adjusted Value
V_{CC}	24 V	specified	-
V_{pkpk}	2.4 V	specified +20%	-
$I_{C(sat)}$	12 mA	$2 * I_{C(ave)}$	-
$R_1 + R_2$	$< 1250\Omega$	$\frac{1}{2}W = \frac{V_{CC}}{R_1+R_2}$	-
$\frac{R_2}{R_1+R_2}$	$\frac{1}{2}$	arbitrary	$[\frac{1}{5}]^5$
$V_{E(sat)}$	4.18 V	equation 24	-
$V_{E(trig)}$	3.48 V	equation 25	-
Component	Designed Value	Design Method	Measured Value
R_{C1}, R_{C2}	200Ω	equation 23	197.1Ω, 196.5Ω
R_2, R_4	250Ω	$R_2 = \frac{R_2}{R_1+R_2}(R_1 + R_2)$	248.1Ω, 249.0Ω
R_1, R_3	1000Ω	$R_1 = (R_1 + R_2) - R_2$	1013Ω, 1007Ω
R_{REF}	$4k\Omega$	equation 21	$3.871k\Omega$
R_{E5}, R_{E6}, R_{E7}	2.2Ω	smallest available	2.19Ω, 2.16Ω, 2.18Ω
$C_{E(0.1MHz)}$	21,400 pF	equation 29	45,870 pF
$C_{E(1MHz)}$	2,140 pF	equation 29	3,080 pF
$C_{E(10MHz)}$	214 pF	equation 29	213.1 pF
$C_{E(50MHz)}$	42.9 pF	equation 29	20.57 pF

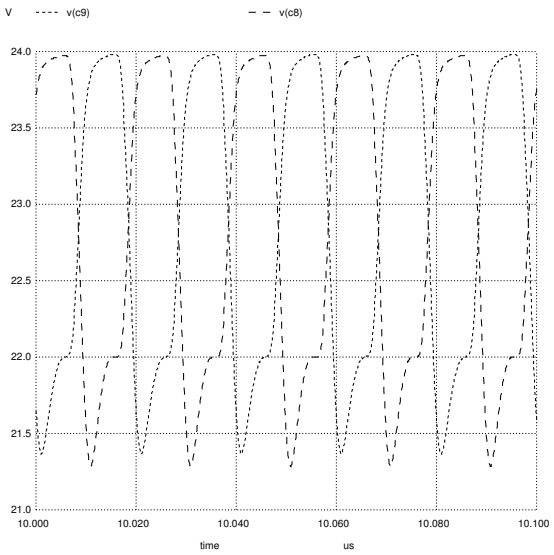

Figure 15: Simulated Ouput Wave of Advanced Circuit

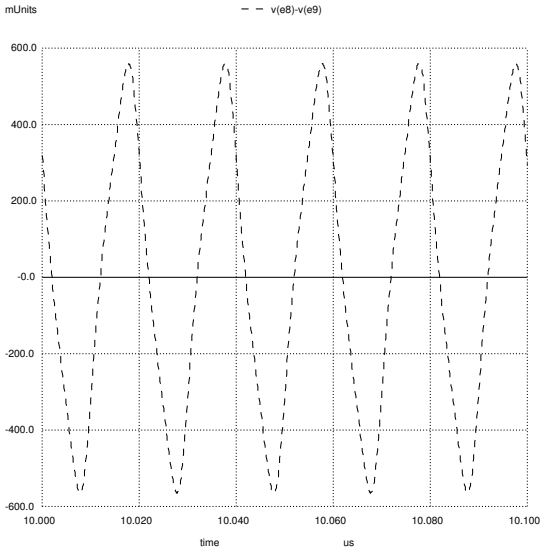

Figure 16: Simulated Voltage Across C_E for Advanced Circuit

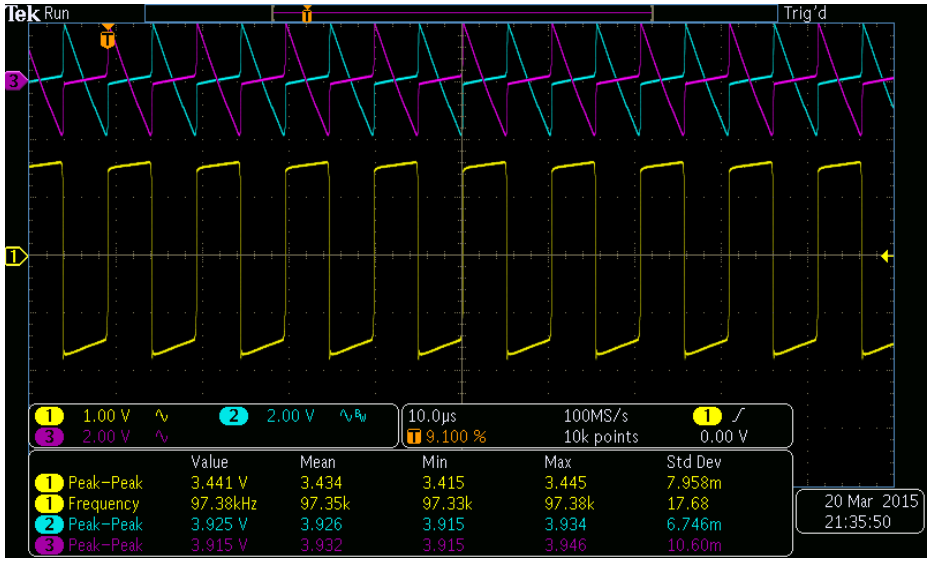

Figure 17: Redesigned Simple Circuit Tuned to 0.1 MHz

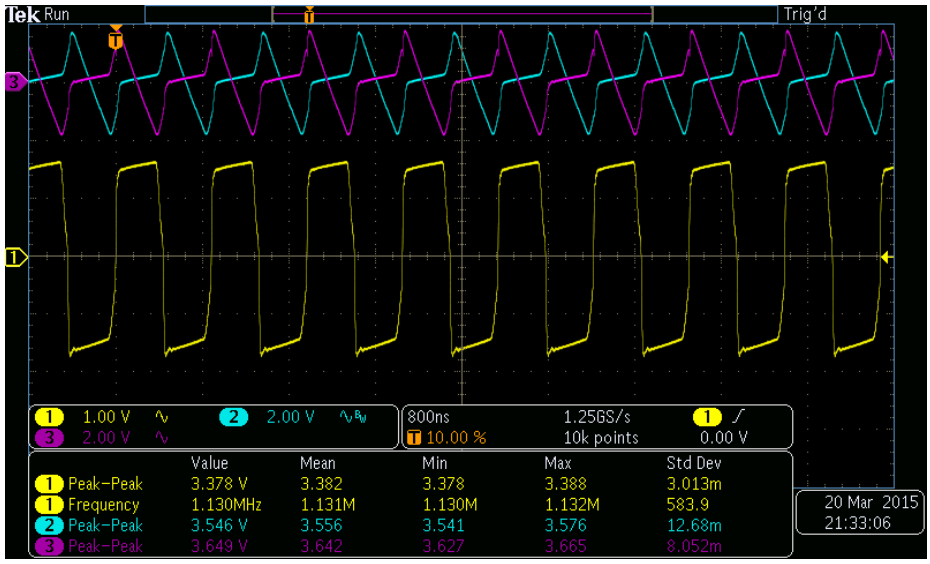

Figure 18: Redesigned Simple Circuit Tuned to 1 MHz

Table 6: Results Summary Table

Circuit	Design f	Design C_E	SPICE f	f	C_E	V_{pkpk}	Wave Shape
Simple	0.1 MHz	25.2 nF	-	97.4 kHz	27.7 nF	3.44 V	square with slight slope
	1 MHz	2.52 nF	-	1.13 MHz	1.92 nF	3.38 V	mostly square
	10 MHz	252 pF	-	9.56 MHz	153.4 pF	3.31 V	Yosimite Half Dome
	50 MHz	25.2 pF	40 MHz	49.1 MHz	14.57 pF	1.24 V	triangular
Advanced	0.1 MHz	21.4 nF	-	94.6 kHz	45.87 nF	3.26 V	square
	1 MHz	2.14 nF	-	1.21 MHz	3.08 nF	3.40 V	square with higher harmonics
	10 MHz	214 pF	-	10.9 MHz	213.1 pF	5.08 V	distorded
	50 MHz	42.9 pF	50 MHz	44.4 MHz	20.57 pF	2.51 V	ocean waves

Figure 19: Redesigned Simple Circuit Tuned to 10 MHz

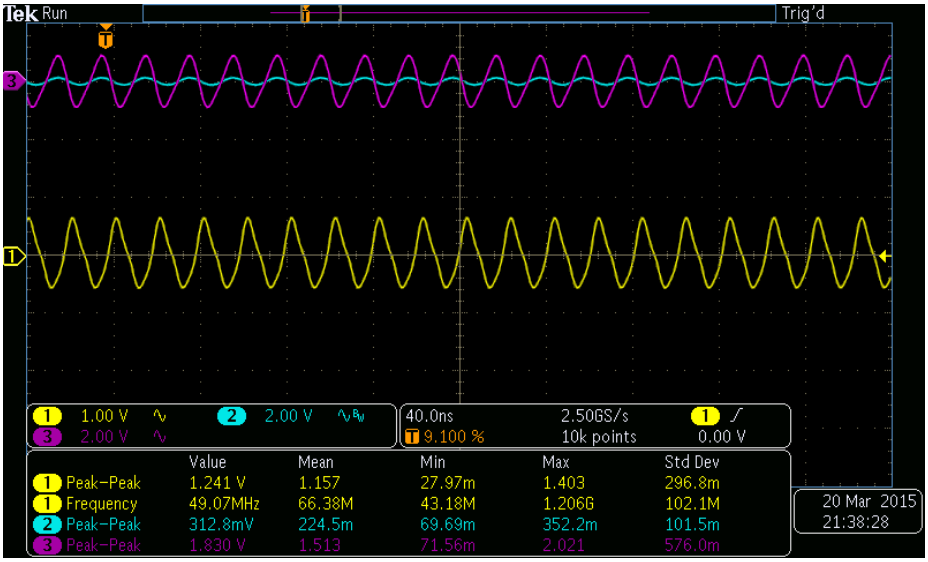

Figure 20: Redesigned Simple Circuit Tuned to 50 MHz

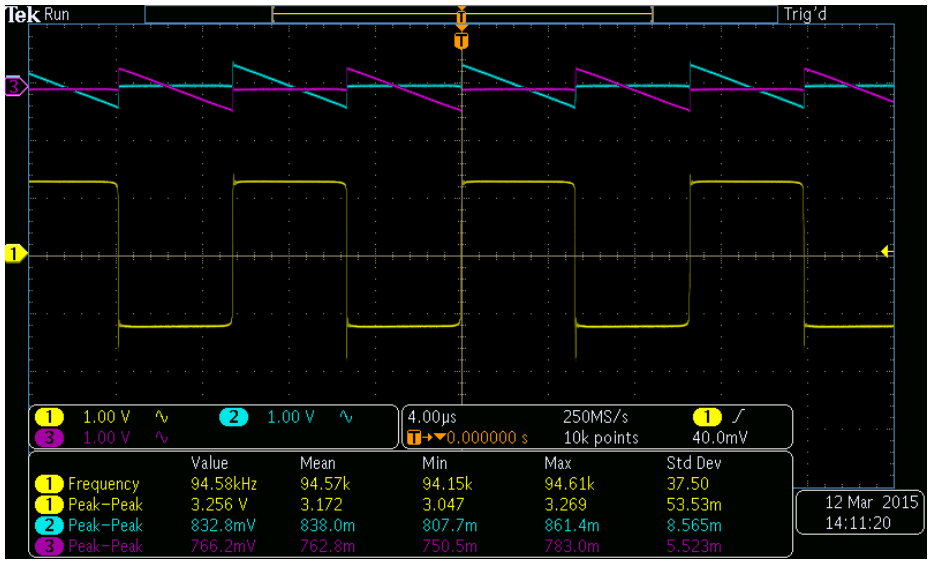

Figure 21: Advanced Circuit Tuned to 0.1 MHz

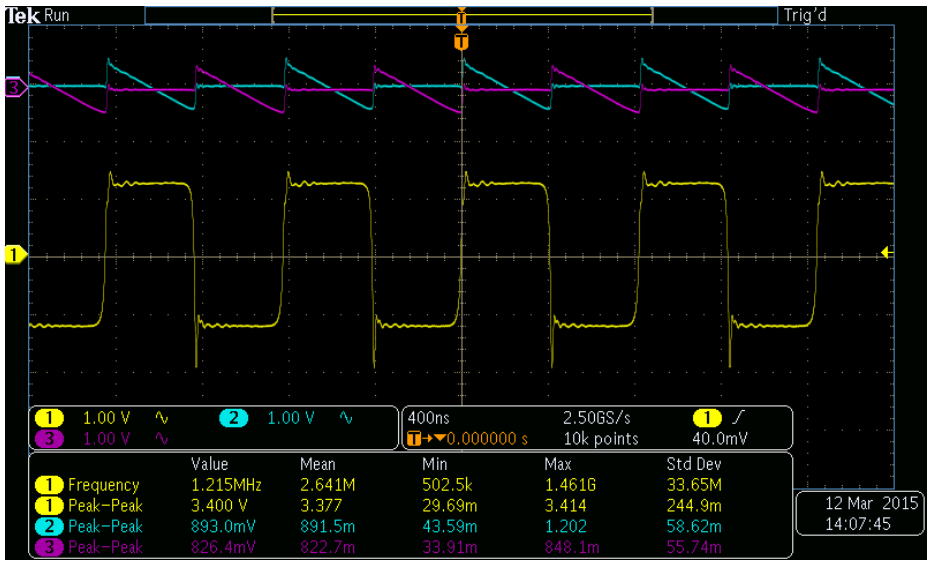

Figure 22: Advanced Circuit Tuned to 1 MHz

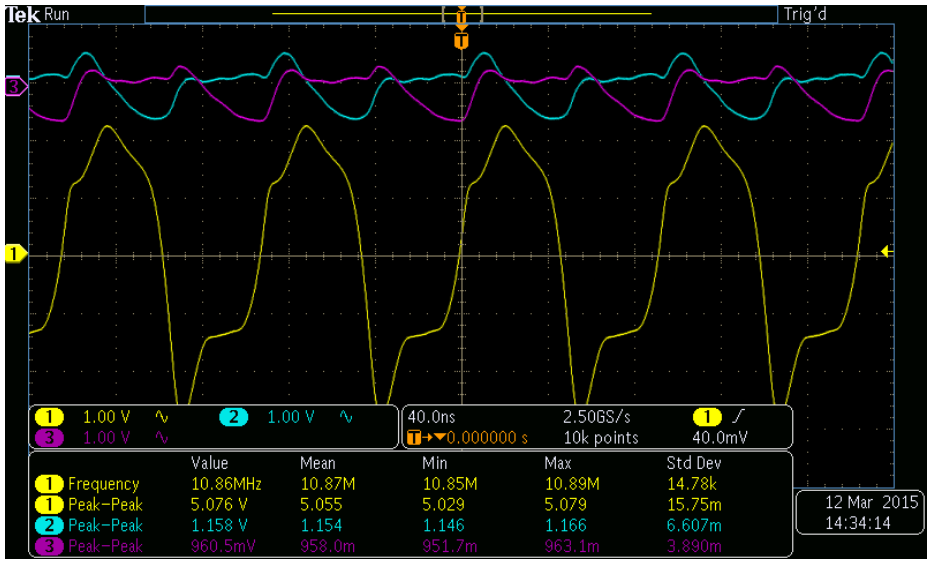

Figure 23: Advanced Circuit Tuned to 10 MHz

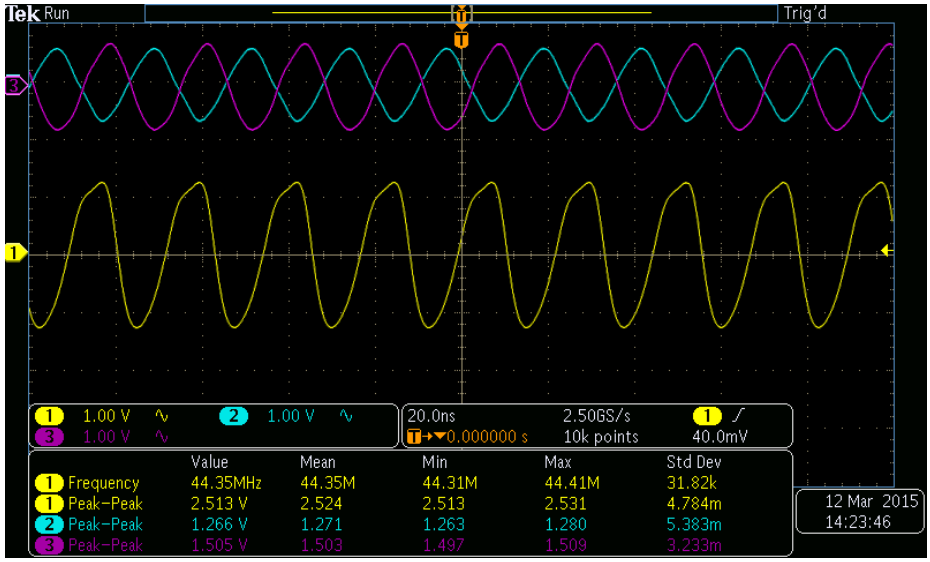

Figure 24: Advanced Circuit Tuned to 50 MHz

7 Appendices

7.1 MATLAB Script for Frequency Function

```
clear
clf
% simple_multivibrator.m
%
% The following 5 parameters can be either a scalar or an array.
% Entering 4 as scalars and 1 as an array allows exploring the effects
% of each on the frequency of oscillation.
% No checks are made on whether oscillations would actually occur.
%
Vcc = 5;
Vpkpk = 2.4;
IcSat = .012;
Ce = 1E-12:1E-13:1E-9;
beta = 100;
%
% The following matrix operations follow the design equations in the
% sections titled "Bistable Latch" and "Astable Multivibrator" of my report.
%
Rc = Vpkpk./IcSat;
R1plusR2 = sqrt(beta) .* (Vcc ./ IcSat);
VoltageDividerRatio = ((Vcc - Vpkpk) ./ Vcc);
R2 = R1plusR2 .* VoltageDividerRatio;
R1 = R1plusR2 - R2;
VeTrig = (VoltageDividerRatio .* (Vcc - Vpkpk)) - 0.7;
VeSat = (VoltageDividerRatio .* Vcc) - 0.7;
Re = VeSat ./ IcSat;
T = (Ce.*Re) .* log ((2*VeSat - VeTrig)./VeTrig);
f = 1 ./ (2 * T);
%
% The plot below should be edited for whichever parameter you are testing.
%
semilogx (Ce, f);
% plot (Vcc, f);
title ('Frequency of Oscillation vs. Coupling Capacitance');
xlabel ('Ce (F)');
ylabel ('f (Hz)');
```

7.2 BJT Characterization Curves

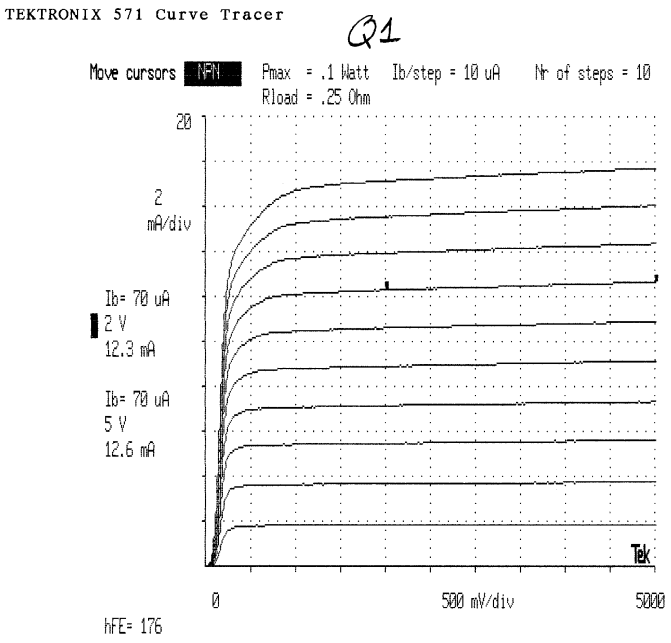

Figure 25: Q_1 Characteristic Collector-Emitter I-V Curve

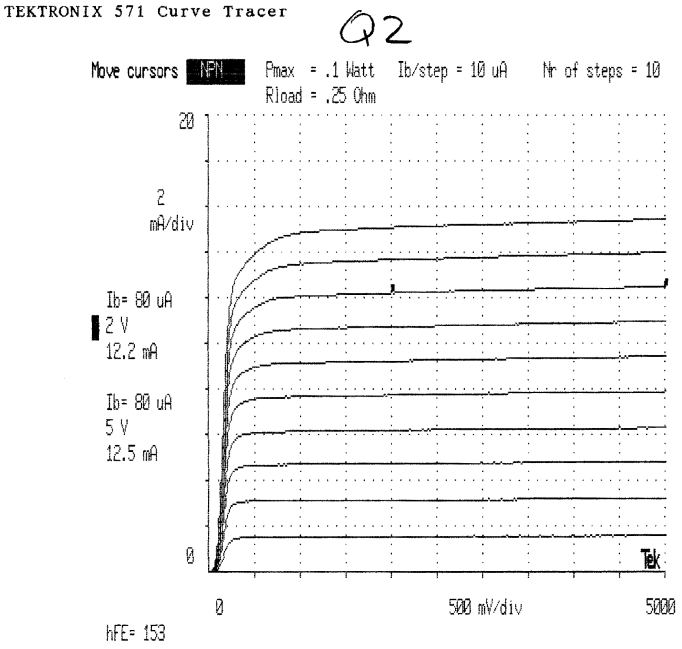

Figure 26: Q_2 Characteristic Collector-Emitter I-V Curve

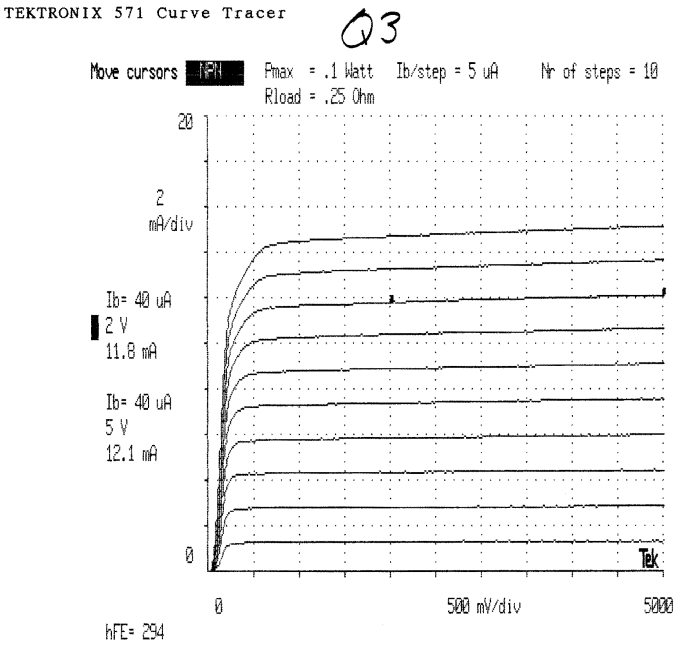

Figure 27: Q_3 Characteristic Collector-Emitter I-V Curve

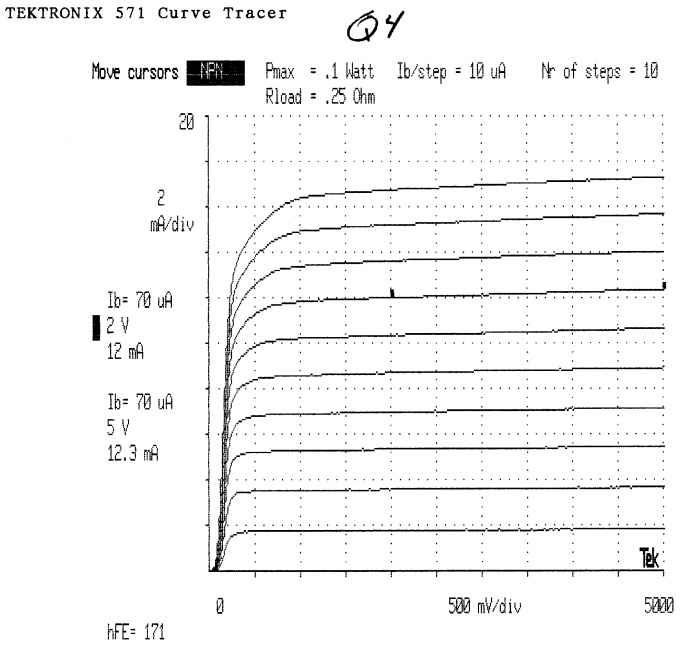

Figure 28: Q_4 Characteristic Collector-Emitter I-V Curve

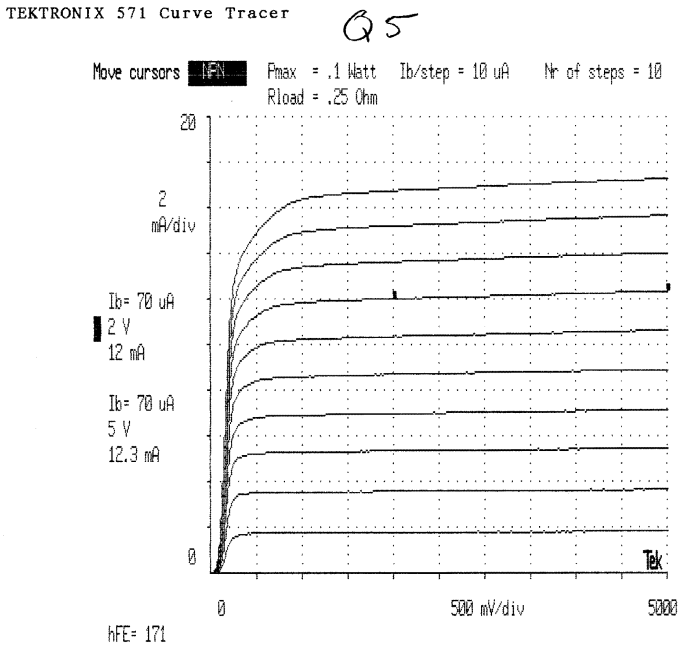

Figure 29: Q_5 Characteristic Collector-Emitter I-V Curve

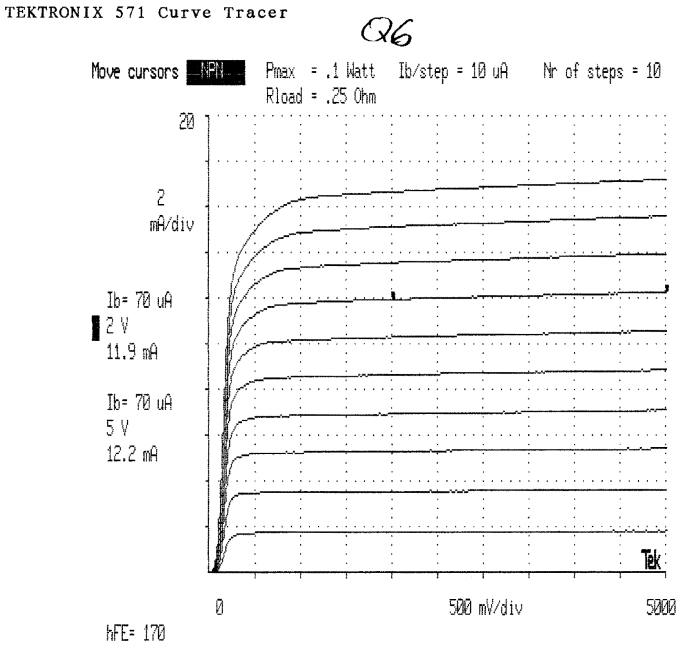

Figure 30: Q_6 Characteristic Collector-Emitter I-V Curve

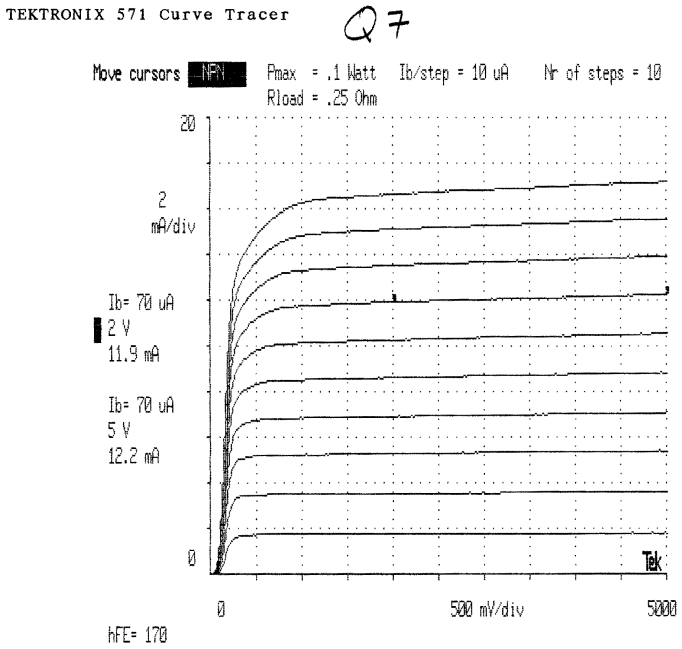

Figure 31: Q_7 Characteristic Collector-Emitter I-V Curve

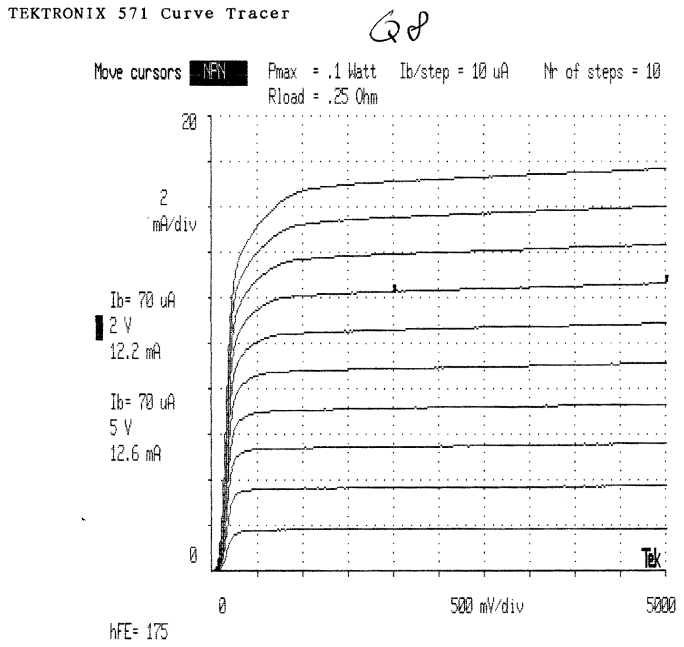

Figure 32: Q_8 Characteristic Collector-Emitter I-V Curve

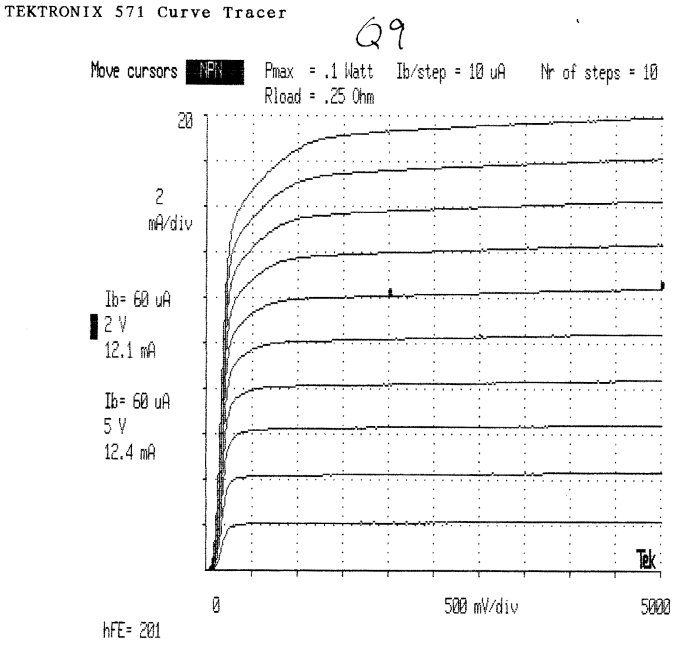

Figure 33: Q_9 Characteristic Collector-Emitter I-V Curve

7.3 SPICE Netlist for Simple Circuit

The circuit diagram shown in figure 4 was typed into a text editor in the standard netlist format for SPICE. The nodes in the netlist correspond to the nodes in the circuit diagram. The netlist below was then piped to NGSPICE for simulation.

```
*** simple.cir ***
* Nodes:
* cc, ee, c1, b1, e1, c2, b2, e2

Vcc cc gnd dc 24V ac 0V
Vee ee gnd dc 0V ac 0V
Rc1 cc c1 98.6
Rc2 cc c2 98.2
Q1 c1 b1 e1 model1
Q2 c2 b2 e2 model2
Re1 e1 ee 899
Re2 e2 ee 899
Rb1 b1 c2 147.8
Rb3 b2 c1 146.5
Rb2 b1 ee 1791
Rb4 b2 ee 1796
Cc e1 e2 50.4E-12


* .model <name> <type> (par1=value1 par2=value2 ...)
* VAF = forward Early voltage
* BF = forward beta; forward common-emitter gain
* CJE = base-emitter zero-bias junction capacitance
* CJC = base-collector zero-bias junction capacitance
* TS = transport saturation current
* NF = forward mode ideality factor

.model model1 npn (BF=176 CJC=3.291p CJE=5.255p IS=1E-16 VAF=121 NF=1)
.model model2 npn (BF=153 CJC=3.199p CJE=5.235p IS=1E-16 VAF=120 NF=1)

.control
set filetype=ascii
* tran <tstep> <tstop> <tstart> <tmax> ; the last two are optional

tran 1E-10 1E-6 1E-10
plot v(c1)
write simple-transient.txt v(c1)

tran 1E-10 101E-7 100E-7 1E-10
plot v(c1) v(c2)
plot v(e1)-v(e2)
```

7.4 SPICE Netlist for Advanced Circuit

The circuit diagram in figure 9 was used to generate a netlist for simulating the advanced circuit. The nodes and component names correspond to the labeling on the circuit diagram and the values correspond to the design values in table 5.

```
*** advanced.cir ***
* Nodes:
* cc, ee, c8, b8, e8, c9, b9, e9, e3, e4, b567, e5, e6, e7

Vcc cc gnd dc 24V ac 0V
Vee ee gnd dc 0V ac 0V
Rc1 cc c8 200
Rc2 cc c9 200
Q1 c8 b8 e8 model8
Q2 c9 b9 e9 model9
Rb1 b8 e3 1000
Rb3 b9 e4 1000
Rb2 b8 ee 250
Rb4 b9 ee 250
Q3 cc c9 e3 model3
Q4 cc c8 e4 model4
Cc e8 e9 42.9E-12
Q5 e8 b567 e5 model5
Q6 e9 b567 e6 model6
Q7 b567 b567 e7 model7
Rref cc b567 4k
Re5 e5 ee 2.2
Re6 e6 ee 2.2
Re7 e7 ee 2.2

* .model <name> <type> (par1=value1 par2=value2 ...)
* VAF = forward Early voltage
* BF = forward beta; forward common-emitter gain
* CJE = base-emitter zero-bias junction capacitance
* CJC = base-collector zero-bias junction capacitance
* TS = transport saturation current
* NF = forward mode ideality factor

.model model8 npn (BF=175 CJC=3.306p CJE=5.242p IS=1E-16 VAF=89.5 NF=1)
.model model9 npn (BF=201 CJC=3.222p CJE=4.964p IS=1E-16 VAF=119 NF=1)
.model model3 npn (BF=294 CJC=4.224p CJE=9.605p IS=1E-16 VAF=116 NF=1)
.model model4 npn (BF=171 CJC=3.304p CJE=5.291p IS=1E-16 VAF=118 NF=1)
.model model5 npn (BF=171 CJC=3.309p CJE=5.252p IS=1E-16 VAF=118 NF=1)
.model model6 npn (BF=170 CJC=3.306p CJE=5.213p IS=1E-16 VAF=117 NF=1)
.model model7 npn (BF=170 CJC=3.288p CJE=5.287p IS=1E-16 VAF=117 NF=1)

.control
set filetype=ascii
* tran <tstep> <tstop> <tstart> <tmax> ; the last two are optional
tran 1E-10 101E-7 100E-7 1E-10
plot v(c8) v(c9)
```

```
plot v(e8)-v(e9)
```