Emitter-Coupled Oscillator

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1 Objective

To investigate the design and operation of an emitter-coupled astable multivibrator for 50 MHz operation.

2 Principles of Operation

In analog electronics, a sinusoidal oscillator is sometimes needed, such as for power conversion, driving a motor, or for the carrier frequency in radio transmissions. These can be built from an amplifier with a passive feedback network, where the gain > 1 and the feedback is positive at the frequency of operation [1]. The only other requirement is that the amplifer operates linearly.

In contrast, digital circuits usually require a square wave clock signal. Ironically, a digital oscillator can be built starting from a basic digital component.

A flip-flop is a digital circuit with two stable states, made from two cross-connected amplifiers. It is a fundamental component in digital logic. In fact, when a master and slave flip-flop are connected in series they form a 1-bit register used in CPUs. Usually, the cross-connection between the two amplifiers is resistive and one amplifier will be driven in saturation while the other is in cutoff. Amplifier in digital circuits are usually driven between saturation and cutoff, making them unlinear, binary (two-state) devices.

DIGITAL FLIP-FLOP AND FLIP FLOP WITH REACTIVE EMITTER COUPLING

If the cross-connection is made to be reactive, then the flip-flop may not be stable in either state. If it oscillates between the two states and produces a near-square wave, it is called a bistable multivibrator. A capacitor is usually used for the cross-connection because it delays the instantaneous voltage change that would normally occur when a transistor switches between saturation and cutoff.

Analog oscillators produce sinusoids; digital oscillators produce square waves. An analog amplifer oscillates if it has reactive feedback that is positive; a digital flip-flop oscillates if it has reactive cross-connection strong enough to switch states. Analog oscillators use an amplifier in a linear range; digital oscillators use drive amplifier to its two limits. An analog oscillator may form unintentionally through parasitic feedback, such as through the Miller capacitance of a BJT. This happens to many frustrated students building amplifiers in Electronics Lab. [2] A digital osciallator may form unintentionally through propagation delay or carry-through logic. This happens to many frustrated students simulating a CPU in Computer Architecture. All of these comparisons between analog and digital oscillators can probably be gleaned from the block, system-level diagrams in figure **??**.

OSCILLATOR BLOCK DIAGRAMS AND CORRESPONDING V-T SIGNALS

The flip-flip circuit shown above was not really indended to oscillate. It can be improved by replacing the emitter resistors with constant current mirrors and adding voltage buffers in the cross-connections to improve charging time of the switching junctions and improve output resistance.

ADVANCED CIRCUIT DIAGRAM

[1] the Barkhausen Criterion

[2] see my last lab

3 Theory

3.1 Bistable Latch

A digital latch can be built with two cross-connected BJT amplifiers, shown in figure 1. The amplifiers should be nearly mirror images of one another and the coupling networks should be entirely resistive.

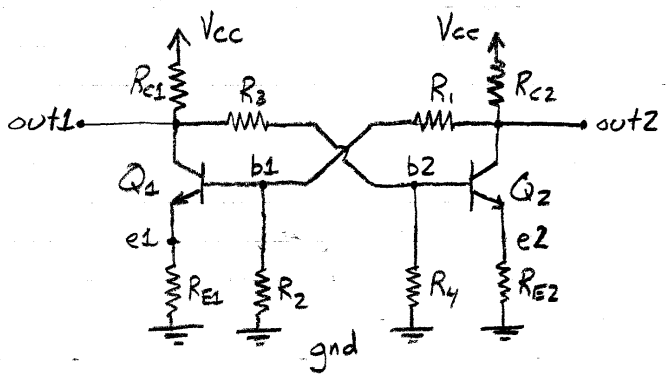

Figure 1: BJT Implementation of a Digital Latch

The latch is bistable, meaning it has two self-sustaining states. Either Q1 is saturated while Q2 is cutoff, or Q1 is cutoff while Q2 is saturated. The circuit is a symmetric loop, so it is not clear where to begin any analysis. Instead of starting at a particular node and time, we will start with some sanity assumptions and determining the conditions that make them true.

If the transistors operate digitally–i.e. either in saturation or cutoff–then the output can have two possible values, the difference between which will be called V_{pkpk}. This difference is set by R_C and the saturation current.

$$R_C = \frac{V_{pkpk}}{I_{C(sat)}} \tag{1}$$

Of course, this assumes that the current through R_1 and R_2 is negligible compared to $I_{C(sat)}$.

$$I_{Bias} << I_{C(sat)}$$

Another design assumption is the stiff base bias. In order to stiffly bias the transistors, the base currents should draw negligible current relative to R_1 and R_2.

$$I_{B(sat)} << I_{Bias}$$

These two biasing network equations compete with each other because the base and collector currents are related by β. The best way to satisfy both is

$$I_{Bias} = \frac{I_{C(sat)}}{\sqrt{\beta}} \tag{2}$$

If the supply voltage is relatively large compared to the output amplitude, then I_{Bias} varies little with binary state and is set by R_1 and R_2.

$$I_{Bias} = \frac{V_{CC}}{R_1 + R_2} \tag{3}$$

Combining equations 2 and 3 helps in designing the bias network.

$$R_1 + R_2 = \frac{\sqrt{\beta} V_{CC}}{I_{C(sat)}} \tag{4}$$

The analysis so far has assumed that the saturation current is fixed, but should it be fixed with R_C or R_E? It makes more sense to limit $I_{C(sat)}$ with R_C because later we will be adding a reactive element to the emitters.

For the transistor to be driven to saturation, V_{CE} is approximately equal to $V_{BE(on)}$ and the collector is equipotential with the base. The collector potential during saturation is the lesser of the two binary outputs, so

$$V_{B(sat)} = V_{CC} - V_{pkpk} \tag{5}$$

For the other transistor to be cutoff, the base-emitter junction must not have achieved the forward bias potential.

$$V_{B(off)} < V_{E(off)} - V_{BE(on)} \tag{6}$$

The transistors are cross-connected from their outputs to the opposite bases, so the base bias is dependent on the opposite transistor's state. The bias networks are voltage dividers and the output has two states, so the base potential is one of the two following values.

$$V_B = \begin{cases} \frac{R_2}{R_1+R_2} V_{CC} & : \text{saturation transistor} \\ \frac{R_2}{R_1+R_2}(V_{CC} - V_{pkpk}) & : \text{cutoff transistor} \end{cases} \tag{7}$$

Combining the required conditions for saturation and cutoff from equations 5 and 6 with the two biasing potentials gives the conditions for stability of the latch.

$$\begin{cases} \frac{R_2}{R_1+R_2} V_{CC} = V_{CC} - V_{pkpk} & : \text{saturation stability} \\ \frac{R_2}{R_1+R_2}(V_{CC} - V_{pk-pk}) < V_{E(off)} + V_{BE(on)} & : \text{cutoff stability} \end{cases}$$

A latch is only useful if the output is self-sustaining, so these two conditions must both be met. The first condition has all fixed values, so the ratio R_2/R_1+R_2 must be chosen there. The second condition can then be rearranged to separate fixed values from as-yet-undetermined values.

$$\begin{cases} \frac{R_2}{R_1+R_2} = \frac{V_{CC}-V_{pkpk}}{V_{CC}} & : \text{saturation stability} \\ V_{E(off)} > \frac{R_2}{R_1+R_2}(V_{CC} - V_{pkpk}) - V_{BE(on)} & : \text{cutoff stability} \end{cases} \tag{8}$$

The stability conditions for both transistors would have to be followed if we were designing digital memory. However, for an oscillator we only want quasi-stable states; in the next section we will violate the stability by adding reative coupling to affect V_E of the off transistor.

3.2 Astable Multivibrator

The simple circuit for an astable multivibrator is shown in figure 2. Topologically it is easy to make–just add a capactitor to a BJT latch.

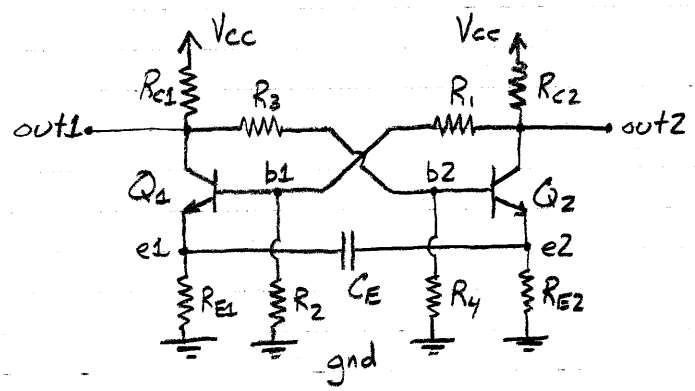

Figure 2: Simple Version of Astable Multivibrator

The top half of the circuit is the same as the latch. The relationships between $I_{C(sat)}$ and V_{pkpk} to R_C, R_1, and R_2 is the same as in equations 1 through 8. Now for the bottom half.

The emitter potential for the saturation transistor is set by the top half because it follow the base. Taking the saturation base voltage from equation 7...

$$V_{E(sat)} = \frac{R_2}{R_1 + R_2} V_{CC} - V_{BE(on)} \tag{9}$$

In a perfect world, this emitter voltage would hold regardless of R_E.[3] However, in the interest of not burning up the base-emitter junction, R_E should probably be just short of becoming the saturation current limiter.

$$R_E = \frac{V_{E(sat)}}{I_{E(sat)}} = \frac{\frac{R_2}{R_1+R_2} V_{CC} - V_{BE(on)}}{I_{C(sat)}} \tag{10}$$

Equation 8 described the stability conditions for the latch. To make an oscillator, the circuit should be quasistable–i.e. it should be stable for some specific length of time. After a period of stable output, an internal trigger cause a change of state. For the emitter-coupled oscillator, the trigger is the emitter potential of the cutoff transistor falling below $V_{E(off)}$. From equation 8, the cutoff state is stable while

$$V_{E(off)} > \frac{R_2}{R_1 + R_2}(V_{CC} - V_{pkpk}) - V_{BE(on)}$$

The capacitor prevents instantaneous voltage changes, so it takes some time for V_E to fall below this trigger threshold. We expect an RC time constant for the discharge to be on order of $\tau = R_E C_E$, but solving for the transient equation may give additional insights.

$$i(t) = C\frac{dv(t)}{dt} \qquad \text{resists instantaneous } \delta V$$

The cross-connected bases make the transistors behave somewhat like a emitter-follower voltage source. If we assume that switching times for the transistors is negligible, then the transient circuit

Figure 3: Transient Circuit for Simple Emitter-Coupled Oscillator

is as shown in figure 3. This assumption is true if the base-emitter capacitance is negligible, and so is the delay in the BJT due to the rate of minority carrier diffusion.

At t=0, Q_2 triggers itself on by v_{E2} falling below the threshold. In turn, this forces Q_1 off through the cross connection. This trigger occurs when $v_{E2(off)}$ breaks the stability condition.

$$V_{E(trig)} = \frac{R_2}{R_1 + R_2}(V_{CC} - V_{pkpk}) - V_{BE(on)} \tag{11}$$

Immediately before the trigger occurs, the voltage at E1 is $V_{E(sat)}$ and the voltage at E2 is the trigger voltage $V_{E(trig)}$. So, the initial voltage across the capacitor is

$$v_C(0^-) = V_{E(sat)} - V_{E(trig)} \tag{12}$$

With the initial conditions in hand, we are ready to analyze the transient circuit. After switching, R_{E2} does not matter because Q_2 acts like a voltage source. Consequently there is only one loop to analyze: the v_{E1} discharge loop. The differential equation describing the loop is found from Kirchoff's Voltage Law.

$$v_{E1}(t) := \quad R_E i_C(t) = V_{E(sat)}u(t) + v_C(t) \tag{13}$$

$$R_E\left(-C_E\frac{dv_C(t)}{dt}\right) = V_{E(sat)}u(t) + v_C(t)$$

$$\frac{d}{dt}v_C(t) + \frac{1}{R_E C_E}v_C(t) = \frac{-V_{E(sat)}}{R_E C_E}u(t) \tag{14}$$

The system will be easier to solve in frequency domain. Taking the Laplace transform gives

$$sV_C(s) - v_C(0^-) + \frac{1}{R_E C_E}V_C(s) = \frac{-V_{E(sat)}}{sR_E C_E}$$

$$V_C(s)\left[s^2 + \frac{s}{R_E C_E}\right] = sv_C(0^-) - \frac{V_{E(sat)}}{R_E C_E}$$

$$V_C(s) = \frac{sv_C(0^-) - \frac{V_{E(sat)}}{R_E C_E}}{s(s + \frac{1}{R_E C_E})}$$

$$V_C(s) = [V_{E(sat)} - V_{E(trig)}]\left[\frac{s - \frac{V_{E(sat)}}{R_E C_E(V_{E(sat)} - V_{E(trig)})}}{s(s + \frac{1}{R_E C_E})}\right]$$

$$V_C(s) = C\frac{s - f_1}{s(s + f_0)} \quad \text{where} \begin{cases} C = V_{E(sat)} - V_{E(trig)} \\ f_0 = \frac{1}{R_E C_E} \\ f_1 = f_0\frac{V_{E(sat)}}{C} \end{cases} \tag{15}$$

Before converting back to time domain, a partial fraction expansion must be done.

$$\frac{s - f_1}{s(s + f_0)} = \frac{A}{s} + \frac{B}{s + f_0} = \frac{A(s + f_0) + Bs}{s(s + f_0)}$$

[3]Actually in a perfect world, I would have already graduated.

$$s - f_1 = A(s + f_0) + Bs$$

Polynomial terms of different order are linearly independent, so this equation can be broken into simultaneous equations.

$$\begin{cases} 1 = A + B \\ -f_1 = Af_0 \end{cases}$$

Solving the simultaneous system gives

$$\begin{cases} A = \frac{-f_1}{f_0} = \frac{-V_{E(sat)}}{C} \\ B = 1 - A = 1 + \frac{V_{E(sat)}}{C} \end{cases} \tag{16}$$

and expanded frequency domain equation is

$$V_C(s) = C\left(\frac{A}{s} + \frac{B}{s - f_0}\right) \tag{17}$$

Converting back to time domain gives

$$v_C(t) = CAu(t) + CBe^{-f_0 t}$$

Substituting values for A, B, and C from equations 15 and 16 describes the voltage across the capacitor as a function of time.

$$v_C(t) = -V_{E(sat)} + (2V_{E(sat)} - V_{E(trig)})e^{-t/R_E C_E}$$

Substituting this description of $v_C(t)$ into the right hand side of the equation 13 gives the final solution for discharging voltage at the off emitter.

$$v_{E(off)}(t) = [2V_{E(sat)} - V_{E(trig)}]e^{-t/R_E C_E} \tag{18}$$

The lifetime of this output state is as long as it takes for $v_{E(off)}$ to reach $V_{E(trig)}$.

$$V_{E(trig)} = [2V_{E(sat)} - V_{E(trig)}]e^{-T_{stability}/R_E C_E}$$

$$T_{stability} = R_E C_E ln\left(\frac{2V_{E(sat)} - V_{E(trig)}}{V_{E(trig)}}\right)$$

There are two stable states per period of the square wave, so the frequency of oscillation is

$$f = \frac{1}{2T_{stability}} = \frac{1}{2R_E C_E ln\left(\frac{2V_{E(sat)} - V_{E(trig)}}{V_{E(trig)}}\right)} \tag{19}$$