# Emitter-Coupled Oscillator

Author: Ben Lorenzetti

Project Start Date: February 26, 2015
Report Submission Date: March 23, 2015

# Contents



# 1 Objective

To investigate the design and operation of an emitter-coupled astable multivibrator for 50 MHz operation.

# 2 Principles of Operation

In analog electronics, a sinusoidal oscillator is sometimes needed, such as for power conversion, driving a motor, or for the carrier frequency in radio transmissions. These can be built from an amplifier with a passive feedback network, where the gain $> 1$ and the feedback is positive at the frequency of operation [1]. The only other requirement is that the amplifer operates linearly.

In contrast, digital circuits usually require a square wave clock signal. Ironically, a digital oscillator can be built starting from a basic digital component.

A flip-flop is a digital circuit with two stable states, made from two cross-connected amplifiers. It is a fundamental component in digital logic. In fact, when a master and slave flip-flop are connected in series they form a 1-bit register used in CPUs. Usually, the cross-connection between the two amplifiers is resistive and one amplifier will be driven in saturation while the other is in cutoff. Amplifier in digital circuits are usually driven between saturation and cutoff, making them unlinear, binary (two-state) devices.

DIGITAL FLIP-FLOP AND FLIP FLOP WITH REACTIVE EMITTER COUPLING

If the cross-connection is made to be reactive, then the flip-flop may not be stable in either state. If it oscillates between the two states and produces a near-square wave, it is called a bistable multivibrator. A capacitor is usually used for the cross-connection because it delays the instantaneous voltage change that would normally occur when a transistor switches between saturation and cutoff.

Analog oscillators produce sinusoids; digital oscillators produce square waves. An analog amplifer oscillates if it has reactive feedback that is positive; a digital flip-flop oscillates if it has reactive cross-connection strong enough to switch states. Analog oscillators use an amplifier in a linear range; digital oscillators use drive amplifier to its two limits. An analog oscillator may form unintentionally through parasitic feedback, such as through the Miller capacitance of a BJT. This happens to many frustrated students building amplifiers in Electronics Lab. [2] A digital osciallator may form unintentionally through propagation delay or carry-through logic. This happens to many frustrated students simulating a CPU in Computer Architecture. All of these comparisons between analog and digital oscillators can probably be gleaned from the block, system-level diagrams in figure **??**.

OSCILLATOR BLOCK DIAGRAMS AND CORRESPONDING V-T SIGNALS

The flip-flip circuit shown above was not really indended to oscillate. It can be improved by replacing the emitter resistors with constant current mirrors and adding voltage buffers in the cross-connections to improve charging time of the switching junctions and improve output resistance.

ADVANCED CIRCUIT DIAGRAM

# 3 Theory

## 3.1 Bistable Latch

A digital latch can be built with two cross-connected BJT amplifiers, shown in figure **??**. The amplifiers should be nearly mirror images of one another and the coupling networks should be entirely resistive, shown in figure **??**.

LATCH AND LATCH BLOCK DIAGRAM

The latch is bistable, meaning it has two self-sustaining states. Either Q1 is saturated while Q2 is cutoff, or Q1 is cutoff while Q2 is saturated. The circuit is a symmetric loop, so it is not clear where to begin any analysis. Instead of starting at a particular node and time, we will start with some sanity assumptions and determining the conditions that make them true.

First, we assume that the switching transistors are always driven at saturation or cutoff, and that the saturation/cutoff transistors will not switch except due to external triggers. Most of the following analysis will be spent making this assumption true.

[1] the Barkhausen Criterion

[2] see my last lab

Second, we assume that the current diverted through the cross-connections is negligible relative to the on transistor's saturation current.

$$I_{Bias} << I_{C(sat)}$$

Third, we assume that the base current of the on transistor is negligible relative to the current through its biasing network. [3]

$$I_B(sat) << I_{Bias}$$

The second and third criteria compete with each other because the base and collector currents are related by the forward current amplification ratio, $\beta$. The best way to satisfy both conditions is with the square root of $\beta$.

$$I_{Bias} = \frac{I_{C(sat)}}{\sqrt{\beta}} \tag{1}$$

These three assumptions allow us to analyze half of the circuit in isolation, which is shown in figure **??**.

The output voltage has two states, depending on whether the transistor is the one in saturation or in cutoff.

$$V_o = \begin{cases} V_{CC} & : \text{cutoff} \\ V_{CC} - I_{C(sat)}R_C & : \text{saturation} \end{cases} \tag{2}$$

With the assumption that the other transistor has the opposite state, then the input from the cross-connection has the opposite value of $V_o$, and is stable. The bias network is a voltage divider if the base current is negligible, so the base voltage is

$$V_B = \frac{R_2}{R_1 + R_2}(V_o^{'} - V_{EE}) + V_{EE}$$

It is helpful to break this into a piecewise function corresponding to the states in equation 2.

$$V_B = \begin{cases} \frac{R_2}{R_1+R_2}(V_{CC} - I_{C(sat)}R_C - V_{EE}) + V_{EE} & : \text{cutoff} \\ \frac{R_2}{R_1+R_2}(V_{CC} - V_{EE}) + V_{EE} & : \text{saturation} \end{cases} \tag{3}$$

If the transistor is cutoff, there is no emitter current, and the emitter voltage lies at $V_{EE}$. For this to be true, the base-emitter junctions must be biased less than $V_{BE(on)}$. If the transistor is on, the base-emitter junction will be $V_{BE(on)}$, and the saturation current will be determined by the emitter resistance.

$$\begin{cases} V_B < V_{EE} + V_{BE(on)} & : \text{cutoff} \\ V_B = V_{EE} + V_{BE(on)} + I_{C(sat)}R_E & : \text{saturation} \end{cases} \tag{4}$$

Combining equations 3 and 4 gives two independent conditions without a base voltage term.

$$\begin{cases} \frac{R_2}{R_1+R_2} < \frac{V_{BE(on)}}{V_{CC} - I_{C(sat)}R_C - V_{EE}} & : \text{cutoff} \\ \frac{R_2}{R_1+R_2} = \frac{V_{BE(on)} + I_{C(sat)}R_E}{V_{CC} - V_{EE}} & : \text{saturation} \end{cases} \tag{5}$$

In addition two these two conditions for stability of the latch, the summation $R_1 + R_2$ can be found from the bias current design decision. Solving Ohm's law with the collector voltage and $I_{bias}$ from equation 1 gives

$$R_1 + R_2 = \frac{\sqrt{\beta}(V_{CC} - I_{C(sat)}R_C - V_{EE})}{I_{C(sat)}} \tag{6}$$

## 3.2 Astable Multivibrator

[3] the stiff base bias condition