Phase Locked Loop

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Contents

1 Objective

To measure the characteristics of a phase locked loop and to investigate and model its behavior in an FSK (frequency-shift keying) demodulator.

2 Principles of Operation

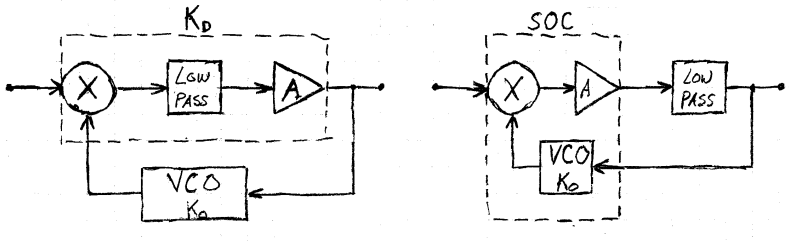

Figure 1: PLL Demodulator Block Diagram (left); Rearrangement for SOC Integration (right).

3 Theory

3.1 Texas Instruments LM656

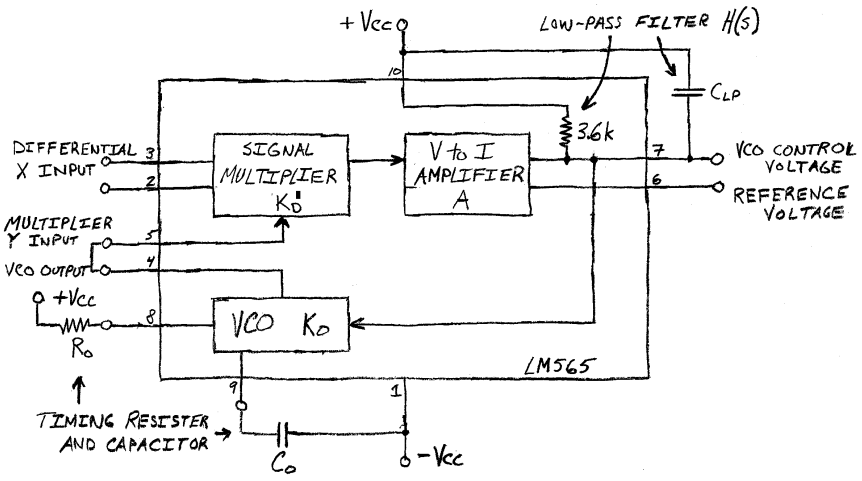

Figure 2: Rough Block Diagram for the LM565 Phase Locked Loop

As discussed in the section 2, most of a PLL demodulator can be integrated onto a single silicon wafer–called a system-on-a-chip (SOC). The only parts that cannot be fabricated on silicon are the capacitors, so the PLL demodulator has been redesigned with this in mind. A company called Signetics was the first to put a PLL on an SOC, but they are out of business so we have a similar chip from Texas Instruments, the LM565.

The LM565 makes it easy for the circuit designer to incorporate frequency-shift keying into their product; you just have to slap on a few capacitors to have a working demodulator. The only design that must be done is selecting a free-running frequency f_0 near the transmission frequency and building a low-pass filter with bandwidth greater than the frequency shift but less than twice the transmission frequency. Use the following equation from the LM565 datasheet to select f_0.

$$f_0 = \frac{0.3}{R_0 C_0} \tag{1}$$

For more information about how the LM565 works, see the schematic diagram in section 7.1.

3.2 Voltage Controlled Oscillator

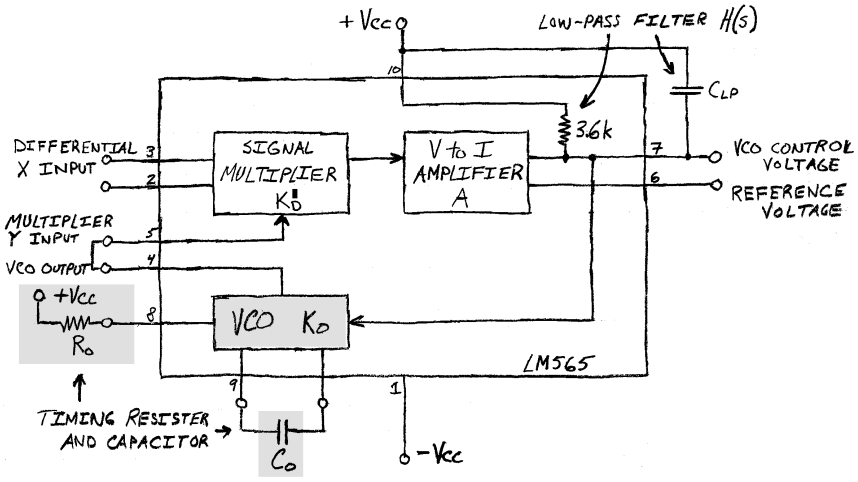

Figure 3: Role of the Voltage Controlled Oscillator in the LM565 PLL

3.3 Signal Multiplier

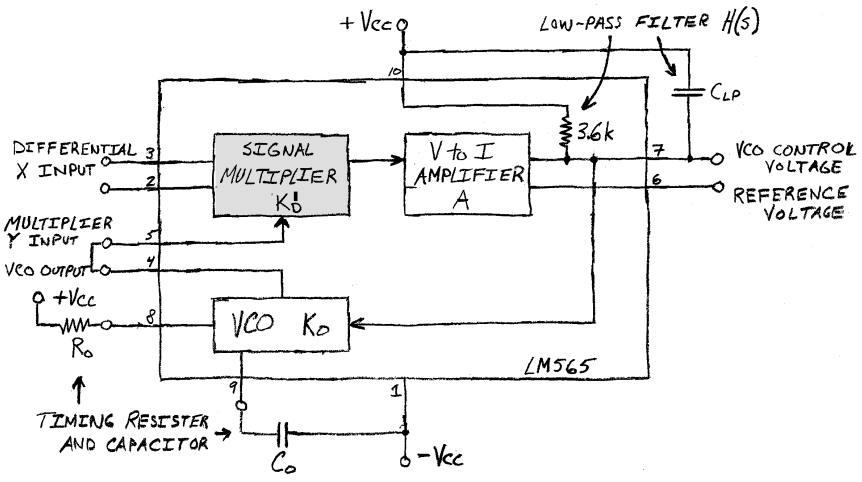

Figure 4: Role of the Multiplier/Mixer/Phase Detector in the LM565 PLL

Addition and subtraction are easy in electronics; just use a shunt or series connection, depending on whether you are summing current or voltage. Multiplication is more difficult; there is no obvious way to mix two signals.

A first though for inplementing a multiplier is to look at the problem in frequency domain and see if that offers any insight. The fourier transform of multiplication is

$$x(t)y(t) \Longleftrightarrow X(s) * Y(s)$$

This is not very helpful because thinking about designing a frequency convolution device is even worse than a signal multiplier. However, there is another mathmatics formula that can give us an implementation idea: the addition propery of logarithms.

$$ln(x) + ln(y) = ln(x \times y) \tag{2}$$

3.4 Transconductance Amplifier

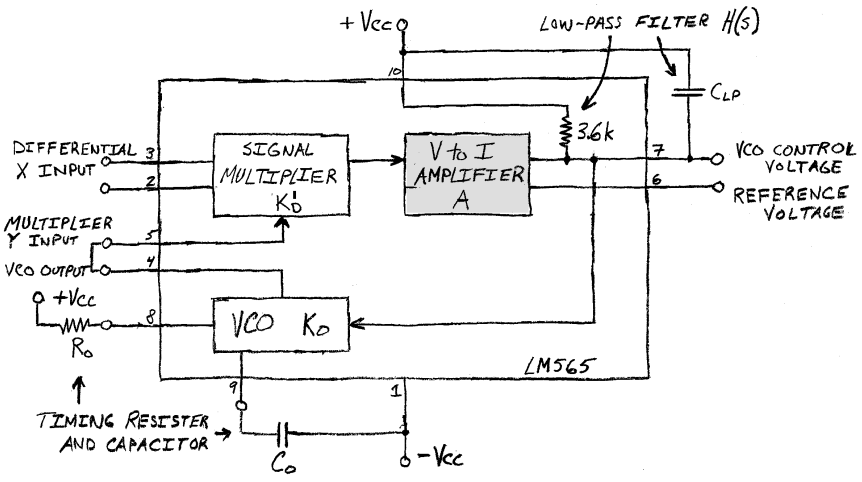

Figure 5: Role of the Transconductance Amplifier in the LM565 PLL

In the circuit schematic for the LM565, the amplifier accepts a voltage from the multiplier and outputs an amplified current signal. Unlike the original Signetics chip, the low pass filter following the amplifier uses current as the input (R and C are parallel). A voltage-to-current amplifier is called a transconductance amplifier.

We are doing feedback in the lecture right now, so I decided to implement this module with an opamp and resistive feedback. Figure 6 shows the block diagram for a feedback amplifier, with an op-amp in the amplifier position. Note that an op-amp is usually depicted as a voltage-to-voltage amplifier.

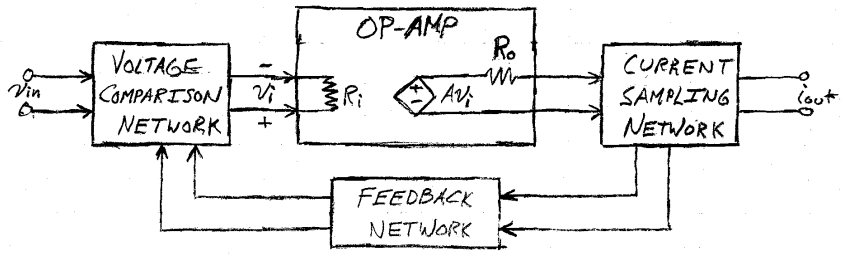

Figure 6: Generic Block Diagram of an Op-Amp Feedback Amplifier

We can replace the voltage source in the op-amp with its norton equivalent current source. Voltage comparison and current sampling are both accomplished with series connections. Figure 7 shows these changes, which now depict a transconductance amplifier.

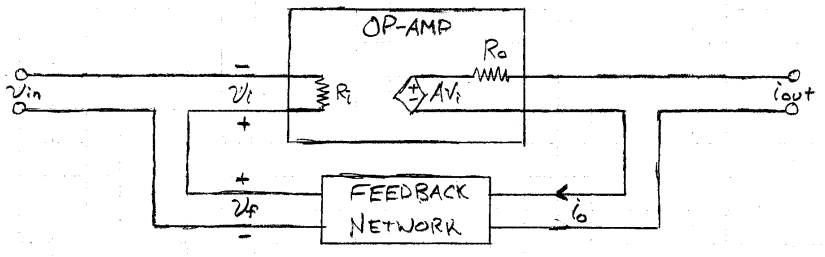

Figure 7: Transconductance Feedback Amplifier Block Diagram

I tried several feedback networks and eventually settled on one with three resistors; see figure 8.

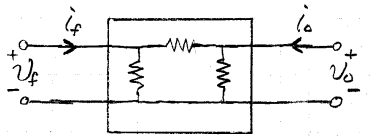

Figure 8: Resistive Feedback Network

To choose sensible resistors, it is helpful to analyze the feedback network with the h-parameter model. The dependent sources in the h-parameter model should be comparison and sampling signals, so the matrix should be

$$\begin{bmatrix} v_f \\ i_o \end{bmatrix} = \begin{bmatrix} h_{11} & h_{12} \\ h_{21} & h_{22} \end{bmatrix} \begin{bmatrix} i_f \\ v_o \end{bmatrix}$$

The h-parameters come out to be

$$\begin{bmatrix} h_{11} & h_{12} \\ h_{21} & h_{22} \end{bmatrix} = \begin{bmatrix} \frac{R_2 R_3}{R_2+R_3} & h_{12} = \frac{R_3}{R_2+R_3} \\ \frac{R_2}{R_2+R_3} & \frac{R_1+R_2+R_3}{R_1(R_2+R_3)} \end{bmatrix}$$

and they correspond to the h-parameter equivalent circuit shown in figure 9.

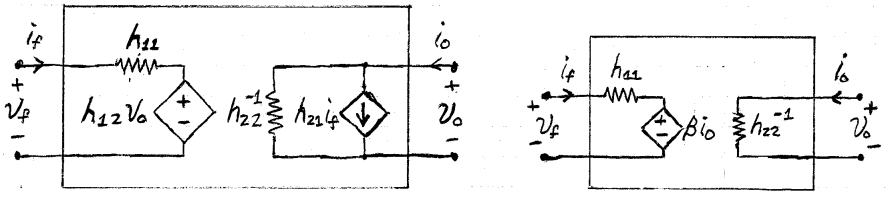

Figure 9: Full h-Parameter Circuit (left) and its Unilateral Approximation (right)

An optimal feedback network is unilateral, so h_{21} must be designed to be negligibly small.

$$h_{21} = \frac{R_2}{R_2 + R_3} \tag{3}$$

The other value that must be designed is the ratio of the feedback output to the sampled value.

$$\beta = \frac{v_f}{i_o} = h_{12} * h_{22}^{-1} = \frac{R_3}{R_2 + R_3} * \frac{R_1(R_2 + R_3)}{R_1 + (R_2 + R_3)} \tag{4}$$

From equation 3, it is clear that $R_2 << R_3$ if we are to neglect the h_{21} crosstalk. This design decision also allows us to simplify equation 4.

$$\beta = 1 * \frac{R_1 R_3}{R_1 + R_3}$$

If we also design $R_1 << R_3$, then the feedback ratio is simply

$$\beta = R_1$$

The return ratio for the feedback amplifier is given by

$$G_{fb} = \frac{G}{1 - \beta G}$$

Because the open circuit gain of an op-amp is so large, the return ratio simplifies to

$$G_{fb} = \frac{-1}{\beta} = \frac{1}{R_1} \tag{5}$$

which is the amplifier gain for the circuit topology shown in figure 10.

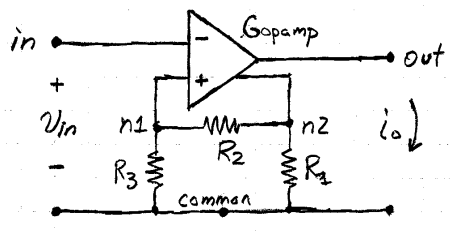

Figure 10: Transconductance Amplifier Module

3.5 Low-Pass Filter

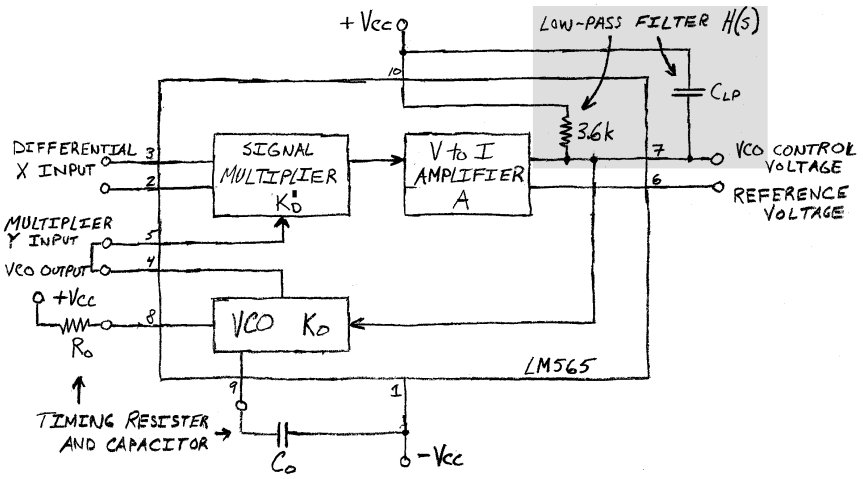

Figure 11: Role of the Low Pass Filter in the LM565 PLL

4 Design and Simulation

4.1 Voltage Controlled Oscillator

4.1.1 LM565 vs SPICE Model

For the timing resistor R_0, I decided to use $3k\Omega$ because it was available with 1% tolerance. Using equation 1, the timing capacitors for 1 kHz, 10 kHz, and 100 kHz operating ranges should be

$$R_0 = 3k\Omega$$

$$C_{0(1kHz)} = 0.1uF \quad | \quad C_{0(10kHz)} = 0.01uF \quad | \quad C_{0(100kHz)} = 1,000pF$$

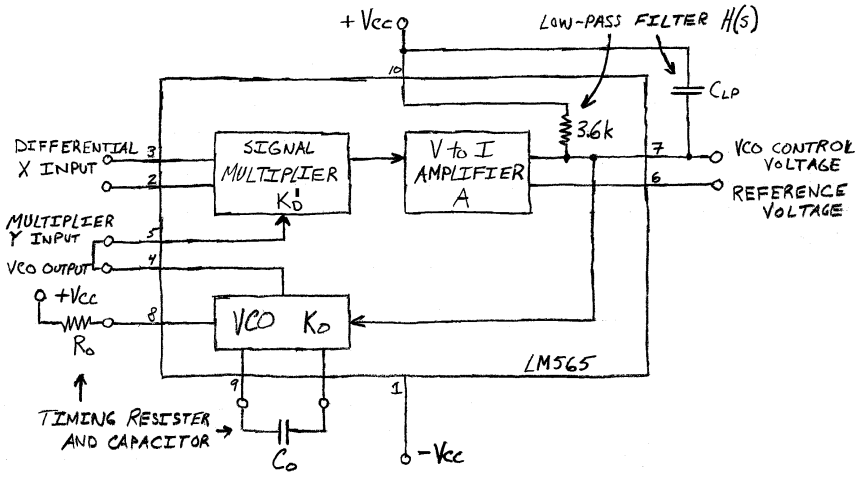

Figure 12: Block Diagram for Phase Locked Loop SPICE Model

4.1.2 Free Running Frequency, f_0

4.1.3 Oscillator Sensitivity, K_O

4.2 Signal Multiplier

4.3 Transconductance Amplifier

4.4 Low-Pass Filter

4.5 Phase Detector Sensitivity, K_D

4.6 PLL Loop Gain, $K_O K_D$

4.7 FSK Generator

4.8 FSK Demodulator

5 Results

5.1 Free Running Frequency, f_0

5.2 Oscillator Sensitivity, K_O

5.3 FSK Demodulator

6 Conclusions

7 Appendices

7.1 LM565 Schematic Diagram

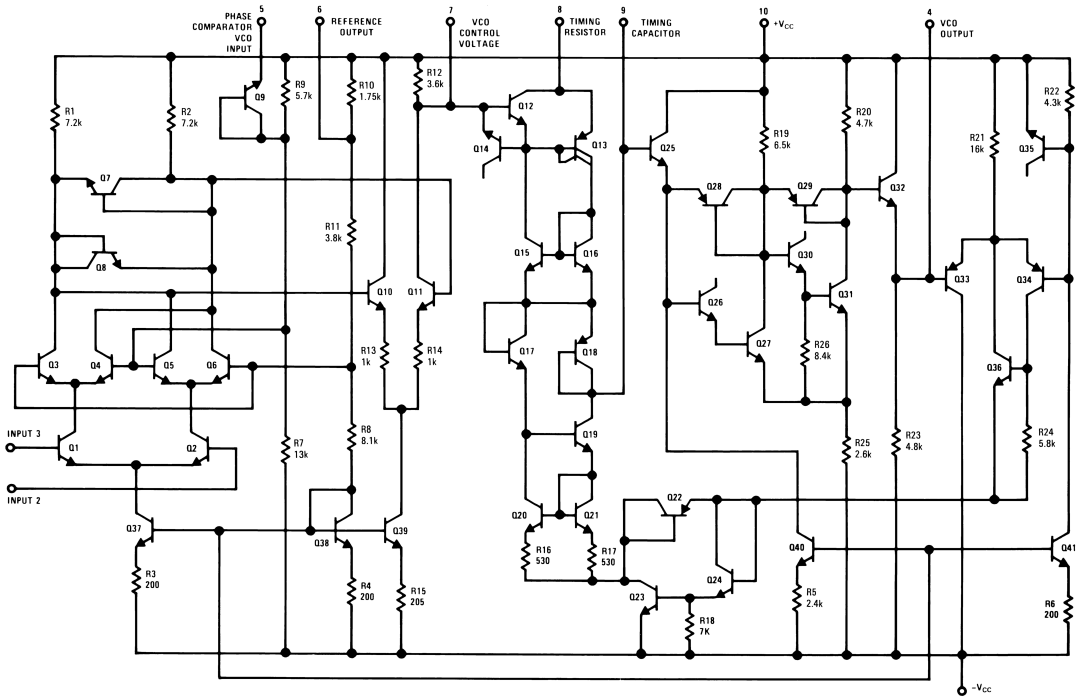

Figure 13: LM565 Schematic Diagram; taken from page 6 of the TI datasheet