Phase Locked Loop

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Contents

1 Objective

To measure the characteristics of a phase locked loop and to investigate and model its behavior in an FSK (frequency-shift keying) demodulator.

2 Principles of Operation

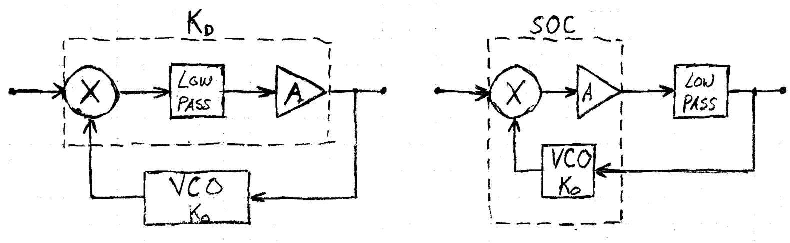

Figure 1: PLL Demodulator Block Diagram (left); Rearrangement for SOC Integration (right).

3 Theory

3.1 Texas Instruments LM656

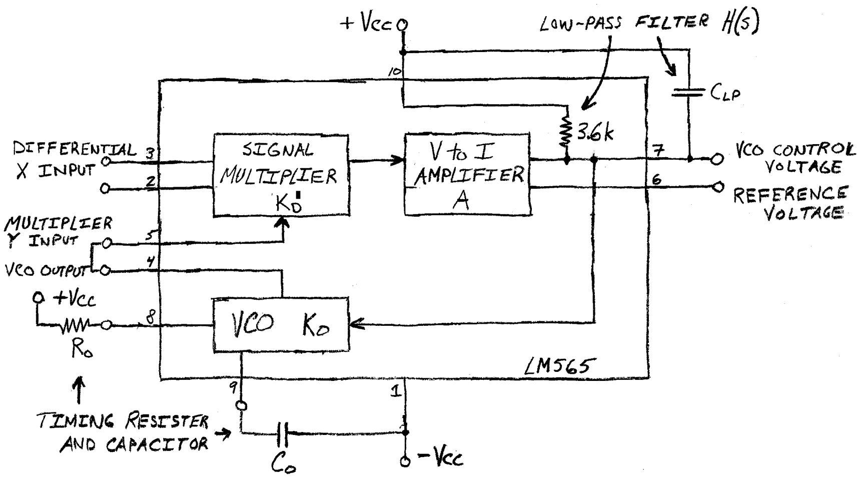

Figure 2: Rough Block Diagram for the LM565 Phase Locked Loop

As discussed in the section 2, most of a PLL demodulator can be integrated onto a single silicon wafer–called a system-on-a-chip (SOC). The only parts that cannot be fabricated on silicon are the capacitors, so the PLL demodulator has been redesigned with this in mind. A company called Signetics was the first to put a PLL on an SOC, but they are out of business so we have a similar chip from Texas Instruments, the LM565.

The LM565 makes it easy for the circuit designer to incorporate frequency-shift keying into their product; you just have to slap on a few capacitors to have a working demodulator. The only design that must be done is selecting a free-running frequency f_0 near the transmission frequency and building a low-pass filter with bandwidth greater than the frequency shift but less than twice the transmission frequency. Use the following equation from the LM565 datasheet to select f_0.

$$f_0 = \frac{0.3}{R_0 C_0} \tag{1}$$

For more information about how the LM565 works, see the schematic diagram in section 7.1.

3.2 Voltage Controlled Oscillator

3.3 Signal Multiplier

3.4 Frequency Independent Amplifier

3.5 Low-Pass Filter

4 Design and Simulation

4.1 Voltage Controlled Oscillator

4.1.1 LM565 vs SPICE Model

For the timing resistor R_0, I decided to use $3k\Omega$ because it was available with 1% tolerance. Using equation 1, the timing capacitors for 1 kHz, 10 kHz, and 100 kHz operating ranges should be

$$R_0 = 3k\Omega$$

$$C_{0(1kHz)} = 0.1uF \quad | \quad C_{0(10kHz)} = 0.01uF \quad | \quad C_{0(100kHz)} = 1,000pF$$

4.1.2 Free Running Frequency f_0

4.1.3 Oscillator Sensitivity K_O

4.2 Signal Multiplier

4.3 Frequency Independent Amplifier

4.4 Low-Pass Filter

4.5 Phase Detector Sensitivity K_D

4.6 Loop Gain $K_O K_D$

5 Results

5.1 Free Running Frequency f_0

5.2 Oscillator Sensitivity K_O

5.3 FSK Demodulator

6 Conclusions

7 Appendices

7.1 LM565 Schematic Diagram

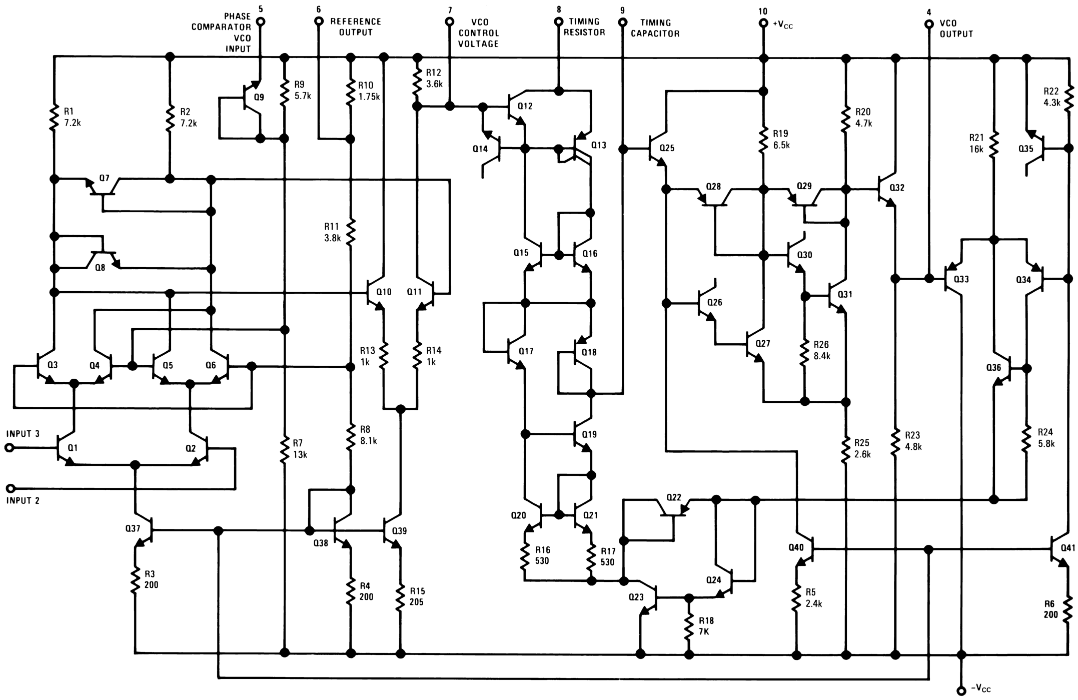

Figure 3: LM565 Schematic Diagram; taken from page 6 of the TI datasheet