ADC Clock Period (TAD) **Device Frequency (Fosc) ADC Clock Source** ADCS<1:0> 20 MHz 8 MHz 4 MHz 1 MHz

100 ns⁽²⁾

400 ns⁽²⁾

 $1.6 \mu s$

0.0

01

10

ADC CLOCK PERIOD (TAD) Vs. DEVICE OPERATING FREQUENCIES (VDD ≥ 3.0V)

250 ns⁽²⁾

1.0 μs⁽²⁾

 $4.0 \mu s$

500 ns⁽²⁾

 $2.0 \mu s$

 $8.0 \, \mu s^{(3)}$

2.0 us

8.0 μs⁽³⁾

32.0 us⁽³⁾

FRC		11	2-6 μs ^(1,4)	2-6 μs ^(1,4)	2-6 μs ^(1,4)	2-6 μs ^(1,4)
Legend:	Shaded cells are outside of recommended range.					
Note 1:	The FRC source has a typical TAD time of 4 μ s for VDD > 3.0V.					
2:	These values violate the minimum required TAD time.					
3:	For faster conversion times, the selection of another clock source is recommended.					
4:	When the device frequency is greater than 1 MHz, the FRC clock source is only recommended if the conversion will be performed during Sleep.					

TABLE 9-1:

Fosc/2

Fosc/8

Fosc/32

FIGURE 9-2:

TCY to TAD TAD1 TAD2 TAD3 TAD4 TAD5 TAD6 TAD7 TAD8 TAD9 TAD10 TAD11 b9 b8 b7 b6 b5 b4 b3 b2 b1 b0 Conversion Starts

ANALOG-TO-DIGITAL CONVERSION TAD CYCLES

Holding Capacitor is Disconnected from Analog Input (typically 100 ns) Set GO/DONE bit GO bit is cleared. ADIF bit is set.

ADRESH and ADRESL registers are loaded. Holding capacitor is connected to analog input