TABLE 9-1: ADC CLOCK PERIOD (T_{AD}) VS. DEVICE OPERATING FREQUENCIES ($V_{DD} \geq 3.0V$)

ADC Clock Period (T_{AD})		Device Frequency (F_{OSC})			
ADC Clock Source	**ADCS<1:0>**	**20 MHz**	**8 MHz**	**4 MHz**	**1 MHz**
$F_{OSC}/2$	00	100 ns(2)	250 ns(2)	500 ns(2)	2.0 µs
$F_{OSC}/8$	01	400 ns(2)	1.0 µs(2)	2.0 µs	8.0 µs(3)
$F_{OSC}/32$	10	1.6 µs	4.0 µs	8.0 µs(3)	32.0 µs(3)
F_{RC}	11	2-6 µs(1,4)	2-6 µs(1,4)	2-6 µs(1,4)	2-6 µs(1,4)

Legend: Shaded cells are outside of recommended range.

Note 1: The F_{RC} source has a typical T_{AD} time of 4 µs for V_{DD} > 3.0V.

2: These values violate the minimum required T_{AD} time.

3: For faster conversion times, the selection of another clock source is recommended.

4: When the device frequency is greater than 1 MHz, the F_{RC} clock source is only recommended if the conversion will be performed during Sleep.

FIGURE 9-2: ANALOG-TO-DIGITAL CONVERSION T_{AD} CYCLES