14.2.3.2 State diagram timers

All timers operate in the same fashion. A timer is reset and starts counting upon entering a state where "start x_timer" is asserted. Time "x" after the timer has been started, "x_timer_done" is asserted and remains asserted until the timer is reset. At all other times, "x_timer_not_done" is asserted.

When entering a state where "start x_timer" is asserted, the timer is reset and restarted even if the entered state is the same as the exited state; for example, when in the Link Test Pass state of the Link Integrity Test function state diagram, the "link_loss_timer" and the "link_test_min_timer" are reset each time the term "RD = active + (link_test_rcv=true * link_test_min_timer_done)" is satisfied.

link_loss_timer. Timer for longest time input activity can be missing before the MAU determines that a link fail condition exists (14.2.1.7).

link_test_min_timer. Timer for the minimum time between valid link test pulses (14.2.1.7).

link_test_max_timer. Timer for maximum time input activity can be missing before Link Test Fail state is exited (14.2.1.7).

SQE_test_timer. Timer for the duration of the CS0 signal used for the SQE Test function (14.2.1.5).

SQE_test_wait_timer. Timer for the delay from end of packet to the start of the CS0 signal used for the SQE Test function (14.2.1.5).

unjab_timer. Timer for the length of time the DO circuit must be continuously idle to allow transmission to be re-enabled (14.2.1.6).

xmit_max_timer. Timer for excessively long transmit time (14.2.1.6).

14.3 MAU electrical specifications

This subclause defines the electrical characteristics of the MAU at the MDI and the AUI. The MAU shall also meet the AUI requirements specified in Clause 7 when the AUI is implemented.

Additional information relative to conformance testing is given in B.4.3.

The ground for all common-mode tests is circuit PG, Protective Ground of the AUI. In implementations without an AUI, chassis ground is used as circuit PG. All components in test circuits shall be ±1% unless otherwise stated.

14.3.1 MAU-to-MDI interface characteristics

14.3.1.1 Isolation requirement

A MAU with a MDI that is a PI (see 33.1.3) shall meet the isolation requirements defined in 33.4.1.

A MAU with a MDI that is not a PI shall provide isolation between the DTE Physical Layer circuits including frame ground and all MDI leads including those not used by 10BASE-T.

This electrical isolation shall withstand at least one of the following electrical strength tests.

a) 1500 V rms at 50 Hz to 60 Hz for 60 s, applied as specified in subclause 5.2.2 of IEC 60950-1:2001.
b) 2250 V dc for 60 s, applied as specified in subclause 5.2.2 of IEC 60950-1:2001.

c) A sequence of ten 2400 V impulses of alternating polarity, applied at intervals of not less than 1 s. The shape of the impulses shall be 1.2/50 μs (1.2 μs virtual front time, 50 μs virtual time of half value), as defined in IEC 60950-1:2001 Annex N.

There shall be no insulation breakdown, as defined in subclause 5.2.2 of IEC 60950-1:2001, during the test. The resistance after the test shall be at least 2 MΩ, measured at 500 V dc.

14.3.1.2 Transmitter specifications

The MAU shall provide the Transmit function specified in 14.2.1.1 in accordance with the electrical specifications of this subclause.

Where a load is not specified, the transmitter shall meet requirements of this subclause when connected to a 100 Ω resistive load. The use of 100 Ω terminations simplifies the measurement process when using 50 Ω measurement equipment as 50 Ω to 100 Ω impedance matching transformers are readily available.

Some tests in this subclause require the use of an equivalent circuit that models the distortion introduced by a simplex link segment. This twisted-pair model shall be constructed according to Figure 14–7 or a type 10BASE-T MAU that is not a type 10BASE-Te MAU and according to Figure 14–8 for a type 10BASE-Te MAU with component tolerances as follows: Resistors, ±1%; capacitors, ±5%; inductors, ±10%. Component tolerance specifications shall be met from 5.0 MHz to 15 MHz. For all measurements, the TD circuit shall be connected through a balun to section 1 and the signal measured across a load connected to section 4 of the model. The balun shall not affect the peak differential output voltage specified in 14.3.1.2.1 by more than 1% when inserted between the 100 Ω resistive load and the TD circuit. Also, the value of the resistor that is in series with the inductors includes the series resistance of the inductor itself. The actual value of the resistor that is used is computed by subtracting the series resistance of the inductor from the resistor value shown in the figure.

For a type 10BASE-T MAU that is not a type 10BASE-Te MAU, the insertion loss of the twisted-pair model when measured with a 100 Ω source and 100 Ω load shall be between 9.70 dB and 10.45 dB at 10 MHz, and between 6.50 dB and 7.05 dB at 5 MHz.

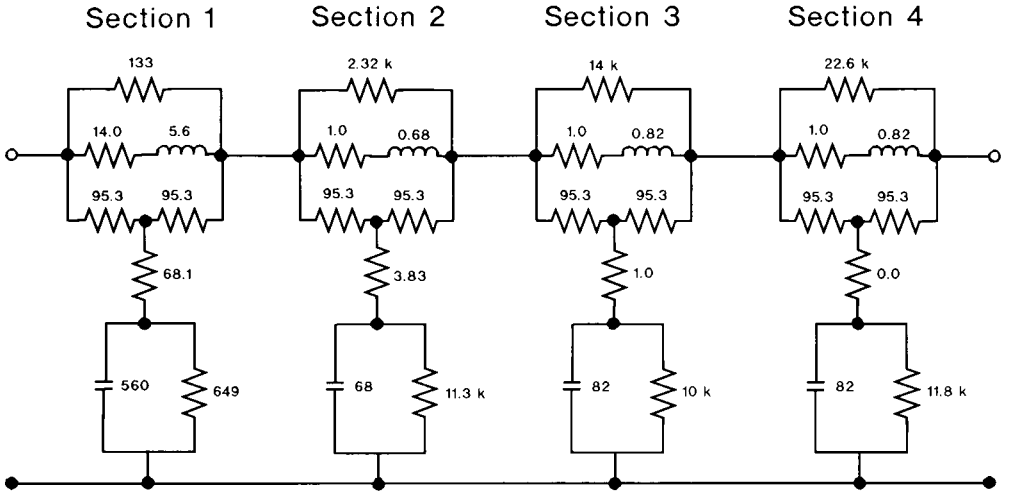


Figure 14–7—Twisted-pair model for 10BASE-T

For a type 10BASE-Te MAU, the insertion loss of the twisted-pair model when measured with a 100 Ω source and 100 Ω load shall be between 6.8 dB and 7.4 dB at 10 MHz, and between 4.75 dB and 5.25 dB at 5 MHz.

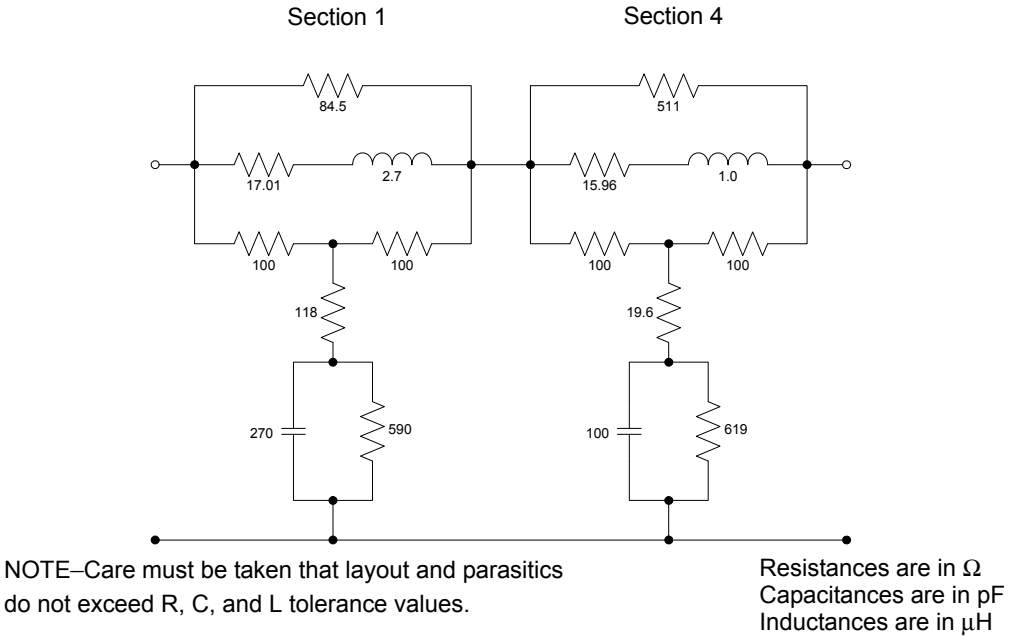


Figure 14–8—Twisted-pair model for 10BASE-Te

14.3.1.2.1 Differential output voltage

Some of the text and figures of this subclause describe the differential voltage in terms of magnitudes. These requirements apply to negative as well as positive pulses.

The peak differential voltage on the TD circuit when terminated with a 100 Ω resistive load shall be between 2.2 V and 2.8 V for all data sequences for a type 10BASE-T MAU that is not a type 10BASE-Te MAU. For a type 10BASE-Te MAU, the peak differential voltage on the TD circuit when terminated with a 100 Ω resistive load shall be between 1.54 V and 1.96 V for all data sequences. When the DO circuit is driven by an all-ones Manchester-encoded signal, any harmonic measured on the TD circuit shall be at least 27 dB below the fundamental.

NOTE—The specification on maximum spectral components is not intended to ensure compliance with regulations concerning RF emissions. The implementor should consider any applicable local, national, or international regulations. Additional filtering of spectral components may therefore be necessary.

The output signal V_o is defined at the output of the twisted-pair model as shown in Figure 14–9. The specific twisted-pair model used in Figure 14–9 shall be the equivalent circuit shown in Figure 14–7 for 10BASE-T except 10BASE-Te and shall be the equivalent circuit shown in Figure 14–8 for 10BASE-Te. The TD transmitter shall provide equalization such that the output waveform shall fall within the template shown in Figure 14–10 for all data sequences. Voltage and time coordinates for inflection points on Figure 14–10 are given in Table 14–1. (Zero crossing points are different for external and internal MAUs. The zero crossings depicted in Figure 14–10 apply to an external MAU.) The template voltage may be scaled by a factor of 0.9 to 1.1 but any scaling below 0.9 or above 1.1 shall not be allowed. The recommended measurement procedure is described in B.4.3.1. Time t = 0 on the template represents a zero crossing, with positive slope, of the output waveform. During this test the twisted-pair model shall be terminated in 100 Ω and driven by a

transmitter with a Manchester-encoded pseudo-random sequence with a minimum repetition period of 511

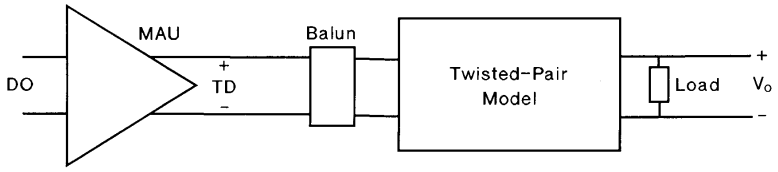


Figure 14–9—Differential output voltage test

bits.

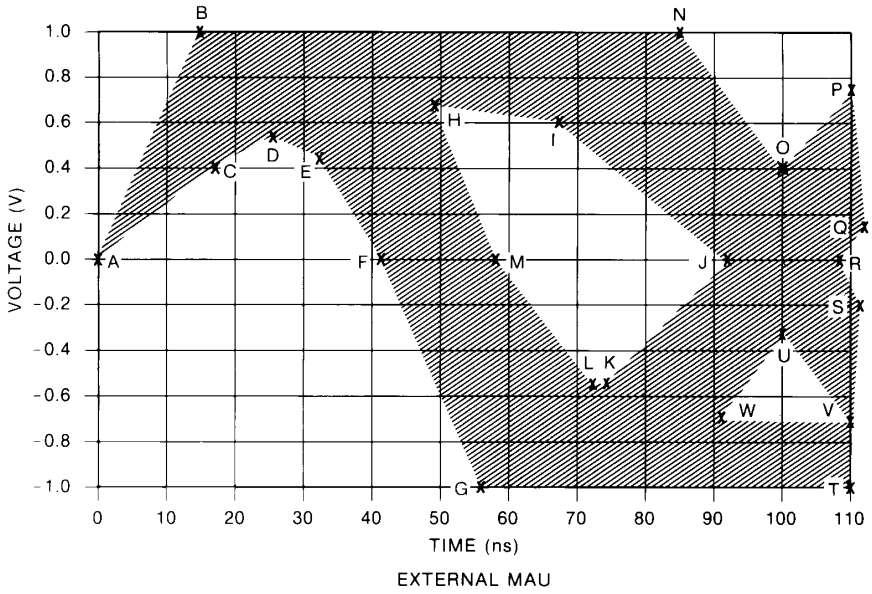


Figure 14–10—Voltage template

Table 14–1—Voltage template values for Figure 14–10

Reference	Time (ns)		Voltage (V)
	External MAU	Internal MAU	
A	0	0	0
B	15	15	1.0
C	15	15	0.4
D	25	25	0.55
E	32	32	0.45
F	42	39	0
G	57	57	–1.0
H	48	48	0.7
I	67	67	0.6
J	92	89	0
K	74	74	–0.55
L	73	73	–0.55
M	58	61	0
N	85	85	1.0
O	100	100	0.4
P	110	110	0.75
Q	111	111	0.15
R	108	111	0
S	111	111	–0.15
T	110	110	–1.0
U	100	100	–0.3

Table 14–1—Voltage template values for Figure 14–10 *(continued)*

Reference	Time (ns)		Voltage (V)
	External MAU	Internal MAU	
V	110	110	–0.7
W	90	90	–0.7

This test shall be repeated with the template inverted about the time axis. In that case, t = 0 on the template represents a zero crossing, with negative slope, of the output waveform. When testing an external MAU the input waveform to the DO circuit of the MAU shall contribute no more than 0.5 ns of jitter. Adherence to this template does not verify that the requirements of 14.3.1.2.3 are met. (See B.4.3.3 for modification of the template to test jitter.)

The TP_IDL shall always start with a positive waveform when a waveform conforming to Figure 7–12 is applied to the DO circuit. If the last bit transmitted was a CD1, the last transition will be at the bit cell center of the CD1. If the last bit transmitted was a CD0, the PLS will generate an additional transition at the bit cell boundary following the CD0. After the zero crossing of the last transition, the differential voltage shall remain within the shaded area of Figure 14–11. Once the differential voltage has gone more negative than –50 mV, it shall not exceed +50 mV. The template requirements of Figure 14–11 shall be met when measured across each of the test loads defined in Figure 14–12, both with the load connected directly to the TD circuit and with the load connected through the twisted-pair model as defined in Figure 14–7 and Figure 14–9 for 10BASE-T except 10BASE-Te, and Figure 14–8 and Figure 14–9 for 10BASE-Te.

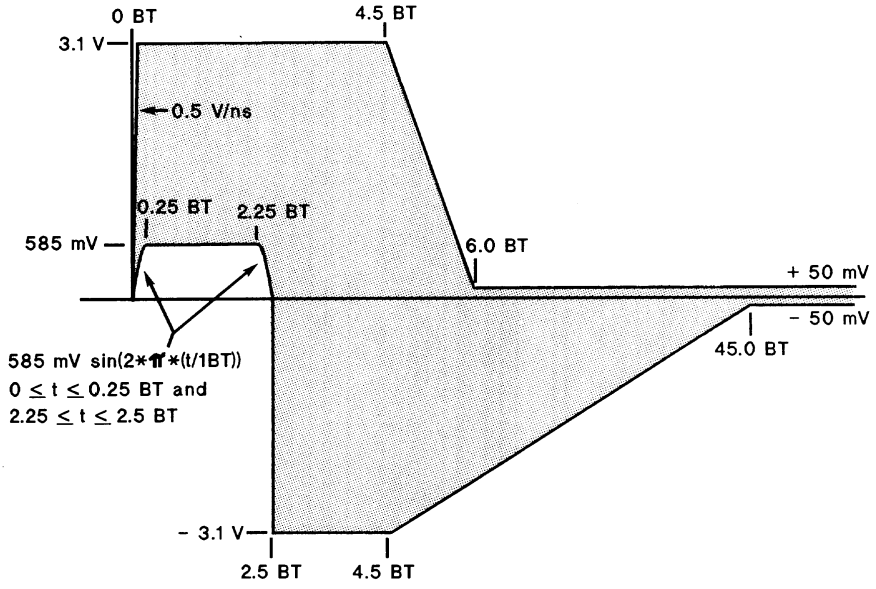
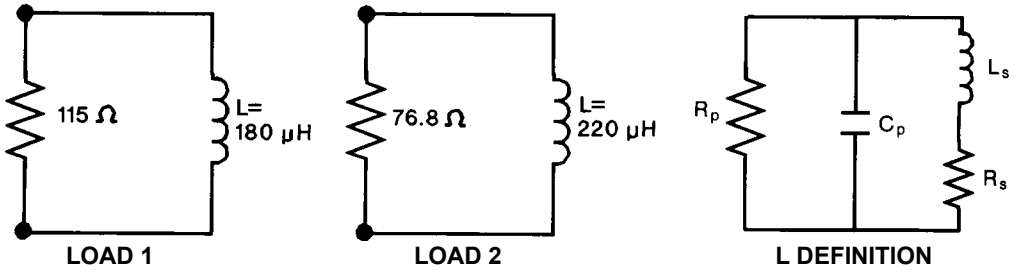


Figure 14–11—Transmitter waveform for start of TP_IDL

The link test pulse shall be a single positive (TD+ lead positive with respect to TD– lead) pulse, which falls within the shaded area of Figure 14–13. Once the differential output voltage has become more negative than –50 mV, it shall remain less than +50 mV. The template requirements of Figure 14–13 shall be met when measured across each of the test loads defined in Figure 14–12; both with the load connected directly to the TD circuit and with the load connected through the twisted-pair model as defined in Figure 14–7 and Figure 14–9 for 10BASE-T except 10BASE-Te, and Figure 14–8 and Figure 14–9 for 10BASE-Te.

For a MAU that implements the Auto-Negotiation algorithm defined in Clause 28, the FLP Burst Sequence will consist of multiple link test pulses. All link test pulses in the FLP Burst sequence shall meet the



All parameters are defined over the frequency range of 250 kHz to 6 MHz.

$L_s = L \pm 1\%$ $R_p \geq 2\ k\Omega$
$C_p = 12\ pF \pm 20\%$ $R_s \leq 0.5\ \Omega$

Figure 14–12—Start-of-TP_IDL test load

template requirements of Figure 14–13 when measured across each of the test loads defined in Figure 14–12; both with the load connected directly to the TD circuit and with the load connected through the twisted-pair model as defined in Figure 14–7 and Figure 14–9 for 10BASE-T except 10BASE-Te, and Figure 14–8 and Figure 14–9 for 10BASE-Te.

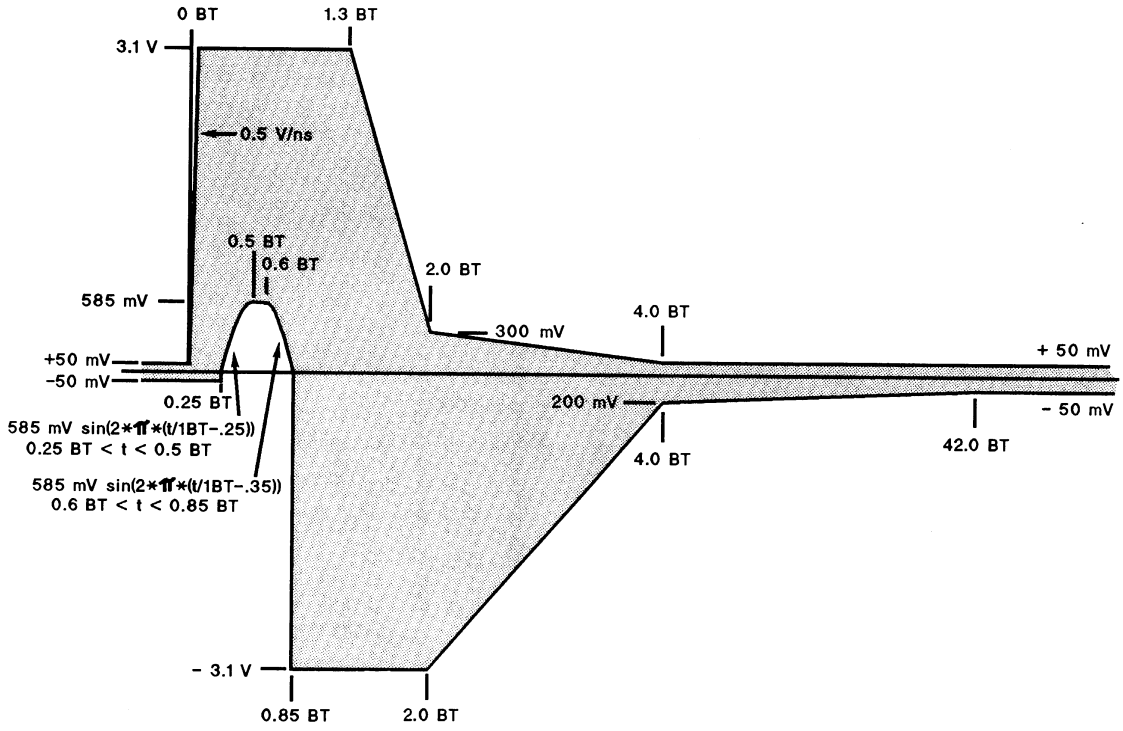


Figure 14–13—Transmitter waveform for link test pulse

14.3.1.2.2 Transmitter differential output impedance

The differential output impedance as measured on the TD circuit shall be such that any reflection, due to differential signals incident upon the TD circuit from a simplex link segment having any impedance within the range specified in 14.4.2.2, shall be at least 15 dB below the incident, over the frequency range of

5.0 MHz to 10 MHz. This return loss shall be maintained at all times when the MAU is powered, including when the TD circuit is sending TP_IDL.

14.3.1.2.3 Output timing jitter

The transmitter output jitter is measured at the output of the twisted-pair model terminated in a 100 Ω load, as shown in Figure 14–9. The jitter added to the signal on the DO circuit as it propagates through the MAU and the twisted-pair model shall be no more than ±3.5 ns. Additionally, the MAU shall add no more than ±8 ns of jitter to the signal received on the DO circuit when the TD circuit is directly driving a 100 Ω resistive load.

14.3.1.2.4 Transmitter impedance balance

The common-mode to differential-mode impedance balance of the TD circuit shall exceed $29-17\log_{10}(f/10)$ dB (where f is the frequency in MHz) over the frequency range 1.0 MHz to 20 MHz. This balance is defined as $20\log_{10}(E_{cm}/E_{dif})$, where E_{cm} is an externally applied sine wave voltage as shown in Figure 14–14.

NOTE—The balance of the test equipment (such as the matching of the 147 Ω resistors) must exceed that required of the transmitter.

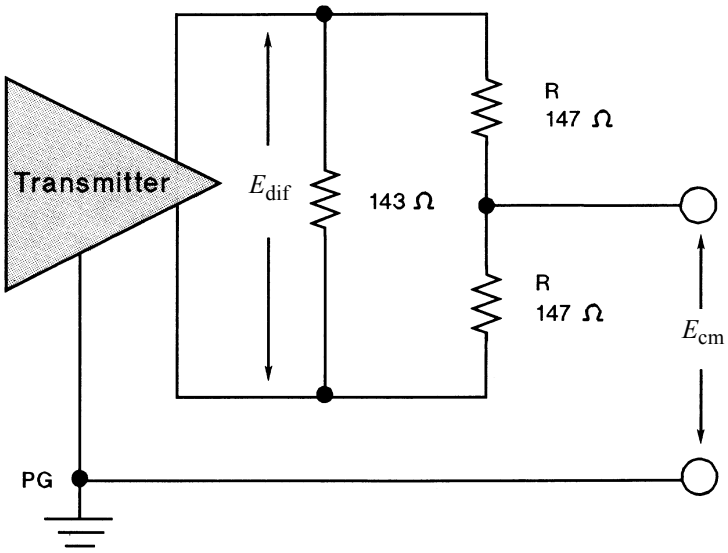


Figure 14–14—Transmitter impedance balance and common-mode rejection test circuit

14.3.1.2.5 Common-mode output voltage

The magnitude of the total common-mode output voltage of the transmitter, E_{cm}, measured as shown in Figure 14–15, shall be less than 50 mV peak at frequencies above 1 MHz.

NOTE—This specification is not intended to ensure compliance with regulations concerning RF emissions. The implementor should consider any applicable local, national, or international regulations. Driving unshielded twisted pairs with high-frequency, common-mode voltages may result in interference to other equipment.

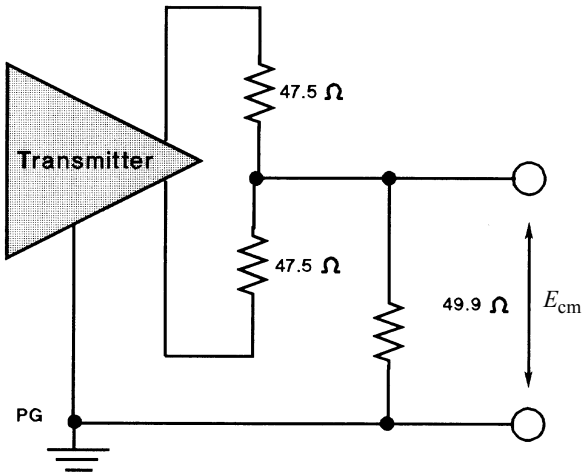


Figure 14–15—Common-mode output voltage test circuit

14.3.1.2.6 Transmitter common-mode rejection

The application of E_{cm}, as shown in Figure 14–14, shall not change the differential voltage at the TD circuit, E_{dif}, by more than 100 mV for all data sequences. Additionally, the edge jitter added by the application of E_{cm} shall be no more than 1.0 ns. E_{cm} shall be a 15 V peak 10.1 MHz sine wave.

14.3.1.2.7 Transmitter fault tolerance

Transmitters, when either idle or non-idle, shall withstand without damage the application of short circuits across the TD circuit for an indefinite period of time and shall resume normal operation after such faults are removed. The magnitude of the current through such a short circuit shall not exceed 300 mA.

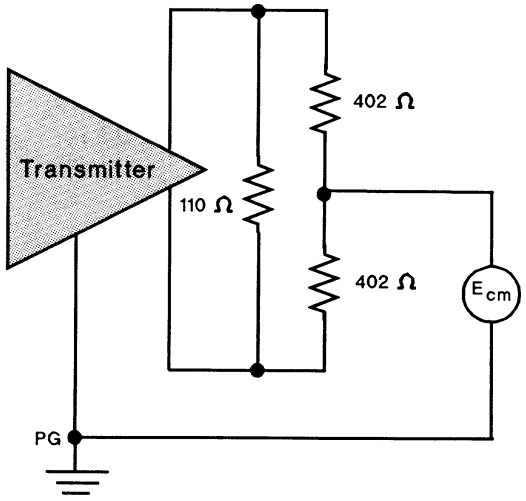


Figure 14–16—Transmitter fault tolerance test circuit

Transmitters, when either idle or non-idle, shall withstand without damage a 1000 V common-mode impulse applied at E_{cm} of either polarity (as indicated in Figure 14–16). The shape of the impulse shall be 0.3/50 µs (300 ns virtual front time, 50 µs virtual time of half value), as defined in IEC 60060.

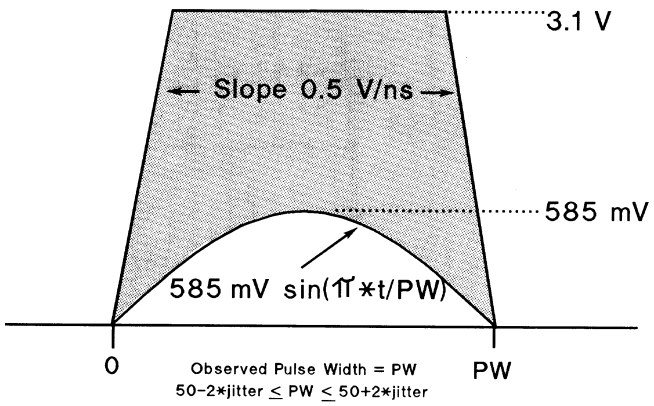


Figure 14–17—Receive differential input voltage—narrow pulse

14.3.1.3 Receiver specifications

The MAU shall provide the Receive function specified in 14.2.1.2 in accordance with the electrical specifications of this clause.

14.3.1.3.1 Receiver differential input signals

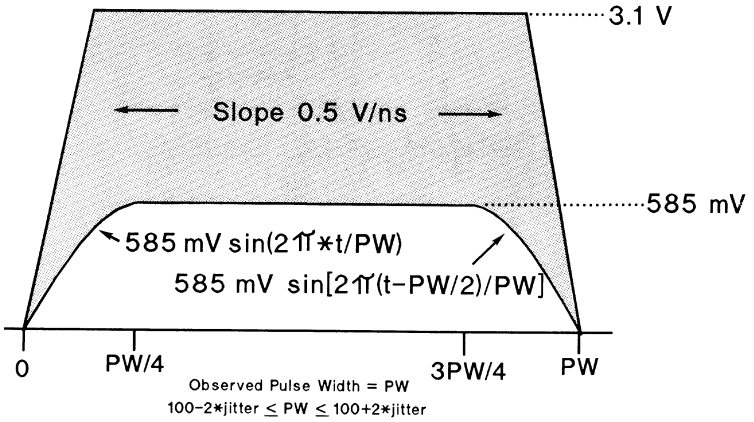


Figure 14–18—Receiver differential input voltage—wide pulse

Differential signals received on the RD circuit that are within the envelope of Figure 14–17 and Figure 14–18, and have a maximum zero crossing jitter up to ±13.5 ns from the ideal shall be sent to the DI circuit. The 13.5 ns includes jitter caused by an encoder, AUI cable and transmitting MAU, the twisted pair, and noise. Additionally, the MAU receiver shall add no more than ±1.5 ns jitter to the receive signal before sending the signal to the DI circuit.

14.3.1.3.2 Receiver differential noise immunity

The receiver, when presented with Manchester-encoded data meeting the requirements of 14.3.1.3.1, shall send this data to the DI circuit with a bit loss of no more than that specified in 14.2.1.2. In addition, the receiver, when presented with a signal meeting the requirements of 14.2.1.1 and within the envelope of Figure 14–13, shall accept it as a link test pulse.

The receiver, while in the Idle state, shall reject as *RD_input* the following signals:

a) All signals that when measured at the output of the following filter would produce a peak magnitude less than 300 mV. The filter is a 3-pole low-pass Butterworth with a 3 dB cutoff at 15 MHz (refer to B.4.2).
b) All continuous sinusoidal signals of amplitude less than 6.2 V peak-to-peak and frequency less than 2 MHz.
c) All sine waves of single cycle duration, starting with phase 0 or 180 degrees, and of amplitude less than 6.2 V peak-to-peak where the frequency is between 2 MHz and 15 MHz. For a period of 4 BT before and after this single cycle, the signal shall be less than 300 mV when measured through the filter specified in a) above.

14.3.1.3.3 Idle input behavior

The idle condition shall be detected within 2.3 BT of the last low-to-high transition at the receiver. The receiver shall take precautions to ensure that the high-to-silence transition of the start of idle is not falsely interpreted as a silence-to-non-idle-transition, even in the presence of signal droop, overshoot, ringing, slow voltage decay, or a combination thereof due to capacitive and inductive effects in the transmitter, link segment, and receiver.

14.3.1.3.4 Receiver differential input impedance

The differential input impedance shall be such that any reflection, due to differential signals incident upon the RD circuit from a twisted pair having any impedance within the range specified in 14.4.2.2 shall be at least 15 dB below the incident over the frequency range of 5.0 MHz to 10 MHz. The return loss shall be maintained when the MAU is powered.

14.3.1.3.5 Common-mode rejection

Receivers shall assume the proper state on DI for any differential input signal E_s that results in a signal E_{dif} that meets 14.3.1.3.1 even in the presence of common-mode voltages E_{cm} (applied as shown in Figure 14–19). E_{cm} shall be a 25 V peak-to-peak square wave, 500 kHz or lower in frequency, with edges no slower than 4 ns (20%–80%). Additionally, E_{cm} shall contribute no more than 2.5 ns of edge jitter to the signal transmitted on the DI circuit. The combination of the receiver timing jitter of 14.3.1.3.1 and the common-mode induced jitter are such that the MAU shall add no more than 4.0 ns of edge jitter to E_s before sending the signal on the DI circuit.

14.3.1.3.6 Receiver fault tolerance

The receiver shall tolerate the application of short circuits between the leads of the RD circuit for an indefinite period of time without damage and shall resume normal operation after such faults are removed. Receivers shall withstand without damage a 1000 V common-mode impulse of either polarity ($E_{impulse}$ as indicated in Figure 14–20). The shape of the impulse shall be 0.3/50 µs (300 ns virtual front time, 50 µs virtual time of half value), as defined in IEC 60060.

14.3.2 MAU-to-AUI specification

When a MAU contains a physical AUI connector, the following specifications shall be met.

14.3.2.1 MAU-AUI electrical characteristics

The electrical characteristics for the driver and receiver components within the MAU that are connected to the AUI shall be identical to those specified in 7.4 and 7.5. Additionally, the AUI DO receiver, while in the Idle state, shall reject an input waveform of less than ±160 mV differential.

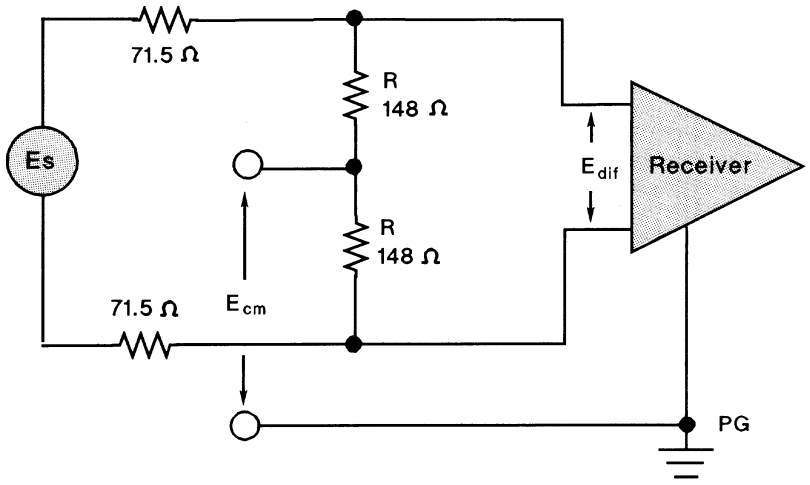


Figure 14–19—Receiver common-mode rejection test circuit

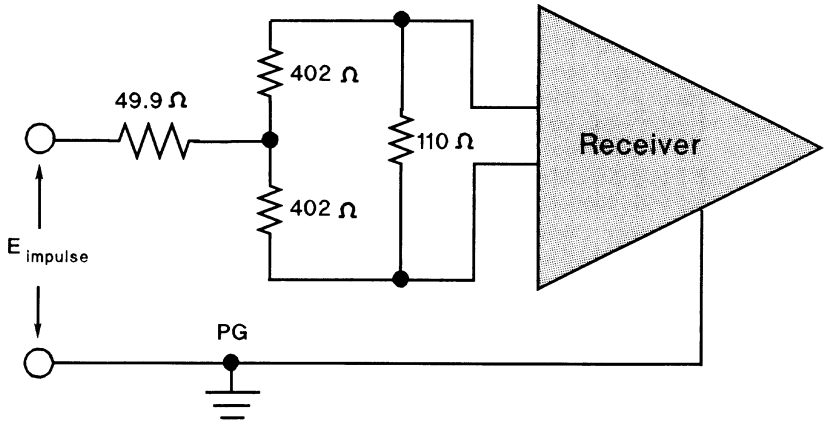


Figure 14–20—Common-mode impulse test circuit

14.3.2.2 MAU–AUI mechanical connection

The MAU shall be provided with a 15-pin male connector as specified in 7.6.

14.3.2.3 Power consumption

Following PowerOn, the surge current drawn by the MAU shall be such that $I_p \quad T_w$ is less than or equal to $2 \quad 10^{-3}$ ampere-seconds, where I_p is the peak surge current and T_w is the time during which the current exceeds the larger of 0.5 A or $0.5 \quad I_p$. After the 100 ms following PowerOn, the current drawn by the MAU shall not exceed 0.5 A when powered by the AUI.

The MAU shall be capable of operating from all possible voltage sources, including those current limited to 0.5 A, as supplied by the DTE or repeater through the resistance of all permissible AUI cables.

The MAU shall not introduce extraneous signals on the TD, CI, or DI circuits during normal power-up and power-down.

14.4 Characteristics of the simplex link segment

Except where otherwise stated, the simplex link segment shall be tested with source and load impedances of 100 Ω.

14.4.1 Overview

The medium for 10BASE-T is twisted-pair wiring. A significant number of 10BASE-T networks are installed utilizing in-place unshielded telephone wiring and typical telephony installation practices, the end-to-end path including different types of wiring, cable connectors, and cross connects must be considered. Typically, a DTE connects to a wall outlet using a twisted-pair patch cord. Wall outlets connect through building wiring and a cross connect to the repeater MAU in a wiring closet.

The medium for 10BASE-Te is twisted-pair wire. The requirements of the 10BASE-Te simplex link segment (either pure 10BASE-Te or mixed 10BASE-T, 10BASE-Te) are equivalent to the requirements of the Class D channel specified by ISO/IEC 11801:1995. This requirement can also be met by Category 5 cable and components as specified in ANSI/TIA/EIA-568-A.

NOTE—ISO/IEC 11801:2002 provides a specification for media that exceeds the minimum requirements of this standard.

14.4.2 Transmission parameters

Each simplex link segment shall have the following characteristics. All characteristics specified apply to the total simplex link segment unless otherwise noted. These characteristics are generally met by 100 m of twisted-pair cable composed of 0.5 mm [24 AWG] twisted pairs.

14.4.2.1 Insertion loss

The insertion loss of a simplex link segment shall be no more than 11.5 dB at all frequencies between 5.0 MHz and 10 MHz for a 10BASE-T MAU that is not a 10BASE-Te MAU. For a 10BASE-Te MAU, the insertion loss of a simplex link segment shall be no more than 8.5 dB at all frequencies between 5.0 MHz and 10 MHz. This consists of the attenuation of the twisted pairs, connector losses, and reflection losses due to impedance mismatches between the various components of the simplex link segment. The insertion loss specification shall be met when the simplex link segment is terminated in source and load impedances that satisfy 14.3.1.2.2 and 14.3.1.3.4.

NOTE—Multipair PVC-insulated 0.5 mm [24 AWG] cable typically exhibits an attenuation of 8 dB to 10 dB/100 m at 20 °C. The loss of PVC-insulated cable exhibits significant temperature dependence. At temperatures greater than 40 °C, it may be necessary to use a less temperature-dependent cable, such as most plenum-rated cables.

14.4.2.2 Differential characteristic impedance

The magnitude of the differential characteristic impedance of a 3 m length of twisted pair used in a simplex link segment shall be between 85 Ω and 111 Ω for all frequencies between 5.0 MHz and 10 MHz. Since characteristic impedance tends to decrease with increasing frequency, the above requirement is generally implied by the condition that the magnitude of the characteristic impedance over the frequency band 1 MHz to 16 MHz is 100 Ω ± 15 Ω. Also, the magnitude of the input impedance averaged over the 5.0 MHz to 10 MHz frequency band of a simplex link segment terminated in 100 Ω shall be between 85 Ω and 111 Ω.

14.4.2.3 Medium timing jitter

Intersymbol interference and reflections due to impedance mismatches between tandem twisted pairs of a twisted-pair link segment and effects of connection devices can introduce jitter to the CD1 and CD0 signals

received on the RD circuit. No more than ±5.0 ns of jitter shall be introduced to a test signal by a simplex link segment. The test signal shall have a peak amplitude of 3.0 V and 10% to 90% rise and fall times of 12 ns. The content of the test signal shall be a Manchester-encoded pseudo-random sequence with a minimum repetition period of 511 bits.

NOTE—Branches off a twisted pair (often referred to as "bridged taps" or "stubs") will generally cause excessive jitter and so should be avoided.

14.4.2.4 Delay

The maximum propagation delay of twisted pair shall be 5.7 ns/m (minimum velocity of 0.585 c). The maximum propagation delay of a link segment shall not exceed 1000 ns.

14.4.3 Coupling parameters

To avoid excessive coupling of signals between twisted pairs of a twisted-pair cable, the crosstalk must be limited. Crosstalk loss is specified for the twisted pairs in a twisted-pair cable or twisted-pair cable binder group that are used as 10BASE-T twisted-pair links. Crosstalk loss is specified with the far ends of both the disturbed and the disturbing pairs and the near end of the disturbed pair terminated in 100 Ω. Drivers of disturbing pairs shall have a source impedance of 100 Ω.

14.4.3.1 Differential near-end crosstalk (NEXT) loss

The NEXT loss between any two twisted pairs of a twisted-pair cable is dependent upon the geometry of the twisted-pair cable. Since the proximity of any two twisted pairs is influenced by the size of the twisted-pair cable, the NEXT loss is affected by twisted-pair cable size.

14.4.3.1.1 Twenty-five-pair cable and twenty-five-pair binder groups

The NEXT loss between any two twisted pairs in a twenty-five-pair twisted-pair cable or binder group used for 10BASE-T applications shall be at least $30 - 15 \log_{10}(f/10)$ dB (where f is the frequency in MHz) over the frequency range 5.0 MHz and 10 MHz.

14.4.3.1.2 Four-pair cable

The NEXT loss between any two twisted pairs in a four-pair twisted-pair cable used for 10BASE-T applications shall be at least $26 - 15 \log_{10}(f/10)$ dB (where f is the frequency in MHz) over the frequency range 5.0 MHz and 10 MHz.

14.4.3.1.3 Other cables

The NEXT loss requirement for all other twisted-pair cables shall be the multiple-disturber NEXT loss of 14.4.3.2.

14.4.3.2 Multiple-disturber NEXT (MDNEXT) loss

When a twisted-pair cable or twisted-pair cable binder group contains twisted pairs from multiple 10BASE-T twisted-pair link segments, the multiple-disturber crosstalk loss is dependent upon the specific selection of disturbing and disturbed pairs. For each 10BASE-T receive pair, MDNEXT is measured by having the remaining near-end transmit pairs (excluding the transmit pair associated with the receive pair under test) driven with identical and synchronized sine wave signals. MDNEXT may then be determined from the signal level observed on the receive pair under test. By examining all pair combinations with a fixed number of disturbers, a cumulative distribution of MDNEXT is obtained at each frequency of interest. The one percentile of this cumulative distribution shall be at least $23 - 15 \log_{10}(f/10)$ (where f is the frequency in

MHz) at 5.0 MHz, 7.5 MHz, and 10 MHz. When the number of possible combinations allowed by a cable is fewer than 100, the MDNEXT loss for all combinations shall be at least $23 - 15 \log_{10}(f/10)$ (where f is the frequency in MHz) at 5.0 MHz, 7.5 MHz, and 10 MHz. Refer to 12.7.3.2 and B.3 for a tutorial and method for estimating the MDNEXT loss for a complete n-pair cable.

14.4.4 Noise environment

The noise level on the link segments shall be such that the objective error ratio is met. The noise environment consists generally of two primary contributors: crosstalk from other 10BASE-T circuits; and externally induced impulse noise, typically from telephone ringing and dialing signals, and other office and building equipment.

14.4.4.1 Impulse noise

The average rate of occurrence of impulses greater than 264 mV shall be less than or equal to 0.2/s as measured at the output of the following specified filter. Following the start of any particular impulse that is counted, any additional impulse shall be ignored for a period of 1 μs. The simplex link segment shall be terminated at the far end in 100 Ω. The filter is a 3-pole Butterworth low-pass with a 3 dB cutoff at 15 MHz (refer to B.4.2).

NOTE—Typically, the impulse noise occurrence rate changes inversely by one decade for each 5 dB to 9 dB change in the threshold voltage. If a count rate of N counts/s is measured on a specific twisted pair and filter at the specified voltage threshold, the media noise margin is approximately $7 \log_{10}(0.2/N)$ dB. Impulse noise may be a burst phenomenon and should be measured over an extended period of time.

14.4.4.2 Crosstalk noise

The level of crosstalk noise on a simplex link segment depends on the level of the disturbing signal(s) and the crosstalk loss between the pair(s) carrying the signal(s) and the disturbed pair. With the maximum transmit level (14.3.1.2), the sinusoidal crosstalk loss (14.4.3.2), and multiple, random Manchester-encoded disturbers, the peak self-crosstalk noise levels as measured at the output of the following specified filter shall be less than or equal to 264 mV. The filter is a 3-pole Butterworth low-pass with a 3 dB cutoff at 15 MHz (refer to B.4.2).

14.5 MDI specification

This subclause defines the MDI for the twisted-pair link segment. The link topology requires a crossover function between PMAs. Implementation and location of this crossover is also defined in this clause.

14.5.1 MDI connectors

Eight-pin connectors meeting the requirements of Clause 3 and Figures 1 through 5 of IEC 60603-7 shall be used as the mechanical interface to the twisted-pair link segment. The plug connector shall be used on the

twisted-pair link segment and the jack on the MAU. These connectors are depicted (for informational use only) in Figure 14–21 and Figure 14–22. The following table shows the assignment of signals to connector contacts.

Contact	MDI signal
1	TD+
2	TD–
3	RD+
4	Not used by 10BASE-T
5	Not used by 10BASE-T
6	RD–
7	Not used by 10BASE-T
8	Not used by 10BASE-T

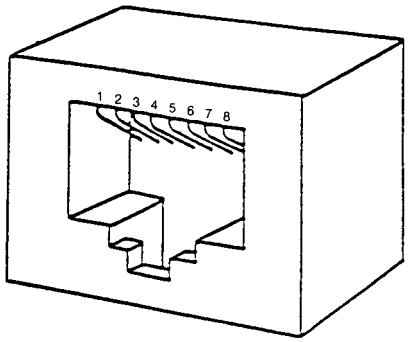


Figure 14–21—MAU MDI connect

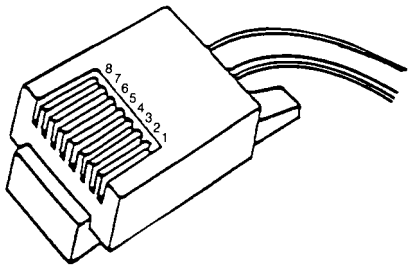


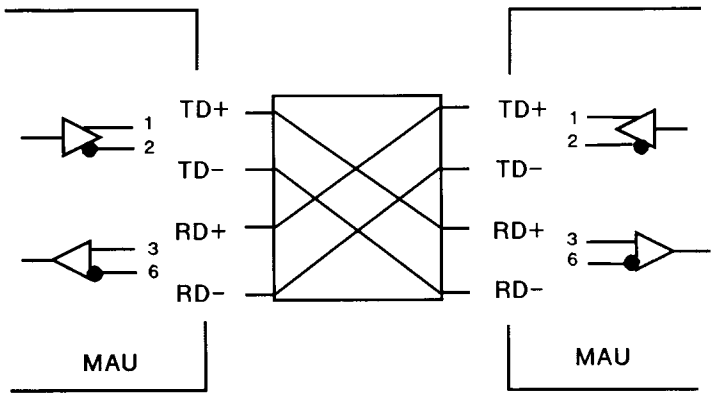
Figure 14–22—Twisted-pair link segment connector

14.5.2 Crossover function

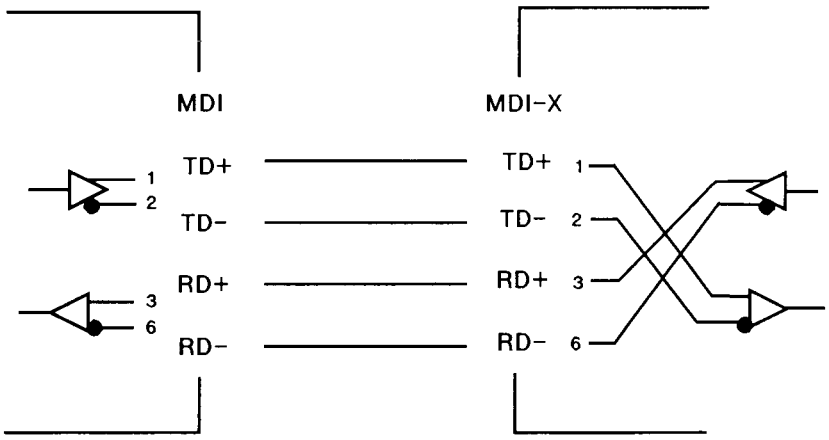
A crossover function shall be implemented in every twisted-pair link. The crossover function connects the transmitter of one MAU to the receiver of the MAU at the other end of the twisted-pair link. Crossover functions may be implemented internally to a MAU or elsewhere in the twisted-pair link. For MAUs that do not implement the crossover function, the signal names of 14.5.1 refer to their own internal circuits. For MAUs that do implement the crossover function, the signal names refer to the remote MAU of the twisted-pair link. Additionally, the MDI connector for a MAU that implements a fixed crossover function shall be marked with the graphical symbol “X”. Internal and external crossover functions are shown in Figure 14–23.

When a twisted-pair link connects a DTE to a repeater, it is recommended that the crossover be implemented in the MAU local to the repeater. If both MAUs of a twisted-pair link contain internal crossover functions, an additional external crossover is necessary. It is recommended that the crossover be visible to an installer from one of the MAUs. When both MAUs contain internal crossovers, it is further recommended in networks in which the topology identifies either a central backbone segment or a central hub that the MAU furthest from the central element be assigned the external crossover to maintain consistency.

Implicit implementation of the crossover function within a twisted-pair cable, or at a wiring panel, while not expressly forbidden, is beyond the scope of this standard.



a) External Crossover function



b) MAU-Embedded Crossover function

Figure 14–23—Crossover function

14.6 System considerations

The repeater unit specified in Clause 9 forms the central unit for interconnecting 10BASE-T twisted-pair links in networks of more than two nodes. It also provides the means for connecting 10BASE-T twisted-pair links to other 10 Mb/s baseband segments. The proper operation of a CSMA/CD network requires network size to be limited to control round-trip propagation delay to meet the requirements of 4.2.3.2.3 and 4.4.2, and the number of repeaters between any two DTEs to be limited in order to limit the shrinkage of the interpacket gap as it travels through the network. Configuration rules, which ensure that these limits are not exceeded, are given in Clause 13.

14.7 Environmental specifications

14.7.1 General safety

All equipment meeting this standard shall conform to IEC 60950-1.

14.7.2 Network safety

This subclause sets forth a number of recommendations and guidelines related to safety concerns; the list is neither complete nor does it address all possible safety issues. The designer is urged to consult the relevant local, national, and international safety regulations to ensure compliance with the appropriate requirements.

LAN cable systems described in this subclause are subject to at least four direct electrical safety hazards during their installation and use. These hazards are as follows:

a) Direct contact between LAN components and power, lighting, or communications circuits.
b) Static charge buildup on LAN cables and components.
c) High-energy transients coupled onto the LAN cable system.
d) Voltage potential differences between safety grounds to which various LAN components are connected.

Such electrical safety hazards must be avoided or appropriately protected against for proper network installation and performance. In addition to provisions for proper handling of these conditions in an operational system, special measures must be taken to ensure that the intended safety features are not negated during installation of a new network or during modification or maintenance of an existing network. Isolation requirements are defined in 14.3.1.1.

14.7.2.1 Installation

Sound installation practice, as defined by applicable local codes and regulations, shall be followed in every instance in which such practice is applicable.

14.7.2.2 Grounding

Any safety grounding path for the MAU shall be provided through the circuit PG of the AUI connection.

WARNING

It is assumed that the equipment to which the MAU is attached is properly earthed, and not left floating nor serviced by a “doubly insulated ac power distribution system.” The use of floating or insulated equipment, and the consequent implications for safety are beyond the scope of this standard.

14.7.2.3 Installation and maintenance guidelines

During installation and maintenance of the cable plant, care shall be taken to ensure that uninsulated network cable conductors do not make electrical contact with unintended conductors or ground.

14.7.2.4 Telephony voltages

The use of building wiring brings with it the possibility of wiring errors that may connect telephony voltages to 10BASE-T equipment. Other than voice signals (which are low voltage), the primary voltages that may be encountered are the “battery” and ringing voltages. Although there is no universal standard, the following maximums generally apply.

Battery voltage to a telephone line is generally 56 Vdc applied to the line through a balanced 400 Ω source impedance.

Ringing voltage is a composite signal consisting of an ac component and a dc component. The ac component is up to 175 V peak at 20 Hz to 60 Hz with a 100 Ω source resistance. The dc component is 56 Vdc with a 300 Ω to 600 Ω source resistance. Large reactive transients can occur at the start and end of each ring interval.

Although 10BASE-T equipment is not required to survive such wiring hazards without damage, application of any of the above voltages shall not result in any safety hazard.

NOTE—Wiring errors may impose telephony voltages differentially across 10BASE-T transmitters or receivers. Because the termination resistance likely to be present across a receiver's input is of substantially lower impedance than an off-hook telephone instrument, receivers will generally appear to the telephone system as off-hook telephones. Therefore, full-ring voltages will be applied for only short periods. Transmitters that are coupled using transformers will similarly appear like off-hook telephones (though perhaps a bit more slowly) due to the low resistance of the transformer coil.

14.7.3 Environment

14.7.3.1 Electromagnetic emission

The twisted-pair link shall comply with applicable local and national codes for the limitation of electromagnetic interference.

14.7.3.2 Temperature and humidity

The twisted-pair link is expected to operate over a reasonable range of environmental conditions related to temperature, humidity, and physical handling (such as shock and vibration). Specific requirements and values for these parameters are considered to be beyond the scope of this standard.

It is recommended that manufacturers indicate in the literature associated with the MAU the operating environmental conditions to facilitate selection, installation, and maintenance.

It is recommended that manufacturers indicate, in the literature associated with the components of the twisted-pair link segment, the distance and operating environmental conditions over which the specifications of 14.4 will be met.

14.8 MAU labeling

It is recommended that each MAU (and supporting documentation) be labeled in a manner visible to the user with at least these parameters:

a) Data rate capability in Mb/s,
b) Power level in terms of maximum current drain (for external MAUs),
c) Any applicable safety warnings,
d) Duplex capabilities, and
e) Which of the two specifications is implemented, i.e., 10BASE-T or 10BASE-Te (not both).

See also 14.5.2.

14.9 Timing summary

Table 14–2 summarizes the timing requirements for the 10BASE-T twisted-pair link. This table is a summary; for complete descriptions of the timing requirements, refer to the referenced subclauses.

Table 14–2—Maximum timing parameters

Symbol	Function	Bit loss[a]	Invalid bits[b]	Steady-state propagation delay[b]	Start-up delay[b]		Specified in
					Maximum	Variability	
M1	*RD_input* to *input* on DI	5.0	1.0	2.0	8.0	2.0	14.2.1.2
M2	*output* on DO to *TD_output*	2.0	1.0	2.0	5.0	2.0	14.2.1.1
M3	*RD_input* * *output* to *signal_quality_error*	—	—	—	9.0	—	14.2.1.4
M4	*RD_idle* + *output_idle* (end of collision) to *mau_available*	—	—	—	9.0	—	14.2.1.4
M5	*RD_input* * *output* to *input* on DI from circuit RD	—	—	—	9.0	—	14.2.1.4
M6	*RD_idle* * *output* to *input* on DI from circuit DO	—	—	—	9.0	—	14.2.1.4
M7	*output_idle* on DO to *signal_quality_error*	—	—	—	6 < x < 16	—	14.2.1.5
M8	*signal_quality_error* duration for SQE test	—	—	—	5 < x < 15	—	14.2.1.5
M9	*output* on DO to *input* on DI	5.0	1.0	1.0	7.0	—	14.2.1.3
T1	twisted-pair propagation	0	0	10.00	10.00	—	14.4.2.4
A1	AUI cable propagation (50 m)	0	0	2.57	2.57	—	7.4.3.7

[a]All time in BT.
[b]For an explanation of the meaning of variability, see 14.2.1.1 and 14.2.1.2.