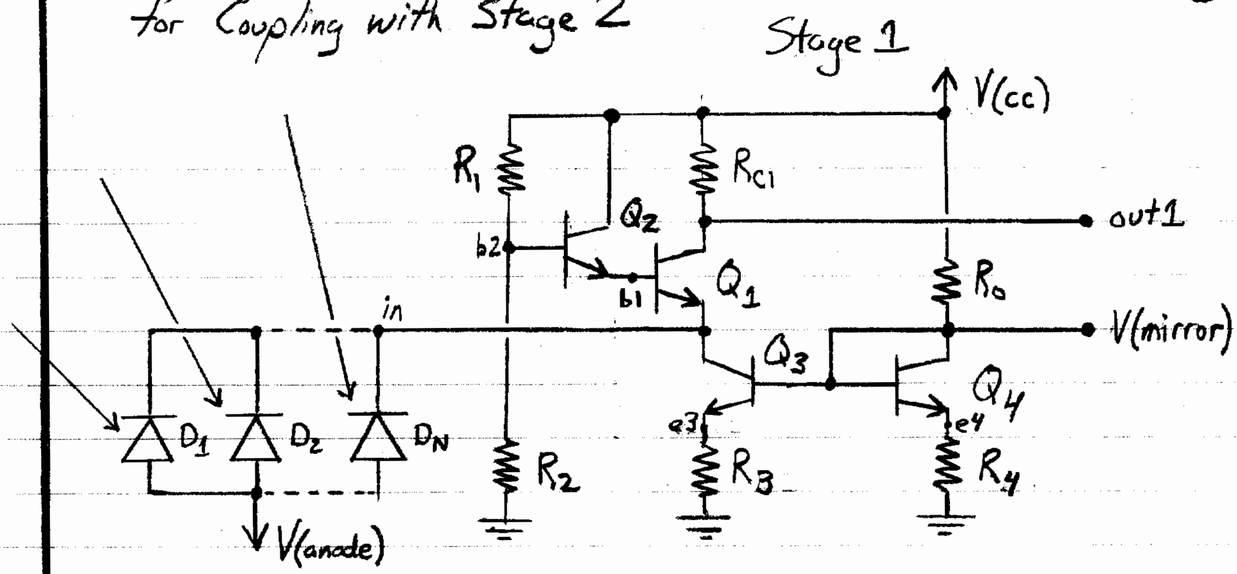
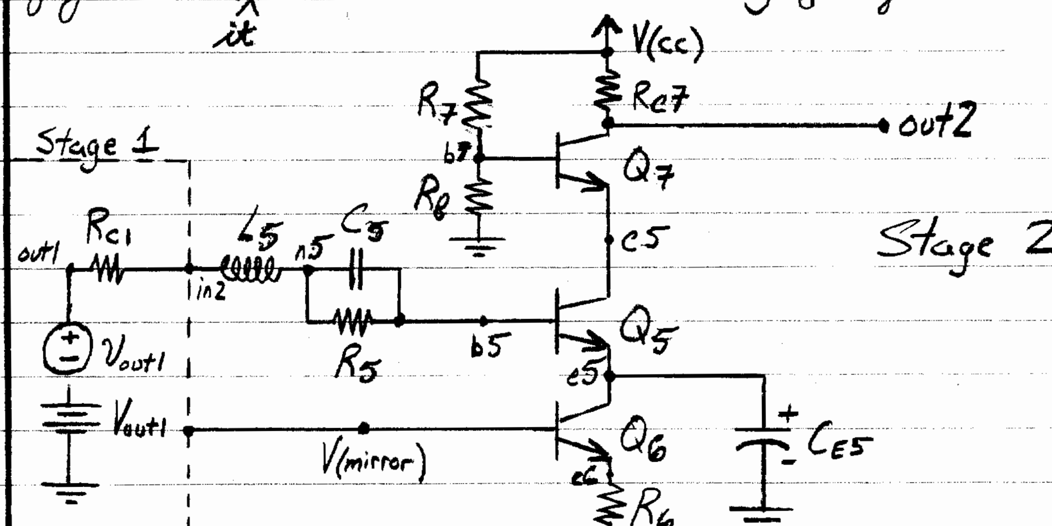
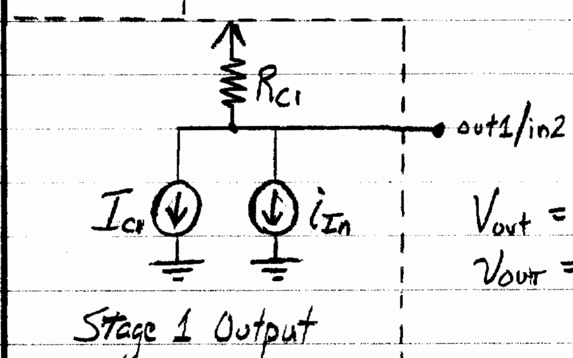
Redesign of Stage 1 for Coupling with Stage 2



This is the 3rd design of stage 1, but it would be more appropriate to call it "version 1.5" than 3; In this design we revert to passing all of I_{C1} through R_{C1}, but keep the Miller capacitance consideration of d2.

It turns out that d2 was a case of premature optimization: Increasing R_{C1} does increase the gain of stage 1 in isolation, but ~~the relation of gain to R_{C1}~~ it is canceled when the loading of stage 2 is considered.





$V_{out} = R_{C1} I_{C1}$

$V_{OUT} = R_{C1} i_{IN}$

Thevenin Equivalent Coupling shows irrelevence of R_{C1} value.

Luckily moving Q_2 from the collector to the base of Q_1 does not change the AC equivalent circuit, so the gain equation [8] is still valid. Ignoring loading effects, it is

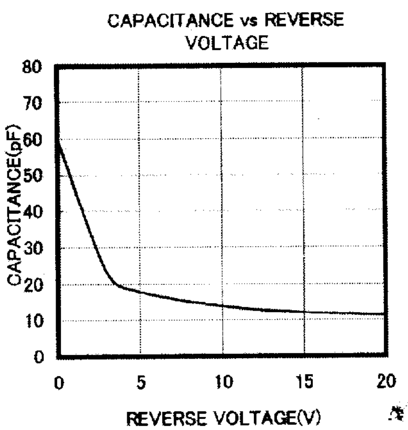
[8] $$Z_{gain}^{-1} = \frac{1}{R_{C1}}\left[1 + \frac{\omega}{\omega_2}\left(\frac{1}{\sqrt{1+(\omega/\omega_1)^2}} + \frac{jA}{\sqrt{1+(\omega_1/\omega)}}\right)e^{-j\left[\frac{\pi}{4}+\tan^{-1}\left(\frac{\omega}{\omega_1}\right)\right]}\right]$$

where

$$A = 1 + \frac{R_{C1} I_{C1}}{V_T}, \quad \omega_1 = \frac{1}{R_{TH} C_c}, \quad \text{and} \quad \omega_2 = \frac{I_C}{C_Z V_T}$$

The quiescent I_{C1} current is still dependent on total junction capacitance of the photodiodes. Note that C_Z is non-linearly dependent on V(anode).

[9a] $$I_{C1} = 2\pi f_Z C_Z V_T$$



Where C_Z is the junction capacitance of a single MTD301PM photodiode multiplied by the number connected in parallel.

The total reverse voltage is

[9b] $$V_{reverse} = V_{in} - V_{anode}$$

It would be beneficial to redesign the DC operating potentials to maximize V_{in}.

[10] $V_{CC} = 5V$ | $\cancel{V_{out} = 4.5V}$ | $V_{b1} = 2V$ | $V_{in} = 3V$ | $V_{mirror} = 1V$

The other high frequency pole, ω_1, is dependent on the base-collector junction capacitance of Q_1 and the resistance seen by b1 to ground. In the previous design this was

$$R_{TH} = \frac{1}{2\pi f_1 C_c}$$

But the equivalent resistance seen by b1 is now

$$R_{TH}' = \frac{R_{TH}}{\beta} = \frac{1}{2\pi f_1 C_c}$$ and the voltage is shifted by $V_{BE(on)}$

$$V_{TH}' = V_{TH} - V_{BE(sat)} = V_{b1}$$

Solving for R_{TH} and V_{TH} at node b2,

$$R_{TH} = \frac{\beta}{2\pi f_1 C_c} \qquad V_{TH} = V_{b1} + V_{BE(sat)}$$

Converting R_{TH} and V_{TH} to values for R_1 and R_2

[13a] $$R_1 = R_{TH}\frac{V_{cc}}{V_{TH}} = \frac{\beta}{2\pi f_1 C_c}\cdot\frac{V_{cc}}{V_{b1}+V_{BE(sat)}}$$

[13b] $$R_2 = R_{TH}\frac{V_{cc}}{V_{cc}-V_{TH}} = \frac{\beta}{2\pi f_1 C_c}\cdot\frac{V_{cc}}{V_{cc}-V_{b1}-V_{BE(on)}}$$ $\frac{5}{5-4-0.75} = 20$

But we have already designed all the voltages in equation [10], so assuming $V_{BE(sat)} = 0.75\,V$,

[13.c] $$R_1 = \frac{1.818\beta}{2\pi f_1 C_c}$$

[13d] $$R_2 = \frac{2222\beta}{2\pi f_1 C_c}$$

As discussed earlier, the value of R_{C1} does not matter in terms of gain, so its value should be set based on what is optimal for stage 2. But, from a DC bias consideration, its value must be small enough that Q_1 is not saturated

$$V_{cc} - R_{C1}I_{C1} > V_{b1}$$

$$R_{C1} < \frac{V_{cc}-V_{b1}}{I_{C1}}$$

[14] $$R_{C1} = \left\{ \begin{array}{l} \text{should be set during design} \\ \text{of stage 2, but such that} \end{array} \;\middle|\; R_{C1} < \frac{V_{cc}-V_{b1}}{I_{C1}} \right\}$$

To make the current mirror stiffly biased, I_0 should be an order of magnitude greater than I_{C1}/β_3.

$$R_3 = \frac{V_{mirror} - V_{BE(on)}}{I_{C1}}, \quad R_4 = \frac{V_{mirror} - V_{BE(on)}}{10\cdot I_{C1}/\beta}, \quad R_0 = \frac{V_{cc} - V_{mirror}}{10\cdot I_{C1}/\beta}$$

Assuming $V_{BE(on)} = 0.75V$, $\beta = 100$, and substituting in equation [10] for V_{mirror}, then the remaining resistor values are

[15a,b,c] $$R_0 = \frac{40\,V}{I_{C1}}, \quad R_3 = \frac{0.25\,V}{I_{C1}}, \quad R_4 = \frac{2.5\,V}{I_{C1}}$$

So, iteratively, the way to design component values for stage 1 is

1. Calculate summation of photodiodes' junction capacitance, using

$$V_{reverse} = 1.25V - V_{anode}$$

and the Capacitance vs Reverse Voltage plot, and the # of photodiodes.

$$C_\Sigma = \sum_{i=0}^{n} C_{Vr} = n C_{Vreverse}$$

2. Calculate I_{c1} based on high corner frequency f_2 $\left(= \frac{I_c}{2\pi C_\Sigma V_T}\right)$

$$I_{c1} = 2\pi f_2 C_\Sigma V_T$$

3. Calculate values for R_0, R_4, and R_4 from I_{c1}

$$R_0 = \frac{40V}{I_{c1}}, \quad R_3 = \frac{0.25V}{I_{c1}}, \quad R_4 = \frac{2.5V}{I_{c1}}$$

4. Calculate R_1 and R_2 based on another high corner frequency f_1 $\left(= \frac{1}{2\pi R_{TH} C_c}\right)$

$$R_1 = \frac{1.818\beta}{2\pi f_1 C_c}, \quad R_2 = \frac{2.222\beta}{2\pi f_1 C_c}$$

5. Determine R_{c1} based on what is optimal for stage 2, but ensure that $R_{c1} \leq \frac{3V}{I_{c1}}$

6. One should also check that I_{c1} is within the specifications of the BJT.