A STUDY ON THE IMPLEMENTATION OF THREE-VALUED LOGIC

by

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Abstract

A system of three-valued algebra, based on operators previously defined, is presented. COS/MOS integrated circuits are applied to realize the three-valued operators. An approach to avoid the use of diodes in COS/MOS integrated circuit technology is given and a method for reduction of logical circuitry is discussed.

1. Introduction

Many authors have directed their efforts to the implementation of three-valued logic looking to benefit from all advantages it possesses over the binary logic[1-4]. All these attempts have not yet been sufficient to provide opportunity for three-valued logic systems to be as widely used as the two-valued logic systems. This is due to the lack of a suitable ternary memory element as well as of complete integrable ternary circuits at a reasonable cost. The use of integrated circuits in designing ternary circuits may be a good solution to this problem. Taking advantages of some properties in Complementary-Symmetry Metal Oxide Semi-conductor Devices, known as COS/MOS integrated circuits, a new method of design of three-valued switching circuits has been presented [5-6]. In this paper only the device-oriented algebra used in this design is described and a method for reduction of logical circuitry is discussed. The algebra includes ternary operators previously given by Mine et al[7].

2. The Algebra

Let the three voltage levels of ternary logic circuits be represented by 0, 1 and 2. The 0 represents the low, 1 the intermediate and 2 the high level. Let $L = \{0,1,2\}$. In L a set of operators are defined. For $x, y, z \in L$ there exists an equivalence (=) operation, that is:

$x = x$
If $x = y$, then $y = x$
If $x = y$ and $y = z$, then $x = z$

The simple ternary inverter (STI), positive ternary inverter (PTI), negative ternary inverter (NTI), forward diode (FD) and reverse diode (RD), are considered as basic unary operators. These are presented by Table I and equations (1)-(3), respectively:

$$STI \equiv \overline{x^1} = 2 - x \tag{1}$$

$$PTI,\ NTI \equiv \overline{x^1} = \begin{cases} i & \text{if } x \neq i \\ 2-i & \text{if } x = i \end{cases} \tag{2}$$

where i takes the value of 2 for the PTI and 0 for the NTI operator. The minus sign in equations (1) and (2) represents arithmetic subtraction.

$$FD,\ RD \equiv x^{K_i} = \begin{cases} 1 & \text{if } x \neq i \\ i & \text{if } x = i \end{cases} \tag{3}$$

where i can be 2 or 0, K_2 represents the FD operator ($\overline{\ }$), and K_0 the RD operator ($\overline{\ }$).

The operation of addition (+) and multiplication (·) on L, which can be called ternary OR(TOR) and ternary AND(TAND) respectively, represent two multiple input operators. These are given in Table II and the following equations:

$$TOR \equiv x + y = MAX(x,y) \tag{4}$$
$$TAND \equiv x \cdot y = MIN(x,y) \tag{5}$$

The two-element operations obey the idempotent, commutative, associative, distributive and absorption laws.

It is evident that laws of the identity elements, hold also here.

$$x + 0 = x \tag{6.a}$$
$$x \cdot 2 = x \tag{6.b}$$
$$x + 2 = 2 \tag{7.a}$$
$$x \cdot 0 = 0 \tag{7.b}$$

Theorem: DeMorgan's Theorem holds for ternary logic when the three types of inverters are used:

$$\overline{(x+y)^0} = \overline{x^0} \cdot \overline{y^0} \tag{8.a}$$
$$\overline{(x \cdot y)^0} = \overline{x^0} + \overline{y^0} \tag{8.b}$$
$$\overline{(x+y)^1} = \overline{x^1} \cdot \overline{y^1} \tag{9.a}$$
$$\overline{(x \cdot y)^1} \quad \overline{x^1} + \overline{y^1} \tag{9.b}$$
$$\overline{(x+y)^2} = \overline{x^2} \cdot \overline{y^2} \tag{10.a}$$
$$\overline{(x \cdot y)^2} = \overline{x^2} + \overline{y^2} \tag{10.b}$$

All theorems, laws and relationships presented in this paper have been proven in reference 8.

It can be seen that theorems and laws presented above are nearly the same as those of the Boolean algebra with a little generalization. But there will be some differences due to the existence of three types of complements in the algebra presented here. This is shown clearly in the following theorems.

For any $x, y, z \in L$, the following theorems hold:

$$x + \overline{x^2} = 2 \tag{11.a}$$
$$x \cdot \overline{x^0} = 0 \tag{11.b}$$
$$(x \cdot y) + (x \cdot \overline{y^2}) = x \tag{12.a}$$
$$(x + y) \cdot (x + \overline{y^0}) = x \tag{12.b}$$
$$x + (\overline{x^2} \cdot y) = x + y \tag{13.a}$$
$$x \cdot (\overline{x^0} + y) = x \cdot y \tag{13.b}$$
$$(z \cdot x) + (z \cdot \overline{x^2} \cdot y) = (z \cdot x) + (z \cdot y) \tag{14.a}$$
$$(z + x) \cdot (z + \overline{x^0} + y) = (z + x) \cdot (z + y) \tag{14.b}$$
$$(x \cdot y) + (\overline{x^2} \cdot z) + (y \cdot z) = (x \cdot y) + (\overline{x^2} \cdot z) \tag{15.a}$$
$$(x + y) \cdot (\overline{x^0} + z) \cdot (y + z) = (x + y) \cdot (\overline{x^0} + z) \tag{15.b}$$

There is a set of relationships which interrelate any inverter with the two others. These can be expressed by the following equations:

$$\overline{x^0} + \overline{x^1} + \overline{x^2} = \overline{x^2} \tag{16.a}$$
$$\overline{x^0} \cdot \overline{x^1} \cdot \overline{x^2} = \overline{x^0} \tag{16.b}$$
$$\overline{x^0} + \overline{x^1} = \overline{x^1} \tag{16.a1}$$
$$\overline{x^0} \cdot \overline{x^1} = \overline{x^0} \tag{16.b1}$$
$$\overline{x^2} + \overline{x^1} = \overline{x^2} \tag{16.a2}$$
$$\overline{x^2} \cdot \overline{x^1} = \overline{x^1} \tag{16.b2}$$

$$\overline{\overline{x^1}} = x \tag{17}$$

$$\overline{\overline{\overline{x^0}^i}} = \overline{x^0} \tag{18}$$

$$\overline{\overline{\overline{x^2}^i}} = \overline{x^2} \tag{19}$$

where i = 0, 1, or 2.

$$\overline{\overline{x^1}^2} = \overline{\overline{x^0}^1} \tag{20}$$

$$\overline{\overline{x^1}^0} = \overline{\overline{x^2}^1} \tag{21}$$

$$\overline{\overline{x^2}^0} = \overline{\overline{x^2}^1} = \overline{\overline{x^2}^2} \tag{22}$$

$$\overline{\overline{x^0}^0} = \overline{\overline{x^0}^1} = \overline{\overline{x^0}^2} \tag{23}$$

$$\overline{x^0} + \overline{\overline{x^0}^i} = 2 \tag{24.a}$$

$$\overline{x^0} \cdot \overline{\overline{x^0}^i} = 0 \tag{24.b}$$

$$\overline{x^2} + \overline{\overline{x^2}^i} = 2 \tag{25.a}$$

$$\overline{x^2} \cdot \overline{\overline{x^2}^i} = 0 \tag{25.b}$$

where i = 0, 1, or 2.

For any x, y ∈ L there is also a set of relationships governing the manipulations of the FD and RD operators:

$$x^{\neg} = x + 1 \tag{26.a}$$

$$x^{\sim} = x \cdot 1 \tag{26.b}$$

$$(\overline{x^1})^{\neg} = (\overline{x^0})^{\neg} \tag{27}$$

$$(\overline{x^1})^{\sim} = (\overline{x^2})^{\sim} \tag{28}$$

$$(\overline{x^1})^{\neg} = \overline{(x^{\sim})^1} \tag{29}$$

$$(\overline{x^1})^{\sim} = \overline{(x^{\neg})^1} \tag{30}$$

$$\overline{(x^{\neg})^2} = \overline{x^2} \tag{31}$$

$$\overline{(x^{\sim})^0} = \overline{x^0} \tag{32}$$

$$\overline{(x^{\neg})^2} = 2 \tag{33}$$

$$\overline{(x^{\neg})^0} = 0 \tag{34}$$

$$(x + y)^{\neg} = x^{\neg} + y^{\neg} \tag{35.a}$$

$$(x \cdot y)^{\neg} = x^{\neg} \cdot y^{\neg} \tag{35.b}$$

$$(x + y)^{\sim} = x^{\sim} + y^{\sim} \tag{36.a}$$

$$(x \cdot y)^{\sim} = x^{\sim} \cdot y^{\sim} \tag{36.b}$$

Ternary functions of one or more variables may be represented in truth table or map form or algebraically in canonical form as a product of sums or sum of products.

Theorem: Any ternary function $f(x_1, x_2, \ldots, x_n)$ may be generated from $x_1, x_2, \ldots, x_n$ by means of +,., the unary functions $\overline{x^0}$, $\overline{x^1}$, $\overline{x^2}$, $x^{\neg}$ and $x^{\sim}$.

It has been proven by Halpern and Yoeli[2] that an algebra composed of the MAX, the MIN and three unary operators $\bar{x}$, $x^{\overline{1}0}$ and $x^{\overline{1}}$ with the constant 1 is a functionally complete system. Since the set of operators presented here are equivalent to those of the algebra due to Halpern and Yoeli except the constant 1 which can be substituted by the FD or the RD operator depending on the relationships given by equations (26.a) and (26.b), therefore the above theorem holds.

Moreover, it has been shown in reference 5 how these ternary operators realize algebras due to Post[9], Rosser and Turquette[10], Yeoli and Rosenfeld[4], Vacca[11], and Mine et al[7], which have been all proven to be functionally complete.

Any ternary function of n variables can be represented by:

$$f(x_1,x_2, \ldots, x_n) = 2 \cdot F_2(x_1,x_2, \ldots, x_n) + 1 \cdot F_1(x_1,x_2, \ldots, x_n) + 0 \cdot F_0(x_1,x_2, \ldots, x_n) \tag{37}$$

$$\text{i.e., } f = 2 \cdot F_2 + 1 \cdot F_1 + 0 \cdot F_0 \tag{38}$$

where F_k equals 2 when the value of the function f equals k, otherwise, it will equal 0.

Applying Equations (6.b) and (7.b) to the above equation, the function may be represented by:

$$f = F_2 + 1 \cdot F_1 \tag{39}$$

And with the aid of the relationship given in Equation (26.b) the function f can be directly represented by:

$$f = F_2 + F_1^{\sim} \tag{40}$$

Methods for minimization of ternary switching functions, previously described by several authors[3-4] and [12-13], can be applied to the algebra presented here. Most of these methods were applied to algebras composed of the MAX and MIN operations and unary functions defined by:

$$x^i = \begin{cases} 0 & \text{if } x \neq i \\ 2 & \text{if } x = i \end{cases} \tag{41}$$

where i can be 0, 1, or 2.

To be able to apply these methods the following transformations have to be made.

$$x^0 = \overline{x^0} \tag{42}$$

$$x^1 = \overline{(x + \overline{x^1})^2} \tag{43}$$

$$x^2 = \overline{\overline{x^2}^2} \tag{44}$$

Verification for these transformations as well as other methods of minimization are described in reference 8.

3. Ternary Logic Implementation

Circuit realization of the ternary operators presented above using COS/MOS integrated circuits was described in reference 5. Two resistors are inserted between channels of two transistors of complementary type. The added resistors permit one to obtain three equiprobable stable voltage levels when two power supplies are used to ensure proper biasing. One of the power supplies is positive and is applied to the source of the P-channel transistor (V_{DD}) and the second one is negative and equal in magnitude to the first and is applied to the source of the N-channel transistor (V_{SS}). The three voltage levels are then equal to V_{DD} (positive), zero potential and V_{SS} (negative). This basic circuit has three outputs realizing the three types of ternary inverters (PTI, STI, and NTI). In the case of TNAND and TNOR gates, which realize the TAND and TOR operators by inserting a STI circuit in their outputs, one channel of each transistor type will be added for each additional input. For the TNAND gate the P-channel transistors will be connected in parallel and the N-channels, in series; while for the TNOR gate the P-channels, in series and the N-channels, in parallel. Based on this idea the ternary inverters, TNAND and TNOR are realized with COS/MOS integrated circuits.

The FD and RD operators are simply realized by a silicon diode with a shunt resistance connected to it. The diode in its forward direction will realize the FD operator and in its reversed direction the RD operator.

If the output D of the ternary inverter (Figure 1) is maintained at level 1 (i.e., earthed) and the output is taken from point A, the function of this circuit will be equivalent to a PTI followed by an FD circuit[14]. Let us denote this circuit by the earthed positive ternary inverter (EPTI). This also could be obtained if point B was grounded and the output was taken from point D.

Similarly, if point D is earthed and the output is taken from point B (Figure 2), the circuit will act as a NTI followed by an RD circuit. This will be denoted by the earthed negative ternary inverter (ENTI). It could also be realized if point A was grounded and the output was taken from point D.

The same idea holds for the TNAND (or TNOR) gate giving the earthed positive TNAND (or TNOR) and the earthed negative TNAND (or TNOR). Performances of these circuits are summarised in Table III.

It is obvious that using the ternary earthed circuits one may save the use of FD and RD circuits. This may provide a reduction of costs in the manufacturing process of ternary COS/MOS integrated circuits. The main disadvantage of the use of this technique is that it will not be possible to take three outputs instantaneously from the ternary circuits (e.g., A. D, and B for the PTI, STI, and NTI respectively). So, the number of elements realizing a ternary function will be higher and then the cost will be increased. To take advantage of using this technique the same steps of minimization of ternary functions described in reference 6 may be followed and the ternary earthed circuits will be used only in final steps realizing Equation (40).

4. Conclusion

A method of design of three-valued logic circuits using COS/MOS integrated circuits was presented. A system of three-valued algebra, based on operators previously defined, has been introduced and investigated. A method of logical circuitry reduction has been discussed. It has been shown how the use of diodes with COS/MOS integrated circuits is avoided. Although this reduces the manufacturing process cost and complexity, it increases the number of elements required to realize a given ternary function. An application method is suggested to take advantage of this technique.

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x	$\overline{x^0}$	$\overline{x^1}$	$\overline{x^2}$	$x^{\neg}$	$x^{\frown}$
0	2	2	2	1	0
1	0	1	2	1	1
2	0	0	0	2	1

Table I: Unary ternary operators

x	2 2 2	1 1 1	0 0 0
y	2 1 0	2 1 0	2 1 0
x + y	2 2 2	2 1 1	2 1 0
x · y	2 1 0	1 1 0	0 0 0

Table II: Multiple input ternary operators

x	$E(\overline{x^2})$	$E(\overline{x^0})$
0	2	1
1	2	0
2	1	0

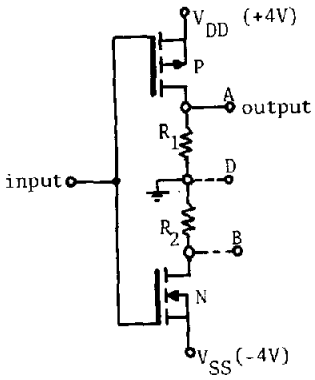
a) Earthed positive and negative inverters

Table III

x	y	$\overline{E(x \cdot y)2}$	$\overline{E(x \cdot y)0}$	$\overline{E(x+y)2}$	$\overline{E(x+y)0}$
0	0	2	1	2	1
0	1	2	1	2	0
0	2	2	1	1	0
1	0	2	1	2	0
1	1	2	0	2	0
1	2	2	0	1	0
2	0	2	1	1	0
2	1	2	0	1	0
2	2	1	0	1	0

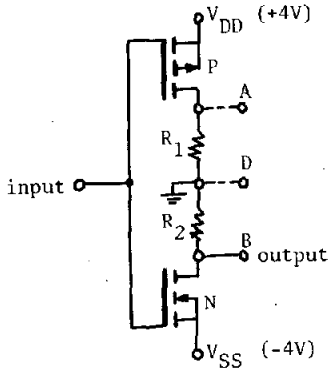
b) Earthed positive and negative TNAND and TNOR

Table III



Earthed positive ternary inverter

Figure 1



Earthed negative ternary inverter

Figure 2