```
// megafunction wizard: %ROM: 1-PORT%
// GENERATION: STANDARD
// VERSION: WM1.0
// MODULE: altsyncram

// ============================================================
// File Name: rom_B4.v
// Megafunction Name(s):
//          altsyncram
//
// Simulation Library Files(s):
//          altera_mf
// ============================================================
// ************************************************************
// THIS IS A WIZARD-GENERATED FILE. DO NOT EDIT THIS FILE!
//
// 17.0.0 Build 595 04/25/2017 SJ Lite Edition
// ************************************************************


//Copyright (C) 2017  Intel Corporation. All rights reserved.
//Your use of Intel Corporation's design tools, logic functions
//and other software and tools, and its AMPP partner logic
//functions, and any output files from any of the foregoing
//(including device programming or simulation files), and any
//associated documentation or information are expressly subject
//to the terms and conditions of the Intel Program License
//Subscription Agreement, the Intel Quartus Prime License Agreement,
//the Intel MegaCore Function License Agreement, or other
//applicable license agreement, including, without limitation,
//that your use is for the sole purpose of programming logic
//devices manufactured by Intel and sold by Intel or its
//authorized distributors.  Please refer to the applicable
//agreement for further details.


// synopsys translate_off
`timescale 1 ps / 1 ps
// synopsys translate_on
module rom_B4 (
   address,
   clock,
   q);

   input [15:0]  address;
   input   clock;
   output   [23:0]  q;
`ifndef ALTERA_RESERVED_QIS
// synopsys translate_off
`endif
   tri1    clock;
`ifndef ALTERA_RESERVED_QIS
// synopsys translate_on
`endif

   wire [23:0] sub_wire0;
   wire [23:0] q = sub_wire0[23:0];

   altsyncram  altsyncram_component (
            .address_a (address),
            .clock0 (clock),
            .q_a (sub_wire0),
            .aclr0 (1'b0),
            .aclr1 (1'b0),
            .address_b (1'b1),
            .addressstall_a (1'b0),
            .addressstall_b (1'b0),
            .byteena_a (1'b1),
            .byteena_b (1'b1),
            .clock1 (1'b1),
            .clocken0 (1'b1),
            .clocken1 (1'b1),
            .clocken2 (1'b1),
```

```
74                .clocken3 (1'b1),
75                .data_a ({24{1'b1}}),
76                .data_b (1'b1),
77                .eccstatus (),
78                .q_b (),
79                .rden_a (1'b1),
80                .rden_b (1'b1),
81                .wren_a (1'b0),
82                .wren_b (1'b0));
83        defparam
84           altsyncram_component.address_aclr_a = "NONE",
85           altsyncram_component.clock_enable_input_a = "BYPASS",
86           altsyncram_component.clock_enable_output_a = "BYPASS",
87           altsyncram_component.init_file = "note_data_B4.mif",
88           altsyncram_component.intended_device_family = "Cyclone V",
89           altsyncram_component.lpm_hint = "ENABLE_RUNTIME_MOD=NO",
90           altsyncram_component.lpm_type = "altsyncram",
91           altsyncram_component.numwords_a = 65536,
92           altsyncram_component.operation_mode = "ROM",
93           altsyncram_component.outdata_aclr_a = "NONE",
94           altsyncram_component.outdata_reg_a = "CLOCK0",
95           altsyncram_component.ram_block_type = "M10K",
96           altsyncram_component.widthad_a = 16,
97           altsyncram_component.width_a = 24,
98           altsyncram_component.width_byteena_a = 1;
99
100
101   endmodule
102
103   // ============================================================
104   // CNX file retrieval info
105   // ============================================================
106   // Retrieval info: PRIVATE: ADDRESSSTALL_A NUMERIC "0"
107   // Retrieval info: PRIVATE: AclrAddr NUMERIC "0"
108   // Retrieval info: PRIVATE: AclrByte NUMERIC "0"
109   // Retrieval info: PRIVATE: AclrOutput NUMERIC "0"
110   // Retrieval info: PRIVATE: BYTE_ENABLE NUMERIC "0"
111   // Retrieval info: PRIVATE: BYTE_SIZE NUMERIC "8"
112   // Retrieval info: PRIVATE: BlankMemory NUMERIC "0"
113   // Retrieval info: PRIVATE: CLOCK_ENABLE_INPUT_A NUMERIC "0"
114   // Retrieval info: PRIVATE: CLOCK_ENABLE_OUTPUT_A NUMERIC "0"
115   // Retrieval info: PRIVATE: Clken NUMERIC "0"
116   // Retrieval info: PRIVATE: IMPLEMENT_IN_LES NUMERIC "0"
117   // Retrieval info: PRIVATE: INIT_FILE_LAYOUT STRING "PORT_A"
118   // Retrieval info: PRIVATE: INIT_TO_SIM_X NUMERIC "0"
119   // Retrieval info: PRIVATE: INTENDED_DEVICE_FAMILY STRING "Cyclone V"
120   // Retrieval info: PRIVATE: JTAG_ENABLED NUMERIC "0"
121   // Retrieval info: PRIVATE: JTAG_ID STRING "NONE"
122   // Retrieval info: PRIVATE: MAXIMUM_DEPTH NUMERIC "0"
123   // Retrieval info: PRIVATE: MIFfilename STRING "note_data_B4.mif"
124   // Retrieval info: PRIVATE: NUMWORDS_A NUMERIC "65536"
125   // Retrieval info: PRIVATE: RAM_BLOCK_TYPE NUMERIC "2"
126   // Retrieval info: PRIVATE: RegAddr NUMERIC "1"
127   // Retrieval info: PRIVATE: RegOutput NUMERIC "1"
128   // Retrieval info: PRIVATE: SYNTH_WRAPPER_GEN_POSTFIX STRING "0"
129   // Retrieval info: PRIVATE: SingleClock NUMERIC "1"
130   // Retrieval info: PRIVATE: UseDQRAM NUMERIC "0"
131   // Retrieval info: PRIVATE: WidthAddr NUMERIC "16"
132   // Retrieval info: PRIVATE: WidthData NUMERIC "24"
133   // Retrieval info: PRIVATE: rden NUMERIC "0"
134   // Retrieval info: LIBRARY: altera_mf altera_mf.altera_mf_components.all
135   // Retrieval info: CONSTANT: ADDRESS_ACLR_A STRING "NONE"
136   // Retrieval info: CONSTANT: CLOCK_ENABLE_INPUT_A STRING "BYPASS"
137   // Retrieval info: CONSTANT: CLOCK_ENABLE_OUTPUT_A STRING "BYPASS"
138   // Retrieval info: CONSTANT: INIT_FILE STRING "note_data_B4.mif"
139   // Retrieval info: CONSTANT: INTENDED_DEVICE_FAMILY STRING "Cyclone V"
140   // Retrieval info: CONSTANT: LPM_HINT STRING "ENABLE_RUNTIME_MOD=NO"
141   // Retrieval info: CONSTANT: LPM_TYPE STRING "altsyncram"
142   // Retrieval info: CONSTANT: NUMWORDS_A NUMERIC "65536"
143   // Retrieval info: CONSTANT: OPERATION_MODE STRING "ROM"
144   // Retrieval info: CONSTANT: OUTDATA_ACLR_A STRING "NONE"
145   // Retrieval info: CONSTANT: OUTDATA_REG_A STRING "CLOCK0"
146   // Retrieval info: CONSTANT: RAM_BLOCK_TYPE STRING "M10K"
```

```
147   // Retrieval info: CONSTANT: WIDTHAD_A NUMERIC "16"
148   // Retrieval info: CONSTANT: WIDTH_A NUMERIC "24"
149   // Retrieval info: CONSTANT: WIDTH_BYTEENA_A NUMERIC "1"
150   // Retrieval info: USED_PORT: address 0 0 16 0 INPUT NODEFVAL "address[15..0]"
151   // Retrieval info: USED_PORT: clock 0 0 0 0 INPUT VCC "clock"
152   // Retrieval info: USED_PORT: q 0 0 24 0 OUTPUT NODEFVAL "q[23..0]"
153   // Retrieval info: CONNECT: @address_a 0 0 16 0 address 0 0 16 0
154   // Retrieval info: CONNECT: @clock0 0 0 0 0 clock 0 0 0 0
155   // Retrieval info: CONNECT: q 0 0 24 0 @q_a 0 0 24 0
156   // Retrieval info: GEN_FILE: TYPE_NORMAL rom_B4.v TRUE
157   // Retrieval info: GEN_FILE: TYPE_NORMAL rom_B4.inc FALSE
158   // Retrieval info: GEN_FILE: TYPE_NORMAL rom_B4.cmp FALSE
159   // Retrieval info: GEN_FILE: TYPE_NORMAL rom_B4.bsf FALSE
160   // Retrieval info: GEN_FILE: TYPE_NORMAL rom_B4_inst.v FALSE
161   // Retrieval info: GEN_FILE: TYPE_NORMAL rom_B4_bb.v TRUE
162   // Retrieval info: LIB_FILE: altera_mf
163
```