```
1   // megafunction wizard: %RAM: 2-PORT%
2   // GENERATION: STANDARD
3   // VERSION: WM1.0
4   // MODULE: altsyncram
5
6   // ============================================================
7   // File Name: ram32x4.v
8   // Megafunction Name(s):
9   //          altsyncram
10  //
11  // Simulation Library Files(s):
12  //          altera_mf
13  // ============================================================
14  // ************************************************************
15  // THIS IS A WIZARD-GENERATED FILE. DO NOT EDIT THIS FILE!
16  //
17  // 17.0.0 Build 595 04/25/2017 SJ Lite Edition
18  // ************************************************************
19
20
21  //Copyright (C) 2017  Intel Corporation. All rights reserved.
22  //Your use of Intel Corporation's design tools, logic functions
23  //and other software and tools, and its AMPP partner logic
24  //functions, and any output files from any of the foregoing
25  //(including device programming or simulation files), and any
26  //associated documentation or information are expressly subject
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29  //the Intel MegaCore Function License Agreement, or other
30  //applicable license agreement, including, without limitation,
31  //that your use is for the sole purpose of programming logic
32  //devices manufactured by Intel and sold by Intel or its
33  //authorized distributors.  Please refer to the applicable
34  //agreement for further details.
35
36
37  // synopsys translate_off
38  `timescale 1 ps / 1 ps
39  // synopsys translate_on
40  module ram32x4 (
41     clock,
42     data,
43     rdaddress,
44     wraddress,
45     wren,
46     q);
47
48     input   clock;
49     input [3:0]  data;
50     input [4:0]  rdaddress;
51     input [4:0]  wraddress;
52     input   wren;
53     output   [3:0]  q;
54  `ifndef ALTERA_RESERVED_QIS
55  // synopsys translate_off
56  `endif
57     tri1    clock;
58     tri0    wren;
59  `ifndef ALTERA_RESERVED_QIS
60  // synopsys translate_on
61  `endif
62
63     wire [3:0] sub_wire0;
64     wire [3:0] q = sub_wire0[3:0];
65
66     altsyncram  altsyncram_component (
67              .address_a (wraddress),
68              .address_b (rdaddress),
69              .clock0 (clock),
70              .data_a (data),
71              .wren_a (wren),
72              .q_b (sub_wire0),
73              .aclr0 (1'b0),
```

```
74                .aclr1 (1'b0),
75                .addressstall_a (1'b0),
76                .addressstall_b (1'b0),
77                .byteena_a (1'b1),
78                .byteena_b (1'b1),
79                .clock1 (1'b1),
80                .clocken0 (1'b1),
81                .clocken1 (1'b1),
82                .clocken2 (1'b1),
83                .clocken3 (1'b1),
84                .data_b ({4{1'b1}}),
85                .eccstatus (),
86                .q_a (),
87                .rden_a (1'b1),
88                .rden_b (1'b1),
89                .wren_b (1'b0));
90        defparam
91           altsyncram_component.address_aclr_b = "NONE",
92           altsyncram_component.address_reg_b = "CLOCK0",
93           altsyncram_component.clock_enable_input_a = "BYPASS",
94           altsyncram_component.clock_enable_input_b = "BYPASS",
95           altsyncram_component.clock_enable_output_b = "BYPASS",
96           altsyncram_component.init_file = "ram32x4.mif",
97           altsyncram_component.intended_device_family = "Cyclone V",
98           altsyncram_component.lpm_type = "altsyncram",
99           altsyncram_component.numwords_a = 32,
100          altsyncram_component.numwords_b = 32,
101          altsyncram_component.operation_mode = "DUAL_PORT",
102          altsyncram_component.outdata_aclr_b = "NONE",
103          altsyncram_component.outdata_reg_b = "CLOCK0",
104          altsyncram_component.power_up_uninitialized = "FALSE",
105          altsyncram_component.ram_block_type = "M10K",
106          altsyncram_component.read_during_write_mode_mixed_ports = "DONT_CARE",
107          altsyncram_component.widthad_a = 5,
108          altsyncram_component.widthad_b = 5,
109          altsyncram_component.width_a = 4,
110          altsyncram_component.width_b = 4,
111          altsyncram_component.width_byteena_a = 1;
112
113
114   endmodule
115
116   // ============================================================
117   // CNX file retrieval info
118   // ============================================================
119   // Retrieval info: PRIVATE: ADDRESSSTALL_A NUMERIC "0"
120   // Retrieval info: PRIVATE: ADDRESSSTALL_B NUMERIC "0"
121   // Retrieval info: PRIVATE: BYTEENA_ACLR_A NUMERIC "0"
122   // Retrieval info: PRIVATE: BYTEENA_ACLR_B NUMERIC "0"
123   // Retrieval info: PRIVATE: BYTE_ENABLE_A NUMERIC "0"
124   // Retrieval info: PRIVATE: BYTE_ENABLE_B NUMERIC "0"
125   // Retrieval info: PRIVATE: BYTE_SIZE NUMERIC "8"
126   // Retrieval info: PRIVATE: BlankMemory NUMERIC "0"
127   // Retrieval info: PRIVATE: CLOCK_ENABLE_INPUT_A NUMERIC "0"
128   // Retrieval info: PRIVATE: CLOCK_ENABLE_INPUT_B NUMERIC "0"
129   // Retrieval info: PRIVATE: CLOCK_ENABLE_OUTPUT_A NUMERIC "0"
130   // Retrieval info: PRIVATE: CLOCK_ENABLE_OUTPUT_B NUMERIC "0"
131   // Retrieval info: PRIVATE: CLRdata NUMERIC "0"
132   // Retrieval info: PRIVATE: CLRq NUMERIC "0"
133   // Retrieval info: PRIVATE: CLRrdaddress NUMERIC "0"
134   // Retrieval info: PRIVATE: CLRrren NUMERIC "0"
135   // Retrieval info: PRIVATE: CLRwraddress NUMERIC "0"
136   // Retrieval info: PRIVATE: CLRwren NUMERIC "0"
137   // Retrieval info: PRIVATE: Clock NUMERIC "0"
138   // Retrieval info: PRIVATE: Clock_A NUMERIC "0"
139   // Retrieval info: PRIVATE: Clock_B NUMERIC "0"
140   // Retrieval info: PRIVATE: IMPLEMENT_IN_LES NUMERIC "0"
141   // Retrieval info: PRIVATE: INDATA_ACLR_B NUMERIC "0"
142   // Retrieval info: PRIVATE: INDATA_REG_B NUMERIC "0"
143   // Retrieval info: PRIVATE: INIT_FILE_LAYOUT STRING "PORT_B"
144   // Retrieval info: PRIVATE: INIT_TO_SIM_X NUMERIC "0"
145   // Retrieval info: PRIVATE: INTENDED_DEVICE_FAMILY STRING "Cyclone V"
146   // Retrieval info: PRIVATE: JTAG_ENABLED NUMERIC "0"
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147   // Retrieval info: PRIVATE: JTAG_ID STRING "NONE"
148   // Retrieval info: PRIVATE: MAXIMUM_DEPTH NUMERIC "0"
149   // Retrieval info: PRIVATE: MEMSIZE NUMERIC "128"
150   // Retrieval info: PRIVATE: MEM_IN_BITS NUMERIC "0"
151   // Retrieval info: PRIVATE: MIFfilename STRING "ram32x4.mif"
152   // Retrieval info: PRIVATE: OPERATION_MODE NUMERIC "2"
153   // Retrieval info: PRIVATE: OUTDATA_ACLR_B NUMERIC "0"
154   // Retrieval info: PRIVATE: OUTDATA_REG_B NUMERIC "1"
155   // Retrieval info: PRIVATE: RAM_BLOCK_TYPE NUMERIC "2"
156   // Retrieval info: PRIVATE: READ_DURING_WRITE_MODE_MIXED_PORTS NUMERIC "2"
157   // Retrieval info: PRIVATE: READ_DURING_WRITE_MODE_PORT_A NUMERIC "3"
158   // Retrieval info: PRIVATE: READ_DURING_WRITE_MODE_PORT_B NUMERIC "3"
159   // Retrieval info: PRIVATE: REGdata NUMERIC "1"
160   // Retrieval info: PRIVATE: REGq NUMERIC "1"
161   // Retrieval info: PRIVATE: REGrdaddress NUMERIC "1"
162   // Retrieval info: PRIVATE: REGrren NUMERIC "1"
163   // Retrieval info: PRIVATE: REGwraddress NUMERIC "1"
164   // Retrieval info: PRIVATE: REGwren NUMERIC "1"
165   // Retrieval info: PRIVATE: SYNTH_WRAPPER_GEN_POSTFIX STRING "0"
166   // Retrieval info: PRIVATE: USE_DIFF_CLKEN NUMERIC "0"
167   // Retrieval info: PRIVATE: UseDPRAM NUMERIC "1"
168   // Retrieval info: PRIVATE: VarWidth NUMERIC "0"
169   // Retrieval info: PRIVATE: WIDTH_READ_A NUMERIC "4"
170   // Retrieval info: PRIVATE: WIDTH_READ_B NUMERIC "4"
171   // Retrieval info: PRIVATE: WIDTH_WRITE_A NUMERIC "4"
172   // Retrieval info: PRIVATE: WIDTH_WRITE_B NUMERIC "4"
173   // Retrieval info: PRIVATE: WRADDR_ACLR_B NUMERIC "0"
174   // Retrieval info: PRIVATE: WRADDR_REG_B NUMERIC "0"
175   // Retrieval info: PRIVATE: WRCTRL_ACLR_B NUMERIC "0"
176   // Retrieval info: PRIVATE: enable NUMERIC "0"
177   // Retrieval info: PRIVATE: rden NUMERIC "0"
178   // Retrieval info: LIBRARY: altera_mf altera_mf.altera_mf_components.all
179   // Retrieval info: CONSTANT: ADDRESS_ACLR_B STRING "NONE"
180   // Retrieval info: CONSTANT: ADDRESS_REG_B STRING "CLOCK0"
181   // Retrieval info: CONSTANT: CLOCK_ENABLE_INPUT_A STRING "BYPASS"
182   // Retrieval info: CONSTANT: CLOCK_ENABLE_INPUT_B STRING "BYPASS"
183   // Retrieval info: CONSTANT: CLOCK_ENABLE_OUTPUT_B STRING "BYPASS"
184   // Retrieval info: CONSTANT: INIT_FILE STRING "ram32x4.mif"
185   // Retrieval info: CONSTANT: INTENDED_DEVICE_FAMILY STRING "Cyclone V"
186   // Retrieval info: CONSTANT: LPM_TYPE STRING "altsyncram"
187   // Retrieval info: CONSTANT: NUMWORDS_A NUMERIC "32"
188   // Retrieval info: CONSTANT: NUMWORDS_B NUMERIC "32"
189   // Retrieval info: CONSTANT: OPERATION_MODE STRING "DUAL_PORT"
190   // Retrieval info: CONSTANT: OUTDATA_ACLR_B STRING "NONE"
191   // Retrieval info: CONSTANT: OUTDATA_REG_B STRING "CLOCK0"
192   // Retrieval info: CONSTANT: POWER_UP_UNINITIALIZED STRING "FALSE"
193   // Retrieval info: CONSTANT: RAM_BLOCK_TYPE STRING "M10K"
194   // Retrieval info: CONSTANT: READ_DURING_WRITE_MODE_MIXED_PORTS STRING "DONT_CARE"
195   // Retrieval info: CONSTANT: WIDTHAD_A NUMERIC "5"
196   // Retrieval info: CONSTANT: WIDTHAD_B NUMERIC "5"
197   // Retrieval info: CONSTANT: WIDTH_A NUMERIC "4"
198   // Retrieval info: CONSTANT: WIDTH_B NUMERIC "4"
199   // Retrieval info: CONSTANT: WIDTH_BYTEENA_A NUMERIC "1"
200   // Retrieval info: USED_PORT: clock 0 0 0 0 INPUT VCC "clock"
201   // Retrieval info: USED_PORT: data 0 0 4 0 INPUT NODEFVAL "data[3..0]"
202   // Retrieval info: USED_PORT: q 0 0 4 0 OUTPUT NODEFVAL "q[3..0]"
203   // Retrieval info: USED_PORT: rdaddress 0 0 5 0 INPUT NODEFVAL "rdaddress[4..0]"
204   // Retrieval info: USED_PORT: wraddress 0 0 5 0 INPUT NODEFVAL "wraddress[4..0]"
205   // Retrieval info: USED_PORT: wren 0 0 0 0 INPUT GND "wren"
206   // Retrieval info: CONNECT: @address_a 0 0 5 0 wraddress 0 0 5 0
207   // Retrieval info: CONNECT: @address_b 0 0 5 0 rdaddress 0 0 5 0
208   // Retrieval info: CONNECT: @clock0 0 0 0 0 clock 0 0 0 0
209   // Retrieval info: CONNECT: @data_a 0 0 4 0 data 0 0 4 0
210   // Retrieval info: CONNECT: @wren_a 0 0 0 0 wren 0 0 0 0
211   // Retrieval info: CONNECT: q 0 0 4 0 @q_b 0 0 4 0
212   // Retrieval info: GEN_FILE: TYPE_NORMAL ram32x4.v TRUE
213   // Retrieval info: GEN_FILE: TYPE_NORMAL ram32x4.inc FALSE
214   // Retrieval info: GEN_FILE: TYPE_NORMAL ram32x4.cmp FALSE
215   // Retrieval info: GEN_FILE: TYPE_NORMAL ram32x4.bsf FALSE
216   // Retrieval info: GEN_FILE: TYPE_NORMAL ram32x4_inst.v FALSE
217   // Retrieval info: GEN_FILE: TYPE_NORMAL ram32x4_bb.v TRUE
218   // Retrieval info: LIB_FILE: altera_mf
219
```