



6. Design via Root Locus

Design of cascade compensators using root locus
PI/Lag Compensator
PD/Lead Compensator
PID/Lag-Lead Compensator
Implementation of Controllers
Notch Filter

A	Improving SSE & Transient Response	ALABAMA		
	Ve can now combine the various controller types listed earlier to			
	improve both the and the	•		
	Basically, we can improve the steady state error by empl	cally, we can improve the steady state error by employing PI or		
	lag control. Then we can employ PD or lead control to in	nprove the		
	transient response.			
	 Disadvantage: the improvement in transient response yiel 	ds		
	deterioration in the improvement in steady state error wh designed first.	ich was		
	We can also improve the transient response by PD or lea	d control and		
	then improve the steady state error by PI or lag compens	sation.		
	 Disadvantage: slight decrease in the speed of the response steady state error is improved. 	when the		
	In this course, we will design for transient response first	, then we will		
	design for steady state error.			
	If we design a PD controller followed by a PI controller,	the resulting		
	compensator is called a PID controller .			
	If we design a lead compensator followed by a lag compe	ensator, the		
	resulting compensator is called a lag-lead compensate	or.		

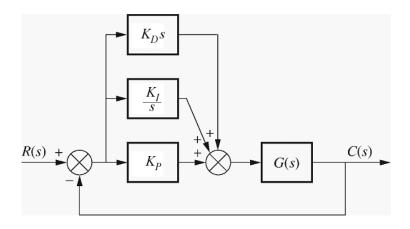


PID Controller Design



☐ It has two zeros and one pole (pole is at the origin). One zero and the pole represents the PI controller. The other zero represents the PD controller.

G_c(s) = $K_P + K_D s + \frac{K_I}{s} = \frac{K_D}{s}$



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PID Controller Design Steps



- 1. Evaluate the performance of the uncompensated (proportional) system to determine how much improvement in transient response is required. Use the root locus to do this.
- 2. Design the **PD controller** to meet the transient response specs. It includes the zero location and the loop gain.
- 3. Simulate the system to be sure all requirements have been met.
- 4. Redesign if the simulation shows that requirements have not been met.
- 5. Design **PI controller** to yield the required steady-state error.
- 6. Determine the gains K_D , K_P , and K_T .
- 7. Simulate system to be sure all requirements have been met.
- 8. Redesign if the simulation shows that requirements have not been met.



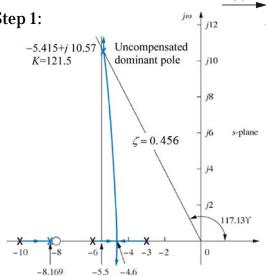
Example: PID Controller Design (1/7)



C(s)

Given the system, design a PID controller that yields a peak time of two-thirds that of the uncompensated system at 20% overshoot and with zero steady-state error for a step input.





$$M_P = 0.20 \implies \zeta = 0.456$$

 $\overline{K(s+8)}$

(s+3)(s+6)(s+10)

$$t_p =$$

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Example: PID Controller Design (2/7)

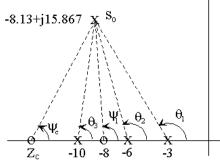


Step 2: Design the PD controller

Peak time of the new system is 2/3 of the uncompensated system.

$$\omega_d = \frac{\pi}{t_p} =$$

- Knowing the imaginary value of $\sigma + j\omega_d$ and the angle $\theta = \sin^{-1}\zeta$, we can calculate σ
- Therefore, the design point is $s_o = \sigma + j\omega_d =$
- We next find the angles between the uncompensated system's poles and zeros and the design point.



$$\angle \operatorname{Zeros} - \angle \operatorname{Poles} = (2k+1)180^{\circ}$$

 $\psi_1 + \psi_c - \theta_1 - \theta_2 - \theta_3 = (2k+1)180^{\circ}$
 $\psi_c = -\psi_1 + \theta_1 + \theta_2 + \theta_3 + (2k+1)180^{\circ}$



Example: PID Controller Design (3/7)



$$\theta_1 = -\tan^{-1}\left(\frac{15.87}{8.13 - 3}\right) + 180^\circ = -72.09^\circ + 180^\circ = 107.91^\circ$$

$$\theta_2 = -\tan^{-1}\left(\frac{15.87}{8.13 - 6}\right) + 180^\circ = -82.36^\circ + 180^\circ = 97.64^\circ$$

$$\theta_3 = \tan^{-1} \left(\frac{15.87}{10 - 8.13} \right) = 83.28^{\circ}$$

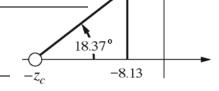
$$\psi_1 = \tan^{-1} \left(\frac{15.87}{-8.13 + 8} \right) = -89.53^{\circ} + 180^{\circ} = 90.47^{\circ}$$

$$\psi_c = -\psi_1 + \theta_1 + \theta_2 + \theta_3 + (2k+1)180^\circ$$

$$= -90.47^\circ + 107.91^\circ + 97.64^\circ + 83.28^\circ + (2k+1)180^\circ$$

$$=$$

• We can find z_c to be:



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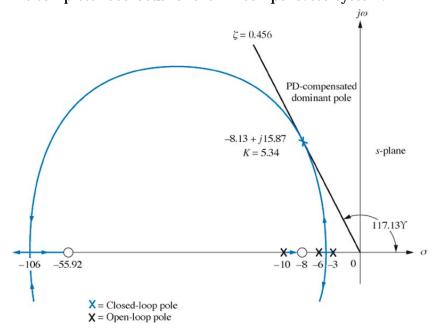
j15.87



Example: PID Controller Design (4/7)

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- Thus the PD controller is: $G_{PD}(s) =$
- The complete root locus for the PD compensated system:

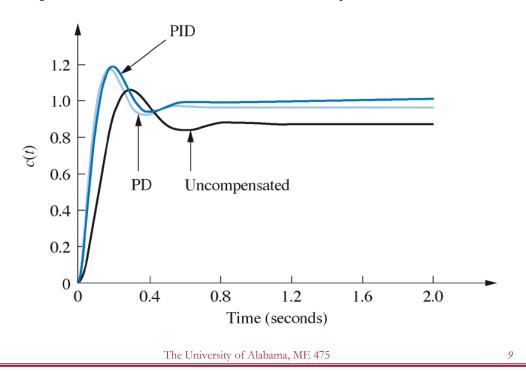




Example: PID Controller Design (5/7)

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☐ Steps 3 and 4: Simulate and check the PD system

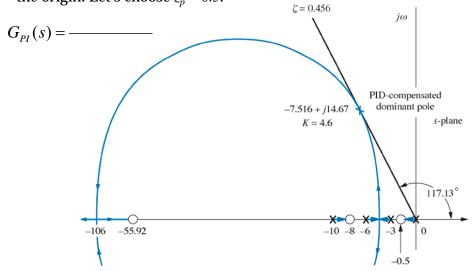




Example: PID Controller Design (6/7)

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- ☐ Steps 5: Design the PI controller
 - Any compensator zero will work as long as the zero is placed close to the origin. Let's choose $z_p = 0.5$.



From the root locus, we calculate K_d to be 4.6 (use the rlocfind(sys) in Matlab)



Example: PID Controller Design (7/7)



- \square Steps 6: Determine the gains, K_P , K_P , and K_{D^*}
 - The designed PID controller is

$$G_{PID}(s) = \frac{K_d(s+55.92)(s+0.5)}{s} = \frac{4.6(s+55.92)(s+0.5)}{s}$$

By comparing it with a standard PID controller

$$G_{PID}(s) = \frac{K_d(s^2 + 56.42s + 27.96)}{s} = \frac{K_d\left(s^2 + \frac{K_p}{K_d}s + \frac{K_I}{K_d}\right)}{s}$$

• The following controller gains are obtained:

$$K_P = \underline{\hspace{1cm}}$$
 , $K_I = \underline{\hspace{1cm}}$, $K_D = 4.6$

☐ Step 7 and 8: Simulate and redesign if necessary.

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Lag-Lead Compensator Design Steps



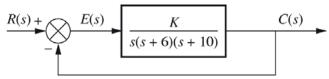
- 1. Evaluate the performance of the uncompensated (proportional) system to determine how much improvement in transient response is required. Use the root locus to do this.
- 2. Design the ______ to meet the transient response specs. It includes the zero location, pole location and the loop gain.
- 3. Simulate the system to be sure all requirements have been met.
- 4. Redesign if the simulation shows that requirements have not been met.
- 5. Evaluate the steady-state error performance for the lead-compensated system to determine how much more improvement in steady-state error is required.
- 6. Design the ______ to yield the required steady-state error.
- 7. Simulate system to be sure all requirements have been met.
- 8. Redesign if the simulation shows that requirements have not been met.



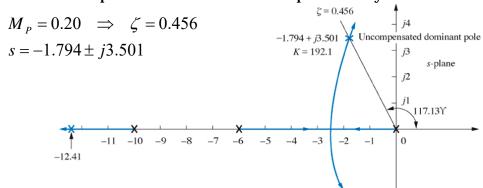
Example: Lag-Lead Compensator (1/6)



Design a lag-lead compensator for the following system so that the system will operate with 20% overshoot and a twofold reduction in settling time. Further, the compensated system will exhibit a tenfold improvement in steady-state error for a ramp input.



Step 1: Evaluate the performance of the uncompensated system.



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Example: Lag-Lead Compensator (2/6)



Step 2: Design the lead compensator

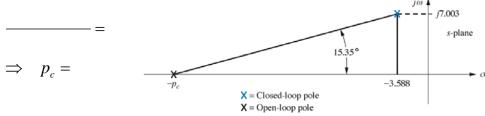
Reduction in the settling time by a factor of 2 yields

$$-\zeta\omega_n =$$

■ The imaginary part of the design point is

$$\omega_d = \zeta \omega_n \tan(117.13^\circ) = 3.588 \tan(117.13^\circ) = 7.003$$

- Arbitrarily select a location for the lead compensator zero. If we choose −6, it will eliminate one of the OL poles and leave the lead-compensated system with three poles.
- Find the location of the compensator pole. By calculation, the sum of all the angular contributions from the OL system poles and zeros and the compensator zero becomes −164.65°. The required angle from the compensator pole is 15.35°.





Example: Lag-Lead Compensator (3/6)



- Steps 3 and 4: Check the design with a simulation
- Step 5: Evaluate the steady-state error performance
 - The uncompensated system's OL transfer function

$$G(s) = \frac{192.1}{s(s+6)(s+10)} \implies K_{\nu} = \underline{\hspace{1cm}}$$

The OL transfer function of the lead-compensated system

$$G_{LC}(s) = \frac{1977}{s(s+10)(s+29.1)} \implies K_{v} = \underline{\hspace{1cm}}$$

Thus, the addition of lead compensation has improved the steady-state error by a factor of 2.122. Since the requirements of the problem specified a tenfold improvement, a lag compensator must be designed to improve the steady-state error by a factor of 4.713 (10/2.122 = 4.713) over the lead-compensated system.

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Example: Lag-Lead Compensator (4/6)

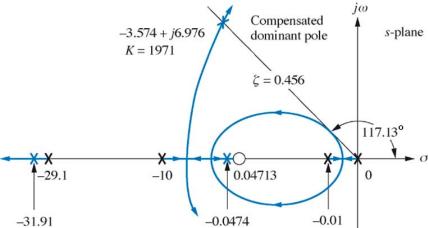
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- Steps 6: Design the lag compensator
 - Arbitrarily choose the lag compensator pole at 0.01, which then places the lag compensator zero at 0.04713.

$$G_{lag}(s) = \frac{(}{}()$$
 $G_{LLC}(s) = \frac{K(s+0.04713)}{s(s+10)(s+29.1)(s+0.01)}$

Lag compensator

OL TF for the lag-lead compensated system





Example: Lag-Lead Compensator (5/6)



	Uncompensated	Lead-compensated	Lag-lead-compensated
Plant and compensator	<u>K</u> s(s+6)(s+10)	K s(s+10)(s+29.1)	K(s+0.04713) s(s+10)(s+29.1)(s+0.01)
Dominant poles	$-1.794 \pm j3.501$	$-3.588 \pm j7.003$	$-3.574 \pm j6.976$
K	192.1	1977	1971
ζ	0.456	0.456	0.456
ω_n	3.934	7.869	7.838
% overshoot	20	20	20
t_s	2.230	1.115	1.119
t_p	0.897	0.449	0.450
K_{v}	3.202	6.794	31.92
$e(\infty)$	0.312	0.147	0.0313
Third pole	-12.41	-31.92	-31.91, -0.0474,
Zero	None	None	-0.04713
Comments	2 nd order approx OK	2 nd order approx OK	2 nd order approx OK

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Example: Lag-Lead Compensator (6/6)

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Steps 7: Simulate the system to check all requirements

