Review of Logic circuits.

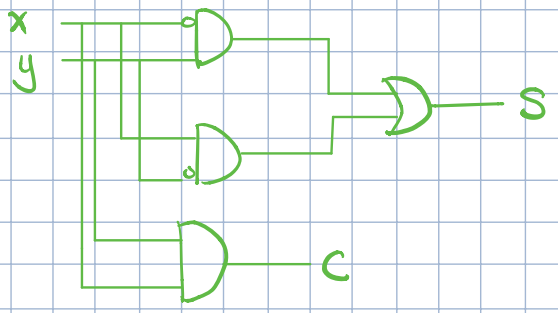
Truth Table: specifies the output value of a logic function for all valuations of its inputs.

eg. 2-bit adder. CS = x+y ("add")

x y	CS
0 0	00
0 1	01
1 0	01
1 1	10

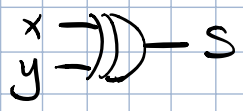
$C = x \cdot y$

$S = \bar{x}y + x\bar{y}$



Recall: the logic function $\bar{x}y + x\bar{y}$ is often useful, so it has its own symbol and name. "exclusive-OR". Thus,

$$S = \bar{x}y + x\bar{y} = x \oplus y$$



Example: 3 bit adder.

C_i	x	y	C_o	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

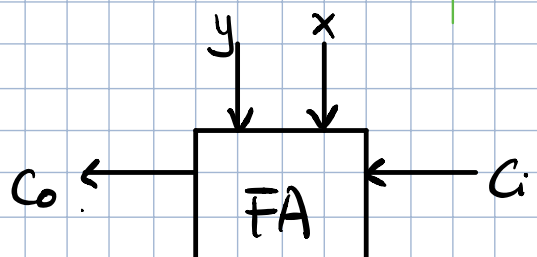
$$C_o = \bar{C}_i xy + C_i \bar{x}y + C_i x\bar{y} + C_i xy$$

(combine. / combine. / combine.)

$$= xy + C_i y + C_i x$$

$$S = \bar{C}_i \bar{x} y + \bar{C}_i x \bar{y} + C_i \bar{x} \bar{y} + C_i x y$$

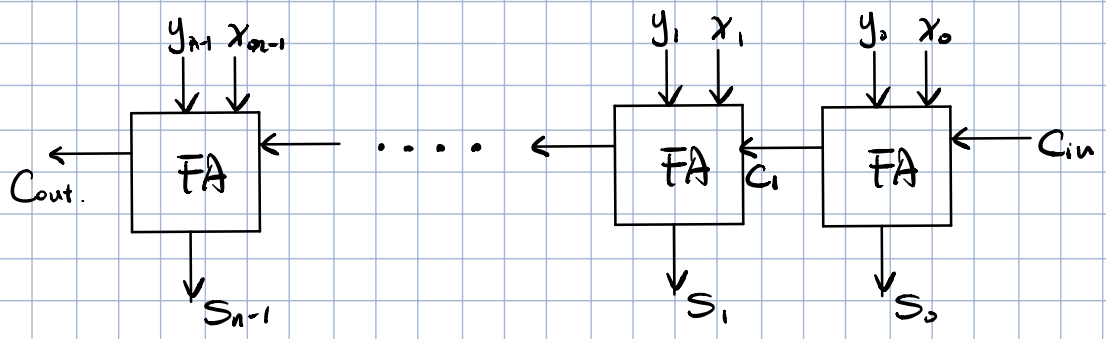
$$= C_i \oplus x \oplus y$$



S

Multibit Adder : $CS = X + Y + C_i$, $X = X_{n-1} \cdots X_1 X_0$

$Y = Y_{n-1} \cdots Y_1 Y_0$



Example. (Verilog Code)

```
module addern (Cin, X, Y, Cout, S);
    parameter n=16;
    input Cin
    input [n-1:0] X,Y;
    output Cout;
    output [n-1:0] S;
    assign {Cout, S} = X+Y+Cin;
endmodule.
```

{....} concatenate operator

"+" means add.

"|" means OR.

miscellaneous circuits.

multiplexer: choose an output from multiple inputs based on a select input (s)

2-to-1 mux:

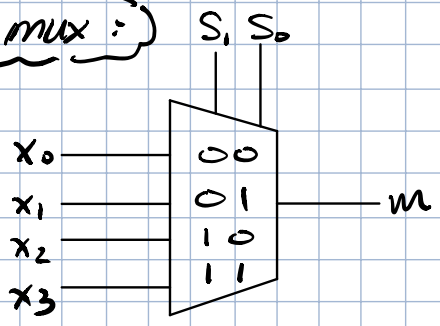
S	x_0	x_1	m
0	0	0	0

S	m
0	x_0
1	x_1

0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

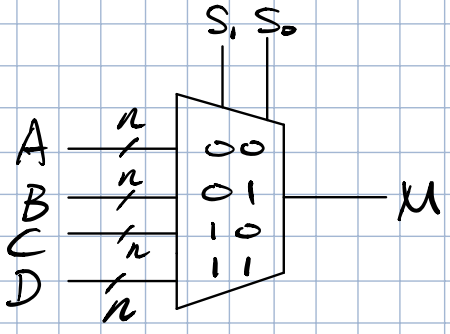
x_0 x_1

4-to-1 mux:



S_1 S_0	m
0 0	x_0
0 1	x_1
1 0	x_2
1 1	x_3

n-bit 4-to-1 mux:



S_1 S_0	M
0 0	A
0 1	B
1 0	C
1 1	D

Verilog Code

```
module nbit-4to1 (A, B, C, D, S, M);
    parameter n=16;
    input [n-1:0] A, B, C, D;
    input [1:0] S;
    output [n-1:0] reg M;
    always @ ( * )
    begin.
        if (S==0) M=A;
        else if (S==1) M=B;
```

Required b/c M is assigned a value in a always block.

```
        else if (s==2) M=C;
        else M=D;
    end.
endmodule.
```

Storage Element

Latch