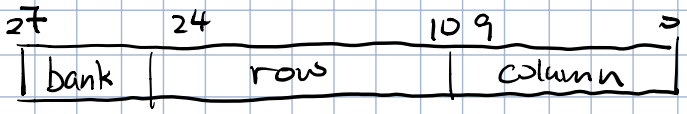
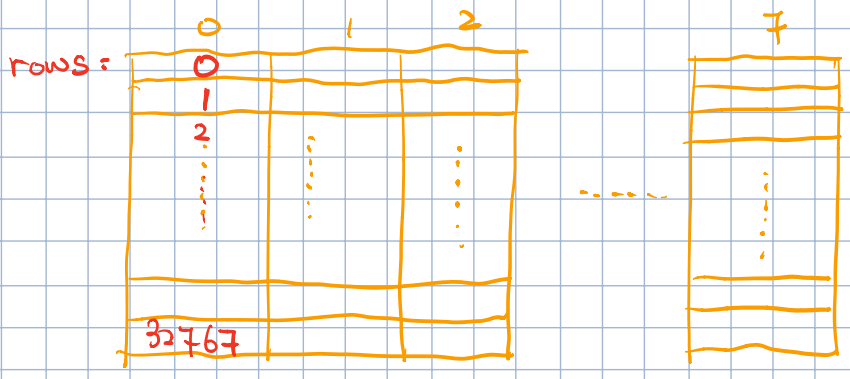
from last lec.

- Address inputs: 15 (row) + 10 (column) + 3 (bank) = 28

Two choices:

BRC





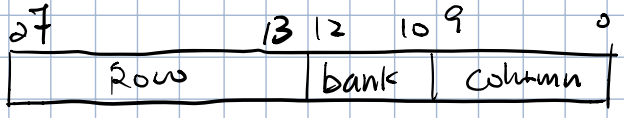
Bank Row lok column.

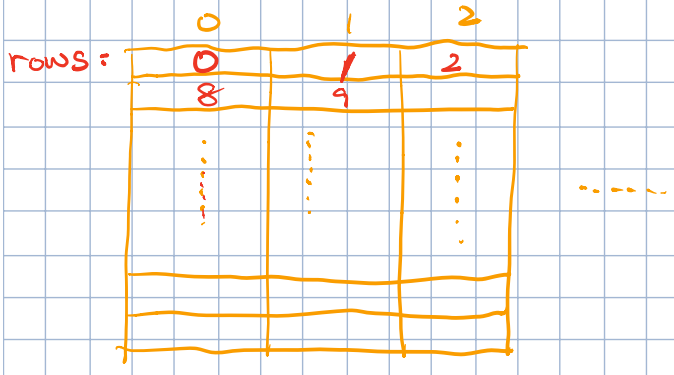
000 00.... 0 0000000000

000 00..... 0 1111111111

000 00 ... 1 0000000000

RBC:





row bank col.

000 ... 0 000 0000000000

000 ... 0 000 1111111111

000 ... 0 001 0000000000

- It is better to use all banks of the memory beenz it allows some operations to be down in parallel

* Refresh: Every storage cell has to be read periodically to avoid losing its stored charge (voltage). This is called refresh. Also, banks can be accessed in parallel for "activate", refresh, read/write.

- A DDR controller is required btw processor and the DDR

Given a 28-bit address A_{27-0}:

1. Activate a bank using BA_{2-0}
2. Send A_{27-13} to pins A_{14-0} on DDR the $\overline{RAS}$ input (row address strobe)
3. Send A_{9-0} to pins A_{9-0} on DDR. Pulse the $\overline{CAS}$ input (column address strobe)
4. The DDR provides 16 bit data (*)
5. If writing data, use UDM and LDM to choose which bytes to write (upper, lower data mask)

(*) **Note**: the DDR is slow to provide the First Column Accessed. But the column address can now be increamented to get the next column. A new 16-bit column data can be output each clock cycle.

Cache memory

- A cache is a small, fast memory (SRAM) that sits between ARM and the DDR port.