MT Review.

Topics: - information representation (binary, hex, 2's complement, ASCII)

- logic circuits and verilog code, modelsim.
- Computer organization: processor, memory, I/O ports, buses
- Processor Architecture.: registers, adder/subtractor/logic, bus mux
- Lab 1/2 processor.: instruction encoding (oooooooIIIXXXYYY);

  mv, mvi, add, sub, ld, str., mvnz, mvnc.

  instruction execution over multiple clock cycles
- memory, address decoding, memory-mapped I/O
- Assembly language code: read/write memory (or I/O devices), add/sub, branching, subroutines, the need for temporary storage (stack)
- Enhanced processor.: registers r0 - r6, r7 (PC), flags (Z, C)

  word addressable
- ARM processor: registers R0 - R12 (general purpose), R13 (stack pt.)

  R14 (link register), R15 (PC), CPSR (flags: N, V, Z, C)

  byte addressable, "Little endian". (V: overflow)
- Load/Store architecture, Addressing modes:

  [Rn] [Rn, #offset] [Rn], #offset ...
- conditional execution (branches, & others)
- LDR, LDRB, STR, STRB, ... MOV(S), ADD(S), SUB(S), ...

  AND, OR, EOR, B, ..., BL, LSL, LSR, ASR, ROR, PUSH, POP
- Loading constants with MOV r0, #D, and LDR R0, =D

Information Representation.

- convert $(624)_{10}$ to binary and hex.

$$624 = 512 + 64 + 32 + 16 = 2^9 + 2^6 + 2^5 + 2^4$$

624
512
112
64
48
32
16

$624 = (1001110000)_2$

$=$

$(270)_{16}$

- convert $-(624)_{10} = (\quad)_2 = (\quad)_{16}$

$(624)_{10} = (0100111000)_2 \Rightarrow (1011000000)_2$

to -ve

1 101

$(D90)_{16}$

put a sign bit at the front.

(1101 = D)

Enhanced Processor Architecture. (Instructions: 0000000 IIIXXYYY)

refer notes.

- write a main program and subroutine equivalent to:

```
int FINDSum (int N){
    int sum=0;
    while (N!=0){
        sum += N;
        --N;
    }
}
```