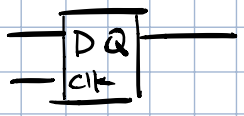
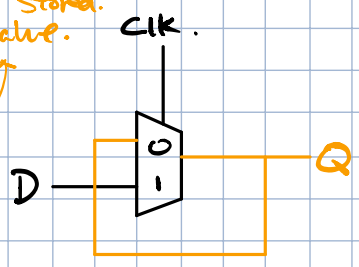
Storage Element.

Latch



Clk	D	Q
0	0	0/1
0	1	0/1
1	0	0
1	1	1

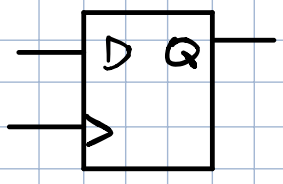
prev. stored value.



operation: if Clk=1, Q=D, But when Clk=0. the feedback loop stores the value that D was when clk was 1.

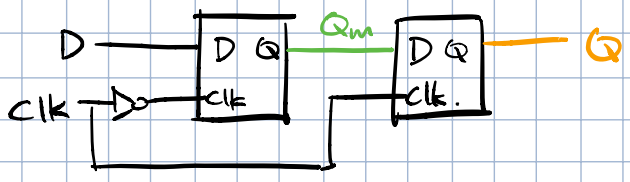
Flip-Flop :

circuit that stores a value on the edge of a clock signal.

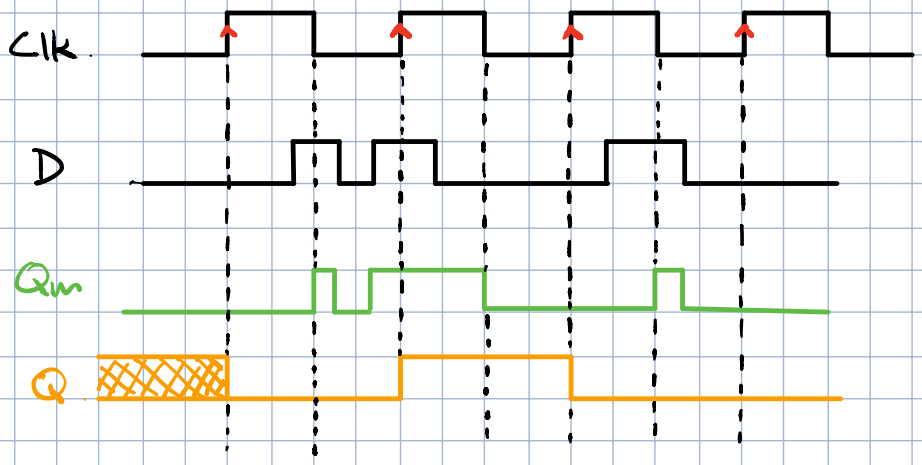


Clk	Q
0	0/1
1	0/1
↑	D

stored value



Timing Diagram.

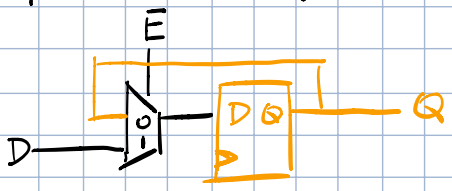


Note: We do not need to look at Qm to draw the waveform for Qs because the FF simply stores the value of D at the movement when clock ↑

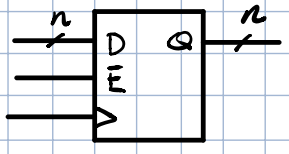
Flip Flop w/ Enable.

if E=0, Q can't change.

if E=1. the flip-flop works normally.

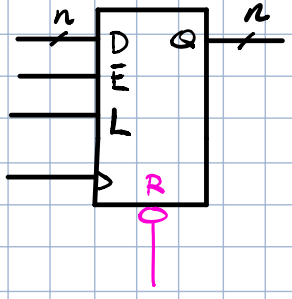


N-bit register.

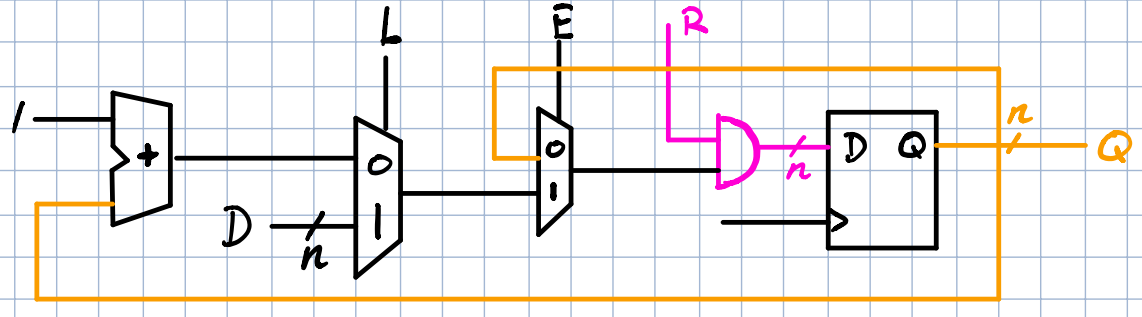


- comprises n FFs in parallel.
- if E=1, when on ↑ clock edge. Store the n-bit value of D in the register.
- if E=0. the data cannot change.

n-bit counter.



- if R=0, then on an ↑ clock Q=0
- if E=1,
  - if L=1, then on ↑ clock edge. Q=D
  - else if L=0, then on ↑ clock edge, Q=Q+1
- Else if E=0,
  - Q cannot change.



Verilog.

```
module counter (L, E, R, D, clock, Q);
    parameter n=16;
    input L, E, R, clock;
    input [n-1:0] D;
```

```
output reg. [n-1:0] Q;
always @ (posedge clock)
    if (R==0)  Q<=0;
    else if (E==1)
        if (L==1)  Q<=D;
        else  Q<=Q+1;
endmodule.
```

use <= for FFs
use = otherwise.
(non-blocking vs. blocking assign.)

Design Example:

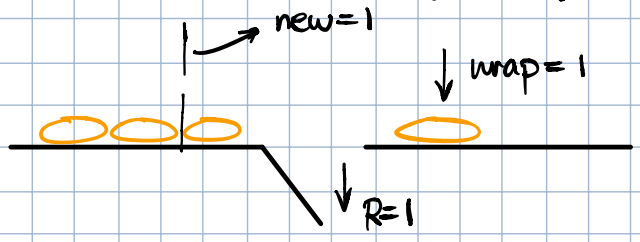
A factory bakes cookies that move down a conveyer belt. There are 3 sensors examine each cookie:

S_0: gives 1 iff a cookie is burned.

S_1: gives 1 iff a cookie is too light in weight.

S_2: gives 1 iff a cookie is not rounded.

- A logic function $R=1$ rejects only cookie for which two or more sensors produce 1. Cookies not rejected get wrapped.



- Design a finite state machine (controller) that does the following. synchronized by a clock signal: