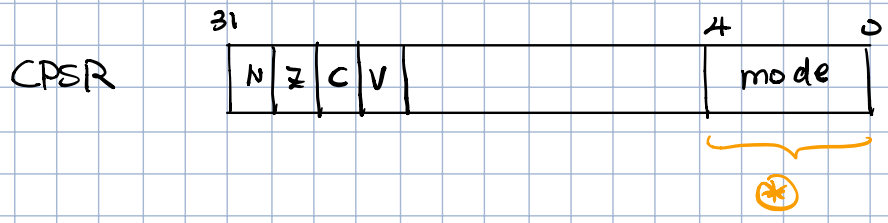
# Processor modes of operation.




| * operating mode. | CPSR 4-0 |
|---|---|
| supervisor (SVC) | 10011 |
| undefined. | 11011 |
| user | 10000 |
| Abort | 10111 |
| IRQ | 10010 |
| FIQ | 10001 |

SVC: this is the mode entered by ARM on power-up or reset
It's normally used for a operating system. (e.g. Linux)

user: places some restrictions on programs (used for non-OS code)

Abort: entered when an error occurrs

IRQ: used for interrupt-driven I/O (lab 6)

Note: Each mode has its own R13 (SP) and R14 (LR) This concept is called "banked" registers. Also, each mode has its own CPSR & a saved CPSR (SPSR)

```
.text
.global _start.

_start: mov  R0,#0b10111  // Abort mode bits
        MSR  CPSR, R0     // enter abort mode.
        LDR  SP, =0x80000 // set SP
        mov  R0, 0b10011  // SVC mode bits
        MSR  CPSR, R0
        LDR  SP, =0x3FFFFFFC
```

not the same register.

The processor automatically changes modes when an exception occurs

1. Processor reset (SVC mode)
2. Unimplemented Instruction (undefined)
3. Processor error (Abort mode)
4. Software Int (SVC instruction) (SVC mode)
5. Hardware Interrupt (IRQ mode)

- When an exception occurs, the processor:
  - saves CPSR in the SPSR of the new mode
  - changes CPSR to enter the new mode
  - saves PC into the banked LR of the new mode
  - load into PC a unique address associated with the new model. These Addresses are called the Exception vector Table:

Address:

0 — Reset exception vector. (Branch to _start)

4 — unimplemented instruction. ( B to code for this exception )

8. — SVC instructions ( B to OS code (system_call)

C — Instruction Abort ( B to code to handle the error)

10 — Data abort. ( B " " " " " "

14 — Not used.

18 — interrupt handler. ( B to IRQ_HANDLR