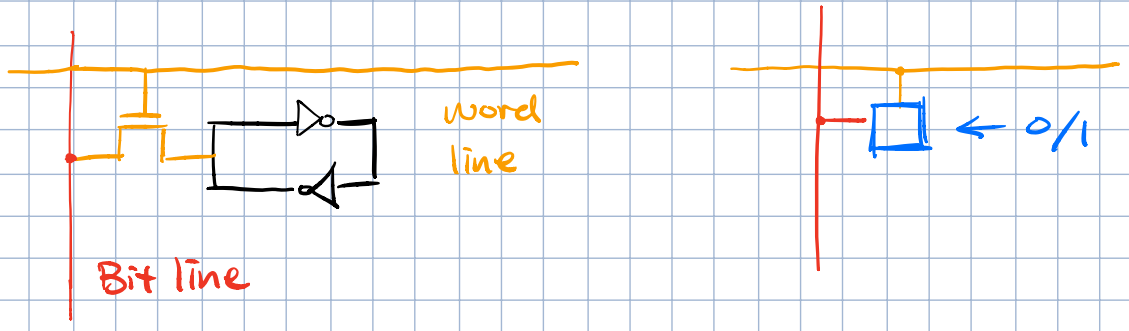
memory technology

-you have now used a # of memories: Onchip, sDRAM, DDR. The design of memory devices is complex. (especially true for DDR memory)

Onchip memory:

-is an example of static random access memory. (SRAM)

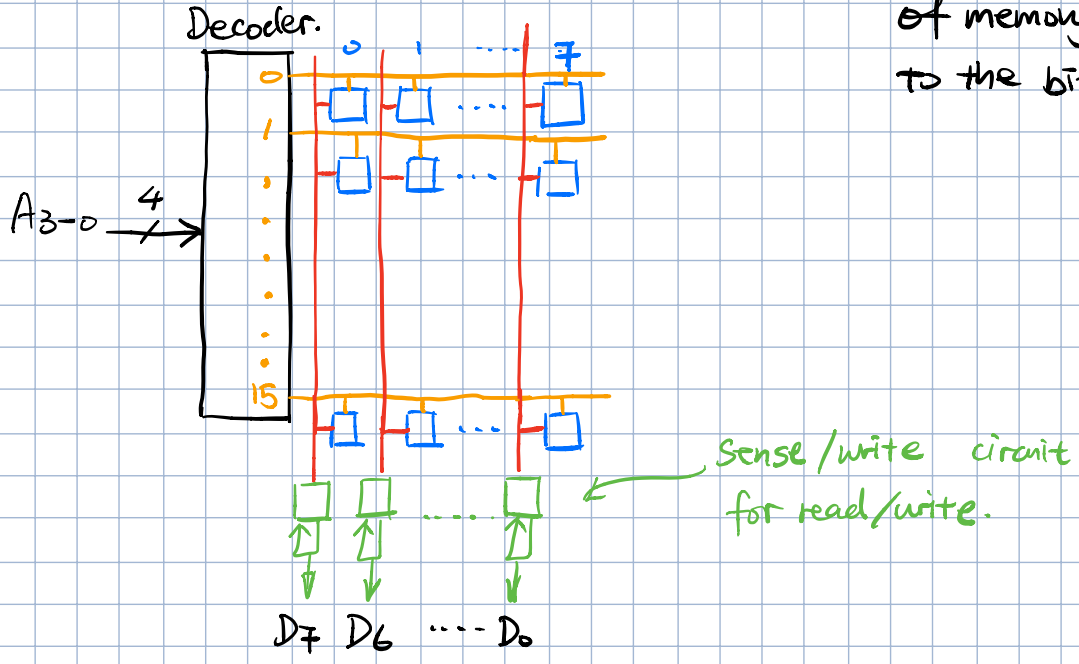
Storage cell:



example:

16×8 SRAM

Summary: The address activate one of the word line. This row of memory cells is then connected to the bit lines.



-Now consider a larger 2M×8 SRAM. Obviously it can't be built as one column. chips have to ~square. 2M×8 storage cells. 2M×8 = 16M cells

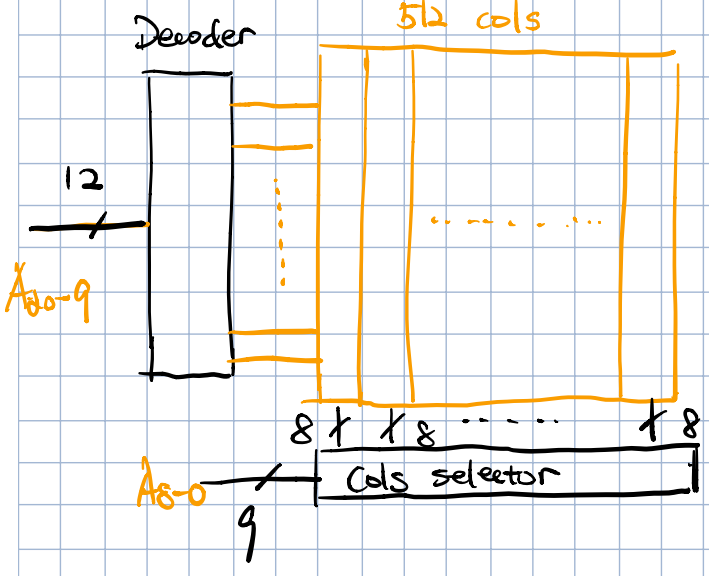
$2M = 2^1 \times 2^{20} = 2^{21}$ address $= 4k \times 4k$

lines.

4k

8 8 8

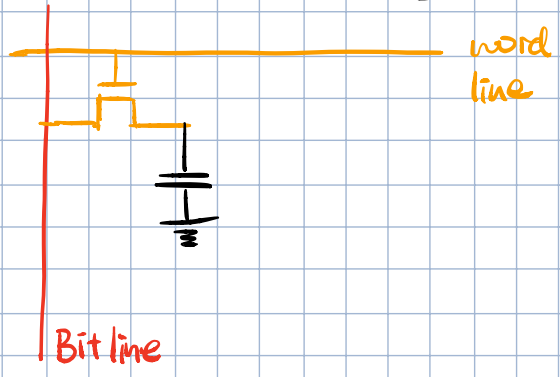
# of columns = 4k / 8 = 512



SDRAM and DDR

- these are examples of dynamic memory.

Storage cell:



- Since the storage cell is very small, then large capacity memorys can be built.
- the capacitor will gradually lose its charge if storing a "1". To avoid this loss, the cell has to be accessed periodically (refresh)

example: 1GB DDR3 on the DE1-SoC board is implemented using two chips from ISSI called IS43TR16256A (256M rows, 16 bits per row)

- consider 1 of these chips: 256M x 16bits = 4Gbits storage
- The chip must ~ square.

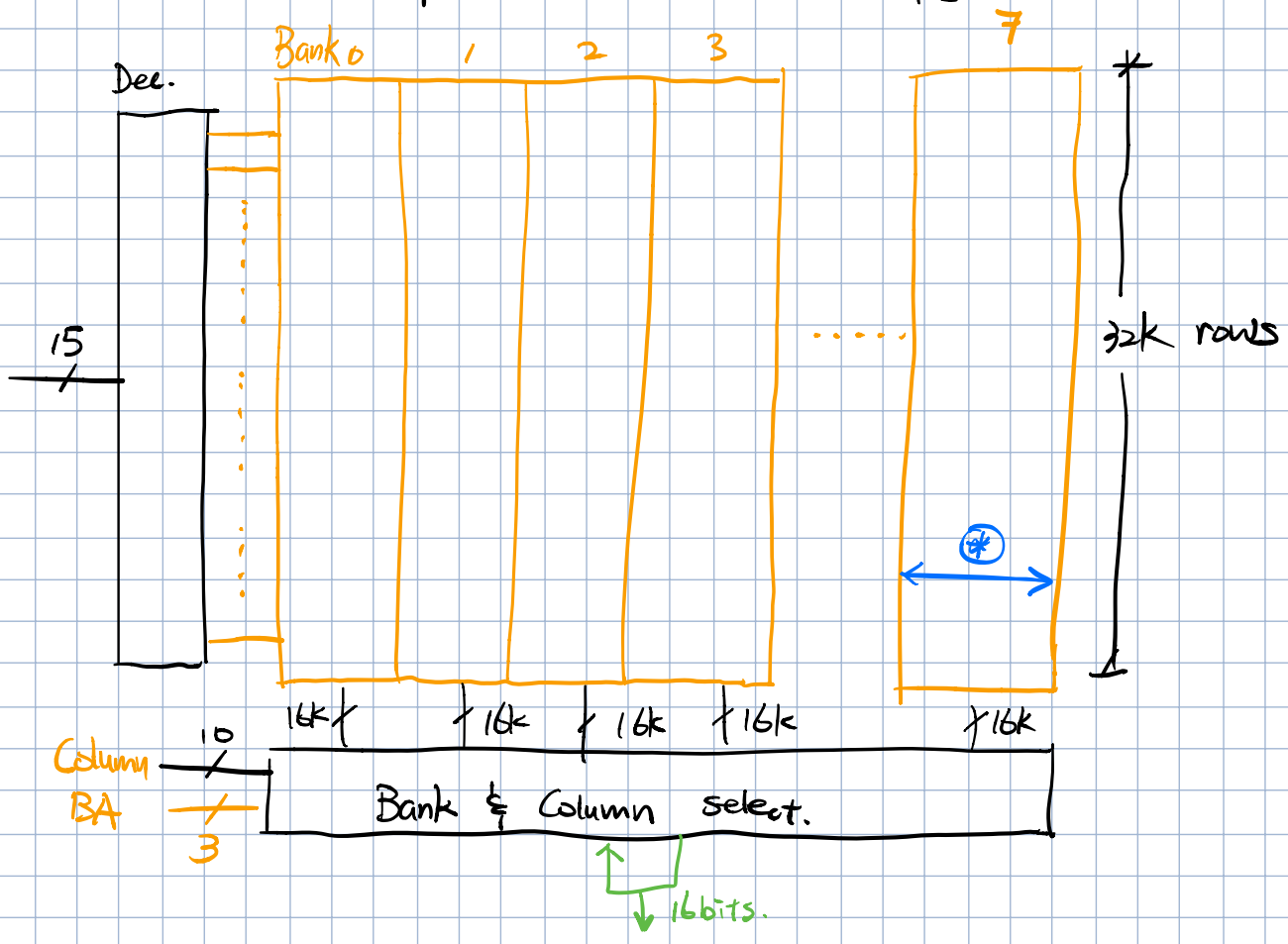
Note: $256M = 2^8 \times 2^{20} = 28$ address input.

- There are actually A_{14-0} address inputs on the package;

These are shared for row and column address.

- There are also three bank addr. BA 2-0

- There are 15 address inputs called A_{14-0}; this implys



* 1k columns / bank with 16 bits in each column.
(10 column address bits)

Note: 4Gbits / 32k rows

= 128 k bits / row ÷ 16 = 8k columns / row

= 1 k columns / bank.