

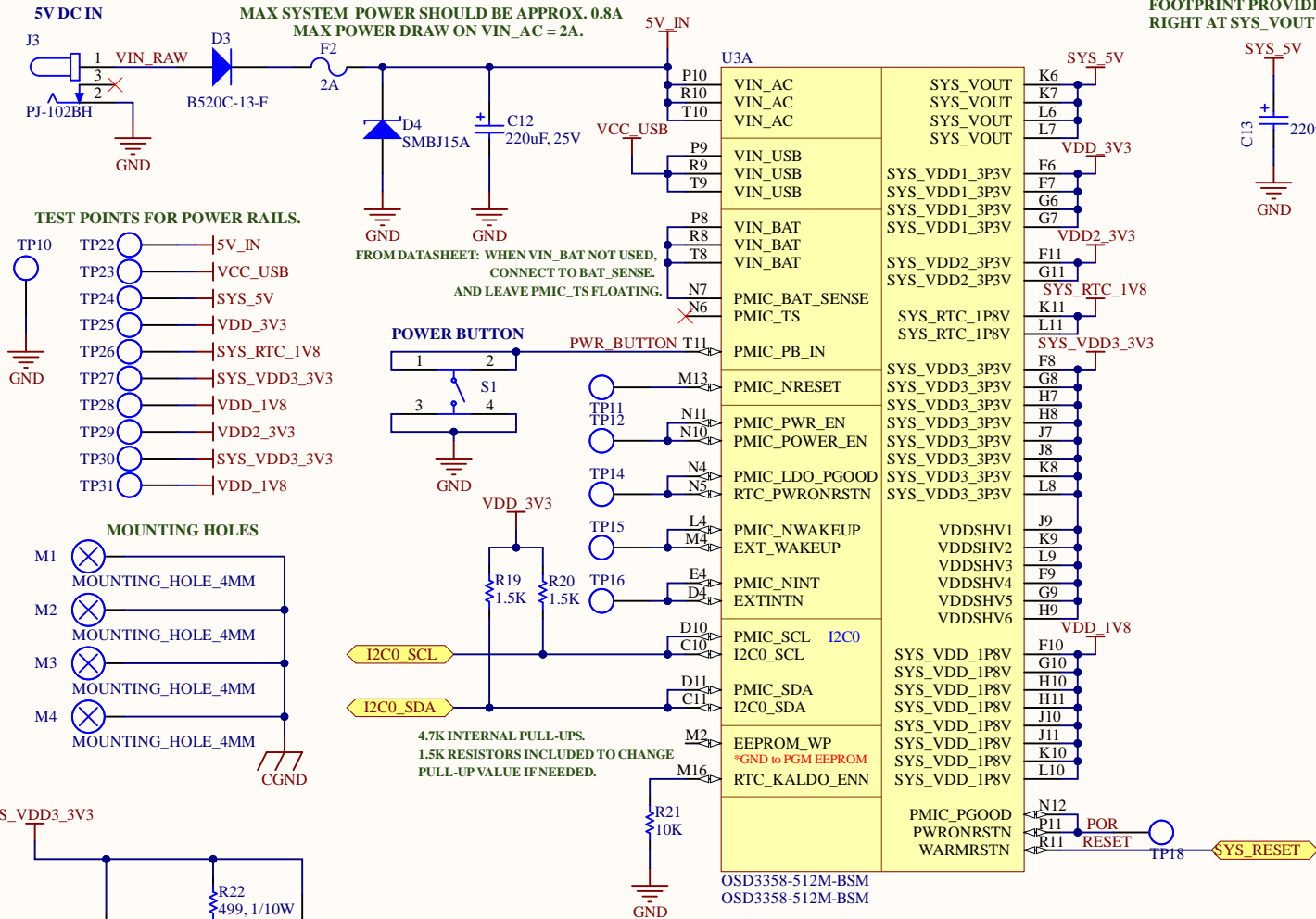
SOM_POWER: POWER CONNECTIONS AND TEST POINTS.

**CONNECT CGND AND GND THROUGH 1206 FOOTPRINT
NEAR BARREL JACK CONNECTION.**

INPUT POWER FROM EXTERNAL POWER SUPPLY.

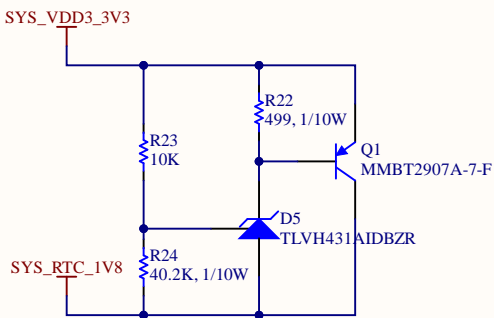
MAX SYSTEM POWER SHOULD BE APPROX. 0.8A
MAX POWER DRAW ON VIN_AC = 2A.

**SYS_VOUT MINIMUM 50uF BULK CAPACITANCE
220uF PLACED NEAR USB HUB.
FOOTPRINT PROVIDED FOR ANOTHER 220uF CAP
RIGHT AT SYS_VOUT OUTPUT.**

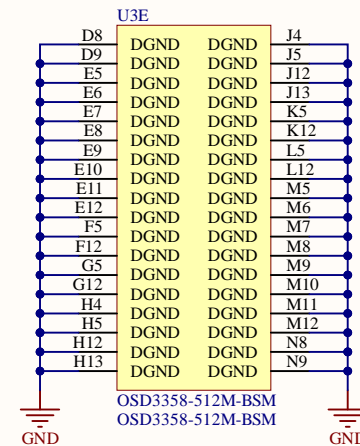
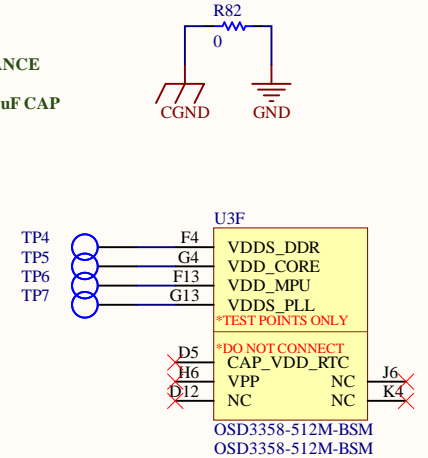
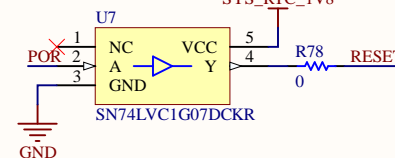
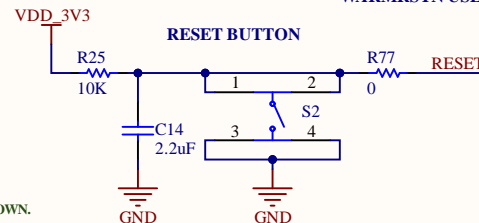


WARMRSTN USE CASE #2 ON OCTAVO DESIGN GUIDE.

POWER ON RESET ELECTRONIC CONTROL

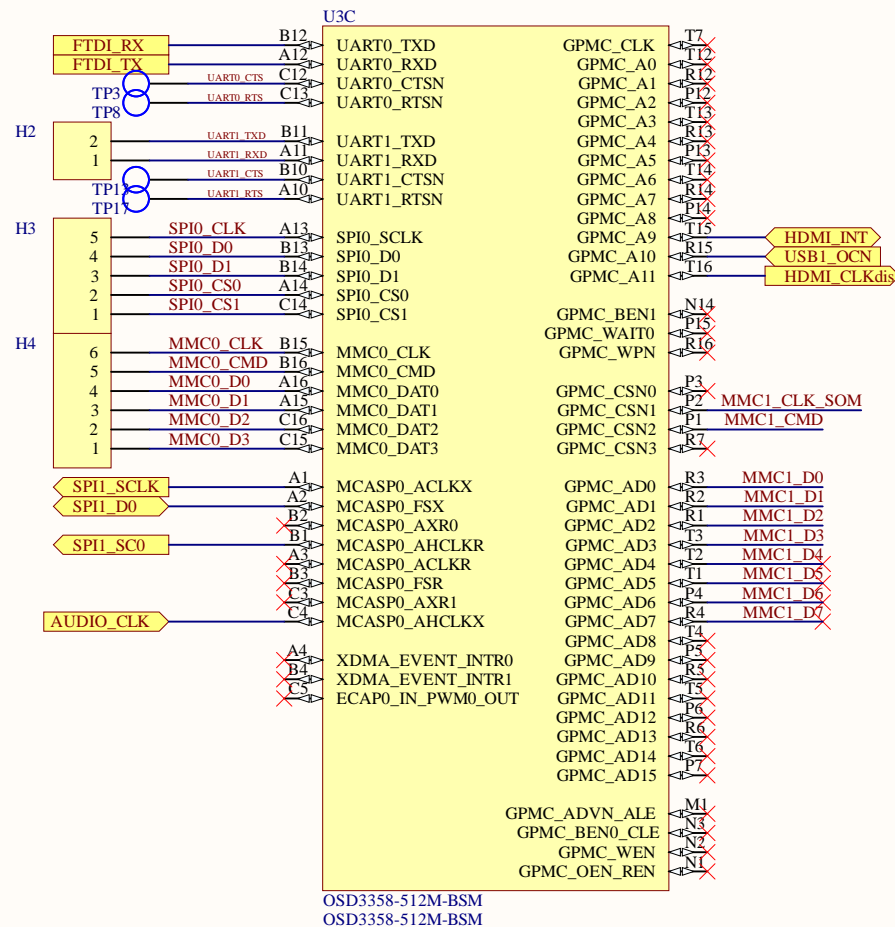


**CLAMPING CIRCUIT IN ORDER TO MAINTAIN 1.55V
DIFFERENCE BETWEEN VDD3_3V3 AND RTC_1V8 RAILS DURING POWER DOWN.**

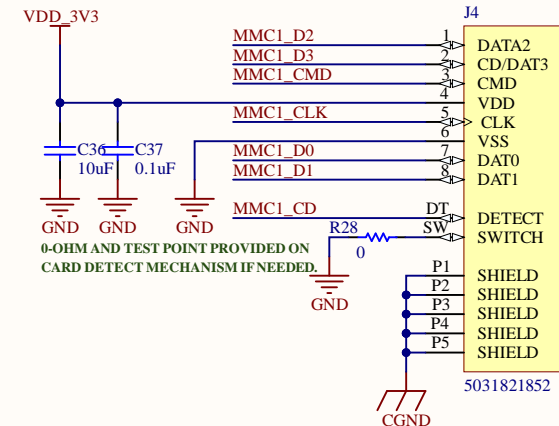


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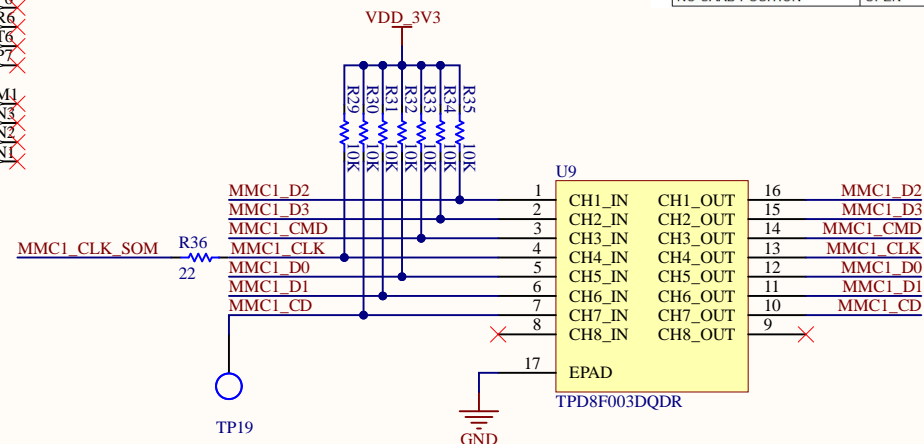
SOM_IO1: UART, SPI, MMC, GPIO, ETC.



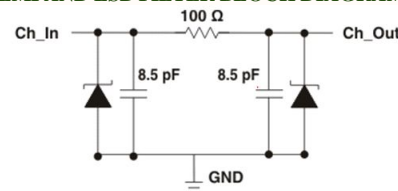
MMC1 SD CARD STORAGE FOR LINUX IMAGE BOOT.



DETECT SWITCH	
カード挿入時	クローズ
CARD INSERTING POSITION	CLOSED
カード未挿入時	オープン
NO CARD POSITION	OPEN



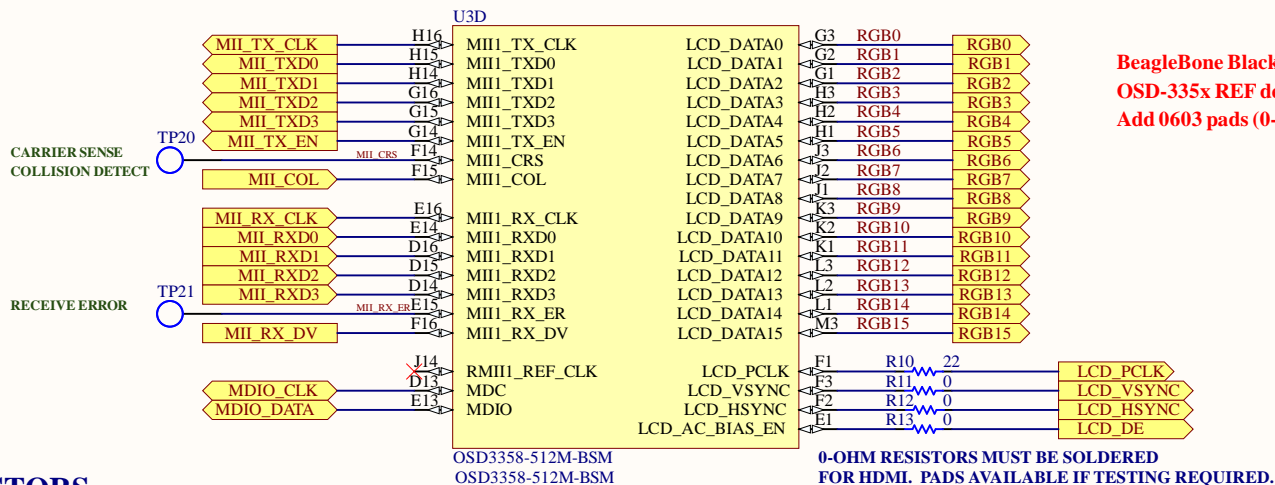
EMI AND ESD FILTER BLOCK DIAGRAM



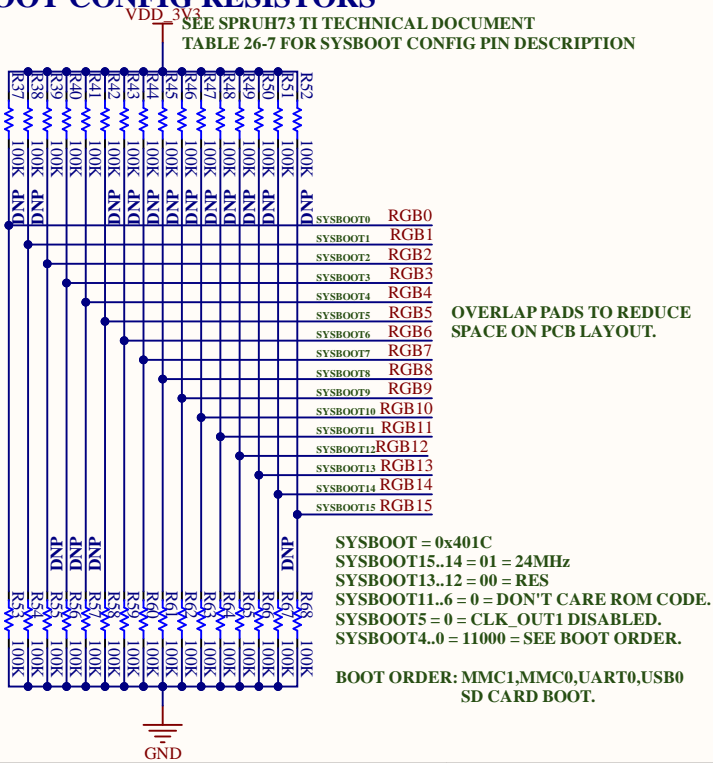
12kV ESD PROTECTION (CONTACT)
25dB @ 1GHz FILTER FOR EMI
CUT-OFF FREQUENCY @ 200MHz

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File:	C:\Users\...\SOM_IO1.SchDoc	Drawn By:

SOM_IO2: ETHERNET AND HDMI.



BOOT CONFIG RESISTORS

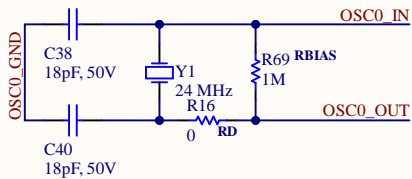


BeagleBone Black Ref design uses 33-ohm resistors in series for each line.
OSD-335x REF design uses none.
Add 0603 pads (0-ohm) for safety?

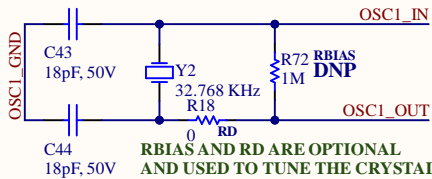
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Date:	2-15-2020	Sheet of
File:	C:\Users\...\SOM_IO2.SchDoc	Drawn By:

SOM_IO3: CLOCK CRYSTALS, JTAG, USB PORTS, AND ANALOG.

MAIN CLOCK OSCILLATOR



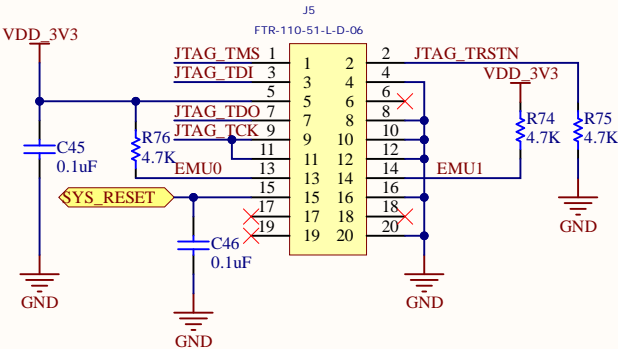
RTC OSCILLATOR



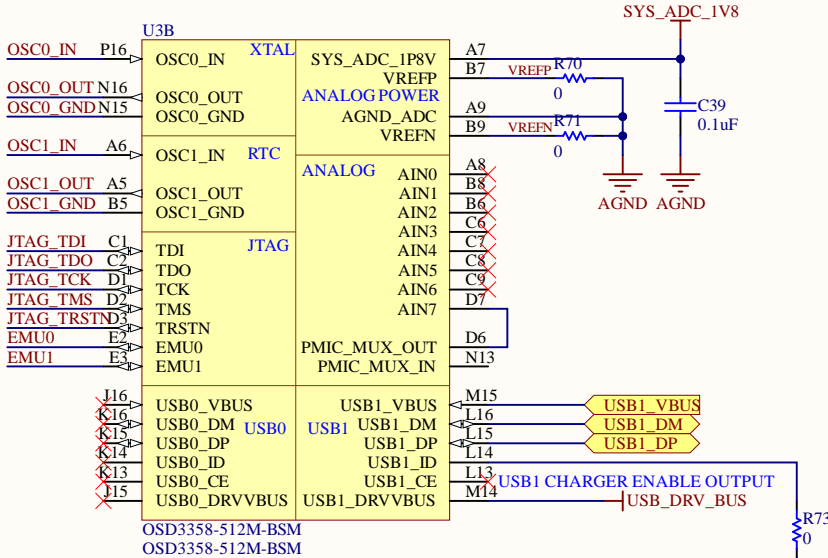
RBIAS AND RD ARE OPTIONAL
AND USED TO TUNE THE CRYSTALS.
RD = 0-OHM BY DEFAULT.
RBIAS = DNP BY DEFAULT.

SEE AM335x DATASHEET Tables 6.2 AND 6.5 FOR CRYSTAL REQUIREMENTS.

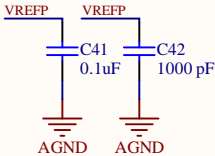
JTAG DEBUG PORT



ADVANCED JTAG FEATURES NOT SUPPORTED
EMU2, EMU3, AND EMU4 NOT CONNECTED.



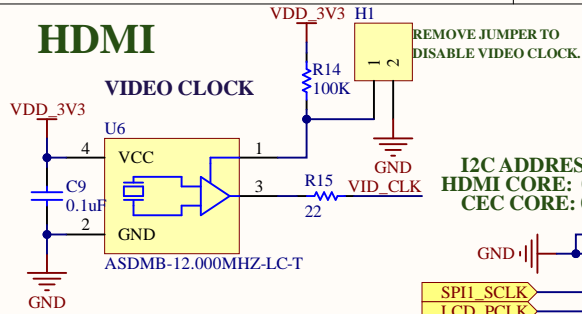
ANALOG REFERENCE DECOUPLING CAPACITORS



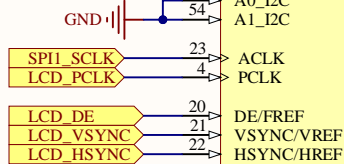
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Date:	2-15-2020	Sheet of
File:	C:\Users\...\SOM_IO3.SchDoc	Drawn By:

HDMI

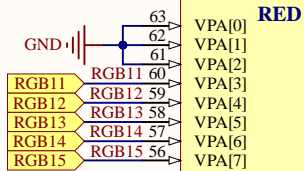
VIDEO CLOCK



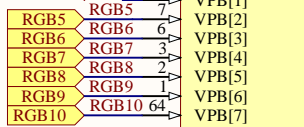
I2C ADDRESSES
HDMI CORE: 0x70
CEC CORE: 0x68



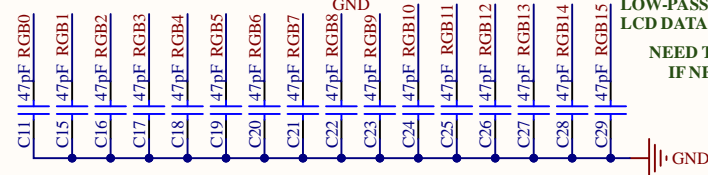
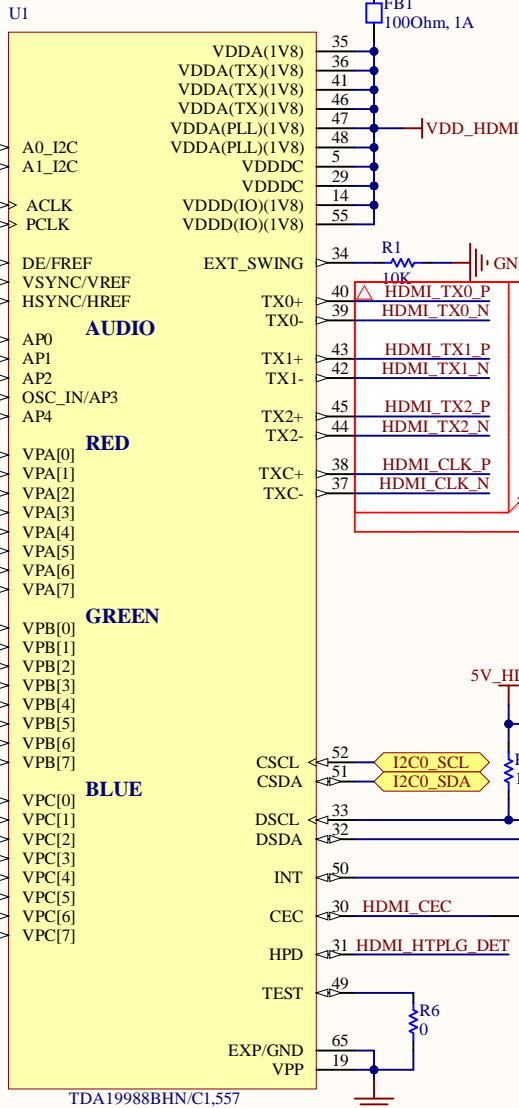
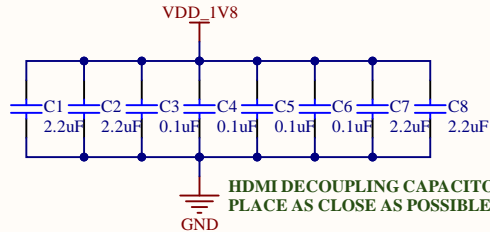
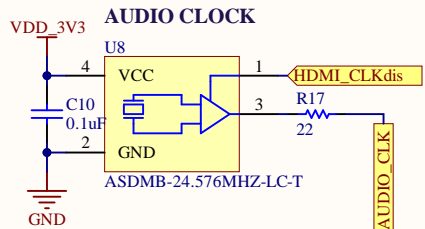
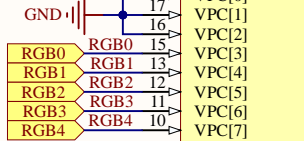
AUDIO



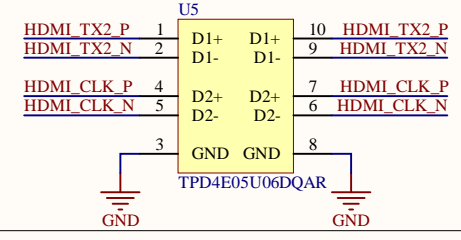
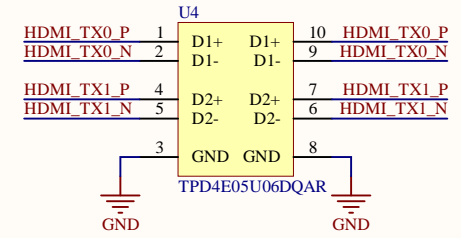
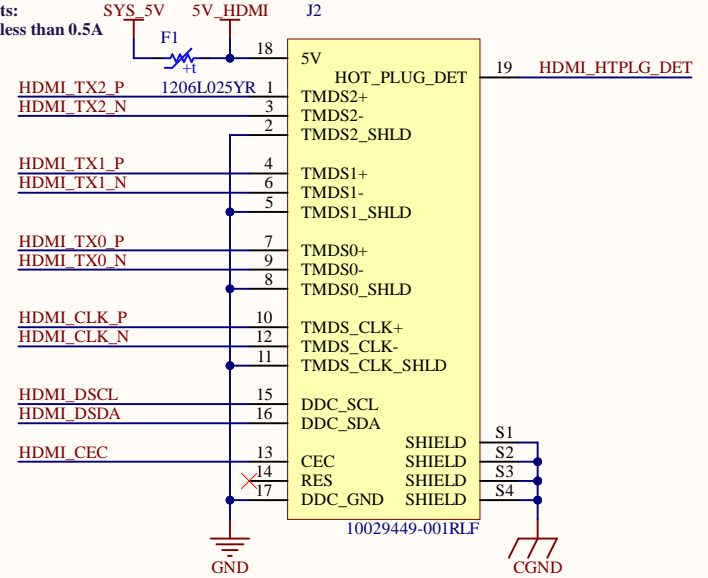
GREEN



BLUE

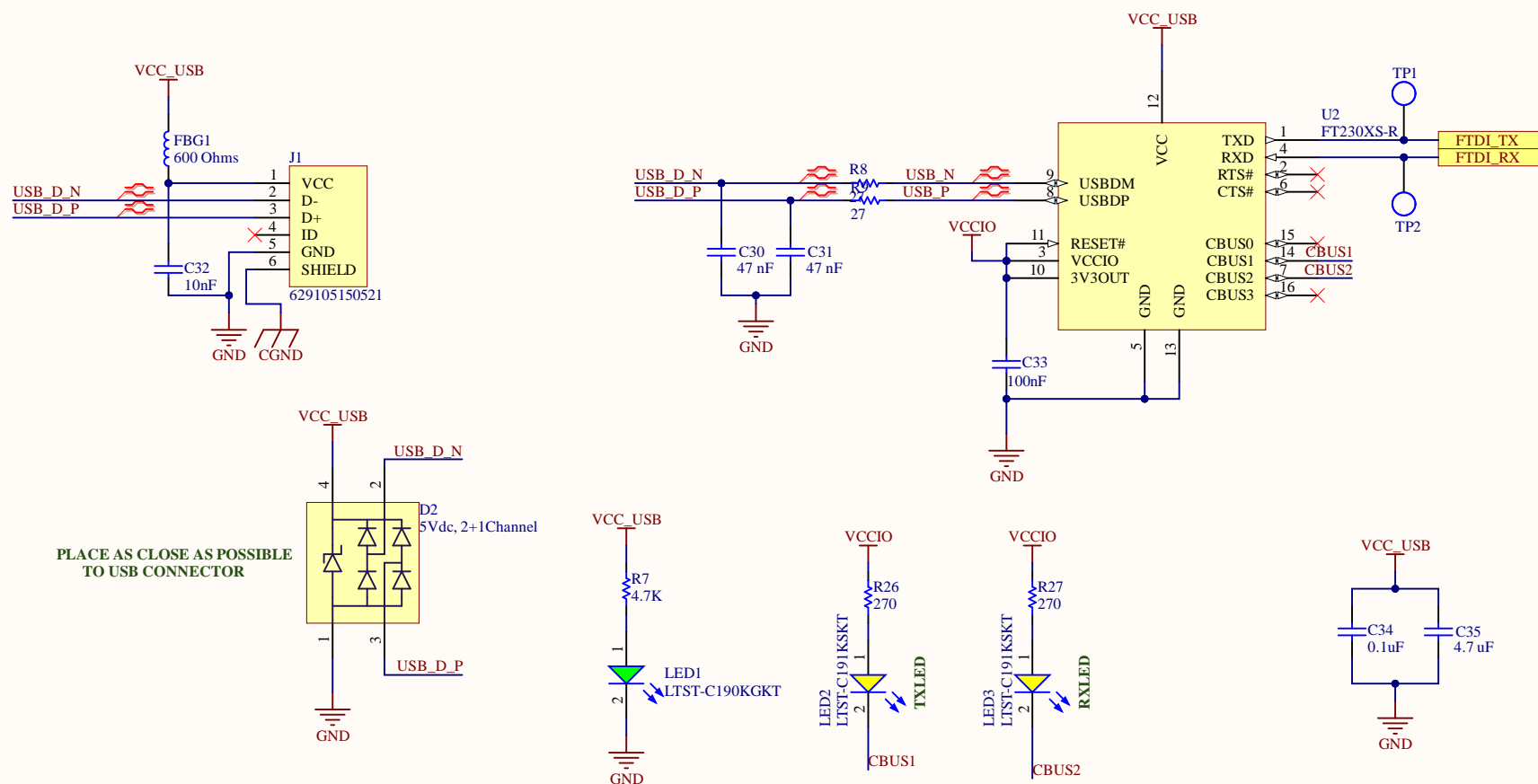


As per HDMI requirements:
- Short circuit protection, less than 0.5A
Fused at 0.25A.



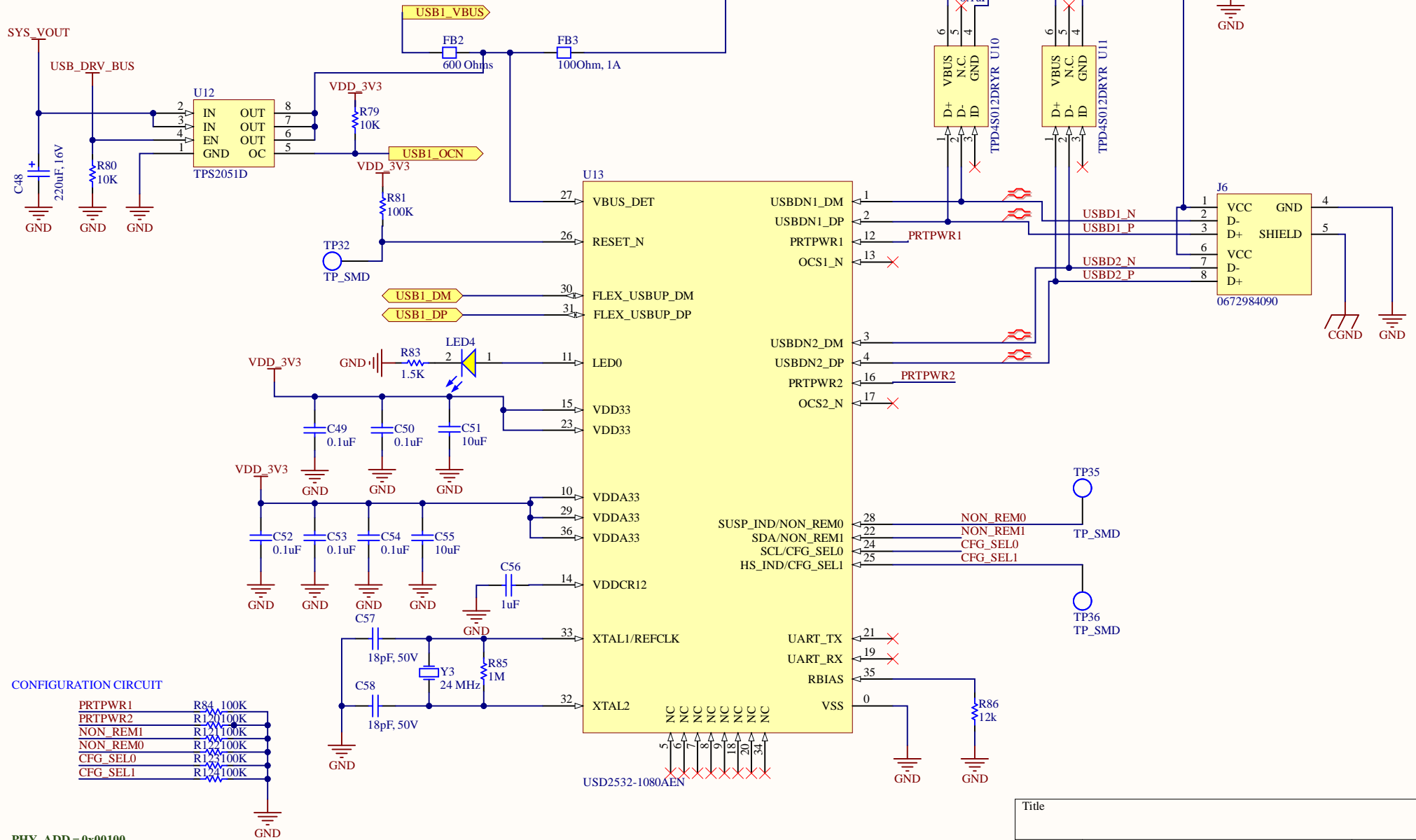
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File:	C:\Users\...\HDMI.SchDoc	Drawn By:

UART DEBUG: DEBUG PORT.



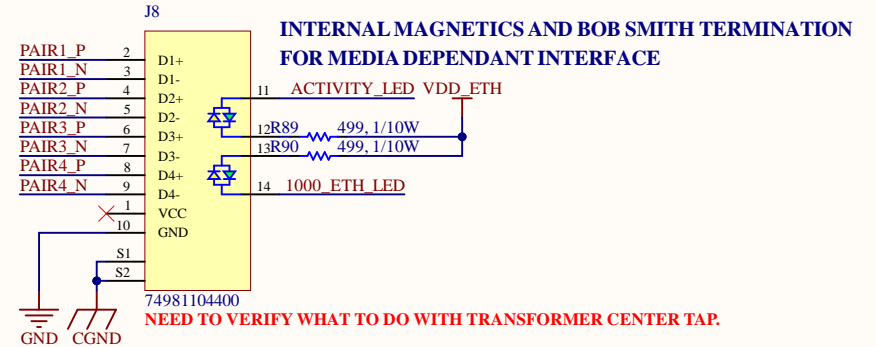
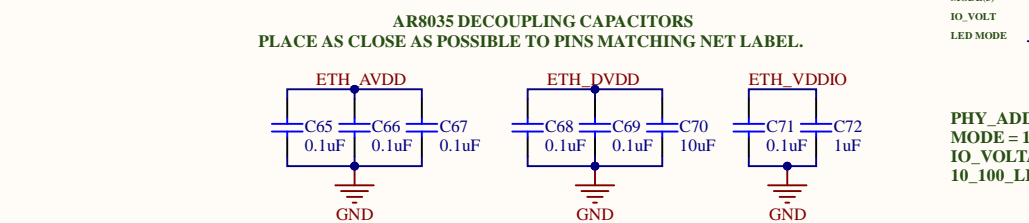
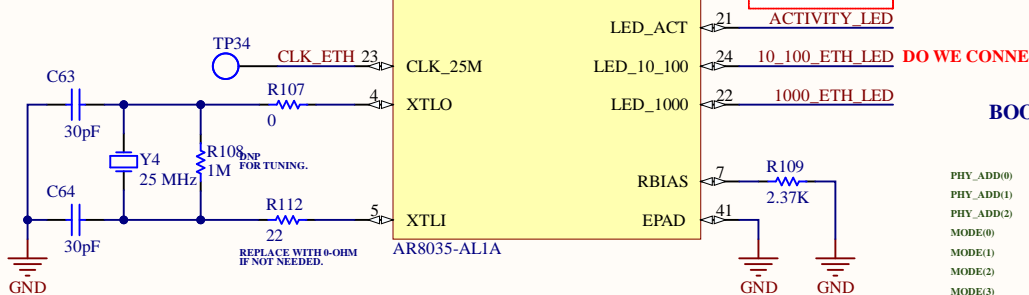
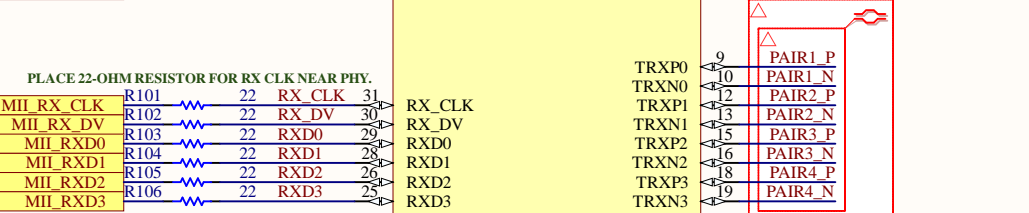
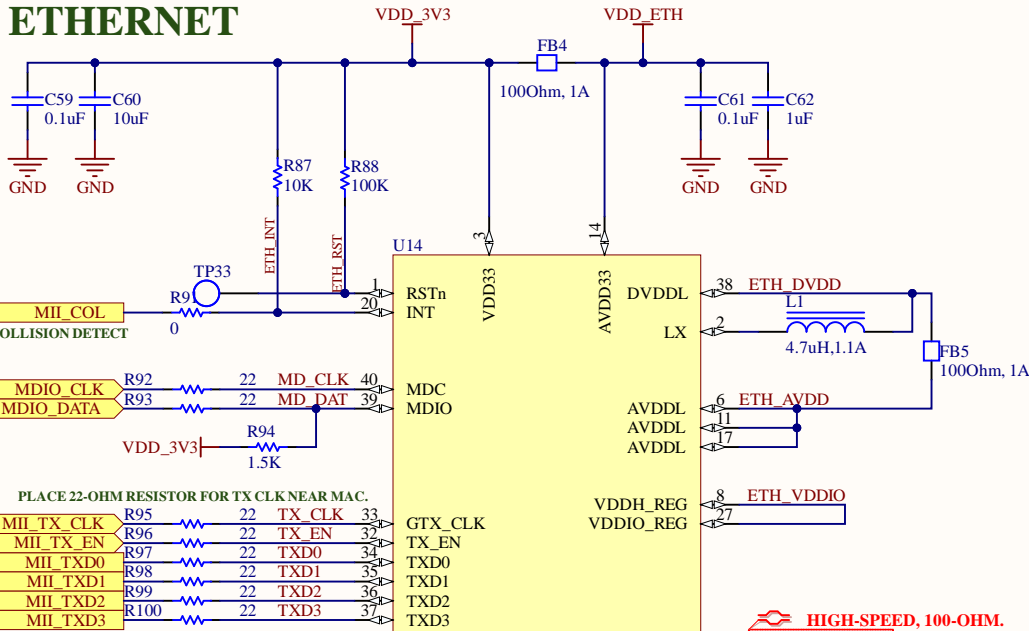
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Size A4	Number	Revision
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File:	C:\Users\...\P03_UART_Debug_SchDoc	Drawn By:

USB HUB



Title		
Size	Number	Revision
A4		
Date:	2-15-2020	Sheet of
File:	C:\Users\...\P04_USB_hub.SchDoc	Drawn By:

ETHERNET



PHY Pin	PHY Core Config Signal	Description	Default Internal Weak Pull-up/Pull-down
RXD0	PHYADDRESS0	LED_ACT, RXD[1:0] sets the lower three bits of the physical address. The upper two bits of the physical address are set to the default, "00".	0
RXD1	PHYADDRESS1		0
LED_ACT	PHYADDRESS2		1
RX_DV	MODE0	mode select bit 0	0
RXD2	MODE1	mode select bit 1	0
LED_1000	MODE2	mode select bit 2	1
RXD3	MODE3	mode select bit 3	0
RX_CLK	1.8V/1.5V	Select the RGMII/RMII I/O voltage level	0

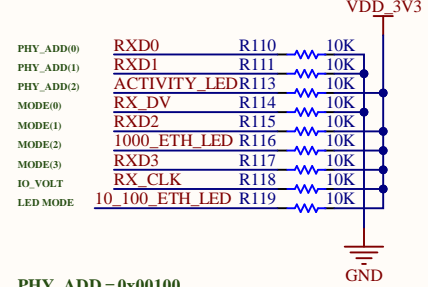
NOTE: 0=Pull-down, 1=Pull-up

NOTE: Power on strapping pins are latched during power-up reset or warm hardware reset.

NOTE: Some MAC devices input pins may drive high/low during power-up or reset. So PHY power on strapping status may be affected by the MAC side. In this case an external 10k pull-down or pull-high resistor is needed to ensure a stable expected status.

NOTE: When using 2.5V RGMII I/O voltage level, RX_CLK can be pull-up or pull-down.

BOOT-CONFIG FOR ETHERNET PHY



PHY_ADD = 0x00100
MODE = 1100 = PLLON (25M OUT CONTINUOUS)
IO_VOLTAGE = 1.8V
10_100_LED PULLED UP = ACTIVE LOW.

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