- 135-mΩ -Maximum (5-V Input) High-Side MOSFET Switch
- 500 mA Continuous Current
- Short-Circuit and Thermal Protection With Overcurrent Logic Output
- Operating Range . . . 2.7 V to 5.5 V
- Logic-Level Enable Input
- 2.5-ms Typical Rise Time
- Undervoltage Lockout
- 10 μA Maximum Standby Supply Current
- Bidirectional Switch
- Available in 8-pin SOIC and PDIP Packages
- Ambient Temperature Range, -40°C to 85°C
- 2-kV Human-Body-Model, 200-V Machine-Model ESD Protection
- UL Listed File No. E169910

TPS2041 D OR P PACKAGE (TOP VIEW) GND [8 OUT IN [ПΟυΤ 2 7 NOUT IN [3 6 ĒΝ 5 \overline{OC} 4 TPS2051 D OR P PACKAGE (TOP VIEW) **GND ∏** OUT 8 I) OUT IN 2 7 IN 3 6 I OUT $\overline{\mathsf{oc}}$ ΕN 4 5

description

The TPS2041 and TPS2051 power distribution switches are intended for applications where heavy capacitive loads and short circuits are likely to be encountered. The TPS2041 and the TPS2051 are $135\text{-m}\Omega$ N-channel MOSFET high-side power switches. Each switch is controlled by a logic enable compatible with 5-V and 3-V logic. Gate drive is provided by an internal charge pump that controls the power-switch rise times and fall times to minimize current surges during switching. The charge pump requires no external components and allows operation from supplies as low as 2.7 V.

When the output load exceeds the current-limit threshold or a short is present, the TPS2041 and TPS2051 limit the output current to a safe level by switching into a constant-current mode, pulling the overcurrent (\overline{OC}) logic output low. When continuous heavy overloads and short circuits increase the power dissipation in the switch, causing the junction temperature to rise, a thermal protection circuit shuts off the switch in overcurrent to prevent damage. Recovery from a thermal shutdown is automatic once the device has cooled sufficiently. Internal circuitry ensures the switch remains off until valid input voltage is present.

The TPS2041 and TPS2051 are designed to limit at 0.9-A load. These power distribution switches are available in 8-pin small-outline integrated circuit (SOIC) and 8-pin plastic dual-in-line packages (PDIP) and operate over an ambient temperature range of –40°C to 85°C.

AVAILABLE OPTIONS

			RECOMMENDED MAXIMUM CONTINUOUS	TYPICAL SHORT-CIRCUIT	PACKAGE	D DEVICES
	TA	ENABLE	LOAD CURRENT (A)	CURRENT LIMIT AT 25°C (A)	SOIC (D)†	PDIP (P)
	–40°C to 85°C	Active low	0.5	0.9	TPS2041D	TPS2041P
I	–40°C to 85°C	Active high	0.5	0.9	TPS2051D	TPS2051P

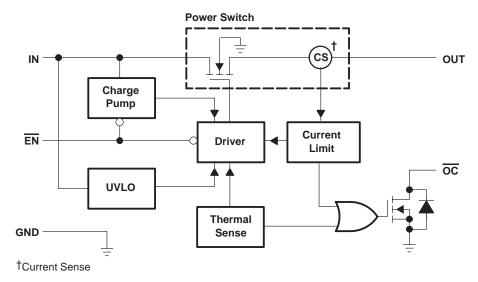
[†] The D package is available taped and reeled. Add an R suffix to device type (e.g., TPS2041DR)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



TPS2041 functional block diagram



Terminal Functions

	TERMINAL	-							
	N	0.	1/0	DESCRIPTION					
NAME	D OR P			DESCRIPTION					
	TPS2041	TPS2051							
EN	4 –		- 1	Enable input. Logic low turns on power switch.					
EN	- 4		- 1	Enable input. Logic high turns on power switch.					
GND	1	1	- 1	Ground					
IN	2, 3 2, 3		1	Input voltage					
<u>oc</u>	5 5		0	Over current. Logic output active low					
OUT	OUT 6, 7, 8 6, 7, 8		0	Power-switch output					

detailed description

power switch

The power switch is an N-channel MOSFET with a maximum on-state resistance of 135 m Ω (V_{I(IN)} = 5 V). Configured as a high-side switch, the power switch prevents current flow from OUT to IN and IN to OUT when disabled. The power switch supplies a minimum of 500 mA per switch.

charge pump

An internal charge pump supplies power to the driver circuit and provides the necessary voltage to pull the gate of the MOSFET above the source. The charge pump operates from input voltages as low as 2.7 V and requires very little supply current.

driver

The driver controls the gate voltage of the power switch. To limit large current surges and reduce the associated electromagnetic interference (EMI) produced, the driver incorporates circuitry that controls the rise times and fall times of the output voltage. The rise and fall times are typically in the 2-ms to 4-ms range.

enable (EN or EN)

The logic enable disables the power switch and the bias for the charge pump, driver, and other circuitry to reduce the supply current to less than 10 μ A when a logic high is present on \overline{EN} (TPS2041) or a logic low is present on EN (TPS2051). A logic zero input on \overline{EN} or a logic high on EN restores bias to the drive and control circuits and turns the power on. The enable input is compatible with both TTL and CMOS logic levels.

overcurrent (OC)

The \overline{OC} open drain output is asserted (active low) when an overcurrent or overtemperature condition is encountered. The output will remain asserted until the overcurrent or overtemperature condition is removed.

current sense

A sense FET monitors the current supplied to the load. The sense FET measures current more efficiently than conventional resistance methods. When an overload or short circuit is encountered, the current-sense circuitry sends a control signal to the driver. The driver in turn reduces the gate voltage and drives the power FET into its saturation region, which switches the output into a constant current mode and holds the current constant while varying the voltage on the load.

thermal sense

An internal thermal-sense circuit shuts off the power switch when the junction temperature rises to approximately 140°C. Hysteresis is built into the thermal sense circuit. After the device has cooled approximately 20°C, the switch turns back on. The switch continues to cycle off and on until the fault is removed.

undervoltage lockout

A voltage sense circuit monitors the input voltage. When the input voltage is below approximately 2 V, a control signal turns off the power switch.



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Input voltage range, V _{I(IN)} (see Note 1)	0.3 V to 6 V
Output voltage range, $\dot{V}_{O(OUT)}$ (see Note 1)	$-0.3 \text{ V to V}_{I(IN)} + 0.3 \text{ V}$
Input voltage range, $V_{I(ENx)}$ or $V_{I(ENx)}$	
Continuous output current, Í _{O(OUT)}	internally limited
Continuous total power dissipation	
Operating virtual junction temperature range, T _J	–40°C to 125°C
Storage temperature range, T _{stq}	
Lead temperature soldering 1,6 mm (1/16 inch) from case for 10 seconds	
Electrostatic discharge (ESD) protection: Human body model MIL-STD-883C	2 kV
Machine model	0.2 kV

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. NOTE 1: All voltages are with respect to GND.

DISSIPATION RATING TABLE

PACKAGE	$T_{\mbox{A}} \le 25^{\circ}\mbox{C}$ POWER RATING	DERATING FACTOR ABOVE T _A = 25°C	T _A = 70°C POWER RATING	T _A = 85°C POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW
Р	1175 mW	9.4 mW/°C	752 mW	611 mW

recommended operating conditions

	TPS	2041	TPS2	2051	UNIT	
	MIN	MIN MAX		MAX	UNIT	
Input voltage, V _{I(IN)}	2.7	5.5	2.7	5.5	V	
Input voltage, V _{I(EN)} or V _{I(EN)}	0	5.5	0	5.5	V	
Continuous output current, IO(OUT)	0	500	0	500	mA	
Operating virtual junction temperature, TJ	-40	125	-40	125	°C	



electrical characteristics over recommended operating junction temperature range, $V_{I(IN)}$ = 5.5 V, I_{O} = rated current, $V_{I(EN)}$ = 0 V, $V_{I(EN)}$ = Hi (unless otherwise noted)

power switch

	PARAMETER	TEST COL	UDITIONST	Т	PS2041		Т	PS2051		UNIT
	PARAMETER	TEST COI	NDITIONST	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
		$V_{I(IN)} = 5 V$	T _J = 25°C		80	95		80	95	
	Static drain-source on-state resistance, 5-V operation	$V_{I(IN)} = 5 V$	T _J = 85°C		90	120		90	120	
r _{DS(on)}	Teoletanes, e v eperation	$V_{I(IN)} = 5 V$	T _J = 125°C		100	135		100	135	mΩ
		$V_{I(IN)} = 3.3 \text{ V},$	$T_J = 25^{\circ}C$		85	105		85	105	
	Static drain-source on-state resistance, 3.3-V operation	$V_{I(IN)} = 3.3 \text{ V},$	$T_J = 85^{\circ}C$		100	135		100	135	
	redistance, d.o v operation	$V_{I(IN)} = 3.3 \text{ V},$	T _J = 125°C		115	150		115	150	
	Digo time output	$V_{I(IN)} = 5.5 \text{ V},$ $C_L = 1 \mu\text{F},$	$T_J = 25^{\circ}C$, $R_L = 10 \Omega$		2.5			2.5		
t _r	Rise time, output	$V_{I(IN)} = 2.7 \text{ V},$ $C_L = 1 \mu\text{F},$			3			3		ms
	Fall time output	$V_{I(IN)} = 5.5 \text{ V},$ $C_L = 1 \mu\text{F},$	$T_J = 25^{\circ}C$, $R_L = 10 \Omega$		4.4	·		4.4		ma
t _f	Fall time, output	$V_{I(IN)} = 2.7 \text{ V},$ $C_L = 1 \mu\text{F},$	$T_J = 25^{\circ}C$, $R_L = 10 \Omega$		2.5			2.5		ms

[†] Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.

enable input EN or EN

	PARAMETER		TEST CONDITIONS	1	TPS2041			TPS2051		
	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
V _{IH}	High-level input voltag	е	$2.7 \text{ V} \le \text{V}_{\text{I(IN)}} \le 5.5 \text{ V}$	2			2			V
\/	Low lovel input voltage	,	$4.5 \text{ V} \le \text{V}_{\text{I(IN)}} \le 5.5 \text{ V}$			0.8			0.8	V
VIL	Low-level input voltage	=	$2.7 \text{ V} \le \text{V}_{\text{I(IN)}} \le 4.5 \text{ V}$			0.4			0.4	
١.	Input ourront	TPS2041	$V_{I}(\overline{EN}) = 0 \text{ V or } V_{I}(\overline{EN}) = V_{I}(IN)$	-0.5		0.5				
l II	Input current	TPS2051	$V_{I(EN)} = V_{I(IN)}$ or $V_{I(EN)} = 0$ V				-0.5		0.5	μΑ
ton	Turnon time		$C_L = 100 \mu F, R_L = 10 \Omega$			20			20	ms
toff	Turnoff time		$C_L = 100 \mu\text{F}, R_L = 10 \Omega$			40			40	

current limit

	PARAMETER	TEST CONDITIONS [†]	7	ΓPS2041		1	UNIT		
	PARAIVIETER	TEST CONDITIONS [†]	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
los	Short-circuit output current	V _{I(IN)} = 5 V, OUT connected to GND, Device enabled into short circuit	0.7	0.9	1.1	0.7	0.9	1.1	A

[†] Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.

TPS2041, TPS2051 POWER-DISTRIBUTION SWITCHES

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electrical characteristics over recommended operating junction temperature range, $V_{I(IN)}$ = 5.5 V, I_{O} = rated current, $V_{I(EN)}$ = 0 V, $V_{I(EN)}$ = Hi (unless otherwise noted) (continued)

supply current

PARAMETER		TEST (CONDITIONS		Т	PS2041		Т	PS2051		UNIT
PARAMETER		TEST	CONDITIONS		MIN	TYP	MAX	MIN	TYP	MAX	UNII
		l	T _J = 25°C	TPS2041		0.015	1				
Supply current,	No Load	$\overline{EN} = V_{I(IN)}$	$-40^{\circ}C \le T_{J} \le 125^{\circ}C$	1732041			10				
low-level output	on OUT	EN = 0 V	T _J = 25°C	TPS2051					0.015	1	μΑ
		LIN = 0 V	$-40^{\circ}C \le T_{J} \le 125^{\circ}C$	11-32031						10	
		EN = 0 V	T _J = 25°C	TPS2041		80	100				
Supply current,	No Load on OUT	EN = 0 V	$-40^{\circ}C \le T_{J} \le 125^{\circ}C$	1732041		100					μА
high-level output		EN = V _{I(IN)}	T _J = 25°C	TPS2051					80	100	
		$\Gamma_{IA} = \Lambda_{I}(IN)$	$-40^{\circ}C \le T_{J} \le 125^{\circ}C$	11-32031					100		
Leakage current	OUT connected	$\overline{EN} = V_{I(IN)}$	$-40^{\circ}C \le T_{J} \le 125^{\circ}C$	TPS2041		100					μΑ
Leakage current	to ground	EN= 0 V	$-40^{\circ}C \le T_{J} \le 125^{\circ}C$	TPS2051					100		μΑ
Reverse leakage	IN = High	$V_{I(EN)} = 0 V$	T 25°C	TPS2041		0.3					
current	impedance	V _{I(EN)} = Hi	T _J = 25°C	TPS2051					0.3		μА

undervoltage lockout

PARAMETER	TEST CONDITIONS	Т	PS2041		Т	UNIT		
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
Low-level input voltage		2		2.5	2		2.5	V
Hysteresis	T _J = 25°C		100			100		mV

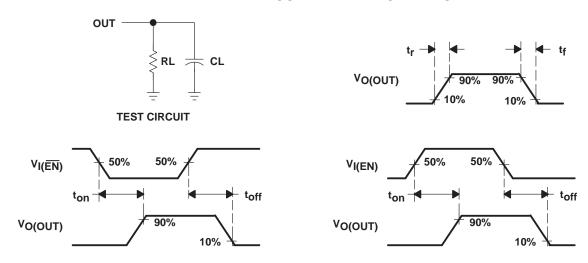
overcurrent OC

PARAMETER	TEST CONDITIONS	TPS2041	TPS2051	UNIT
PARAMETER	TEST CONDITIONS	MIN TYP MAX	MIN TYP MAX	UNIT
Sink current [†]	V _O = 5 V	10	10	mA
Output low voltage	$I_O = 5 \text{ V}, V_{OL(OC)}$	0.5	0.5	V
Off-state current [†]	$V_O = 5 \text{ V}, V_O = 3.3 \text{ V}$	1	1	μΑ

[†] Specified by design, not production tested.



PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORMS

Figure 1. Test Circuit and Voltage Waveforms

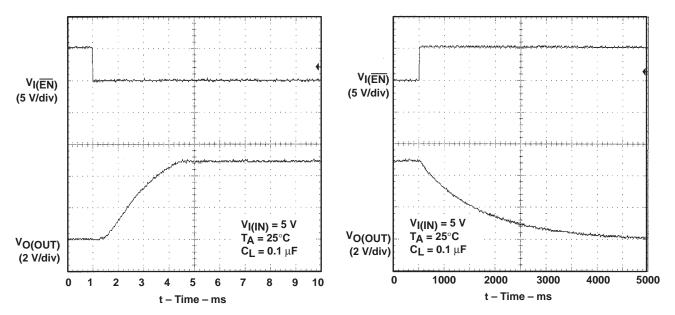
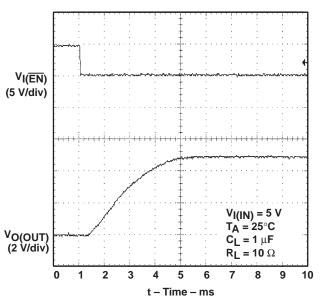


Figure 2. Turnon Delay and Rise Time with 0.1- μ F Load

Figure 3. Turnoff Delay and Fall Time with 0.1-µF Load

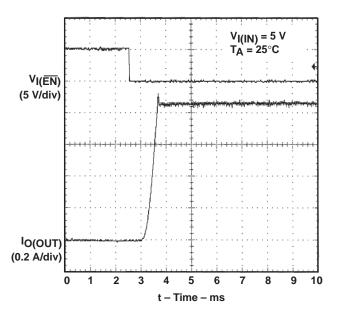
PARAMETER MEASUREMENT INFORMATION



VI(EN) (5 V/div) $V_{I(IN)} = 5 V$ $T_A = 25^{\circ}C$ VO(OUT) $C_L = 1 \mu F$ (2 V/div) $R_L = 10 \Omega$ 2 4 6 8 10 12 18 20 t - Time - ms

Figure 4. Turnon Delay and Rise Time with 1-μF Load

Figure 5. Turnoff Delay and Fall Time with 1-μF Load



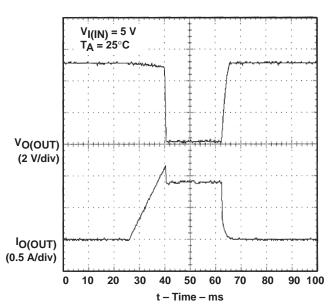


Figure 6. TPS2041, Short-Circuit Current, Device Enabled into Short

Figure 7. TPS2041, Threshold Trip Current with Ramped Load on Enabled Device

PARAMETER MEASUREMENT INFORMATION

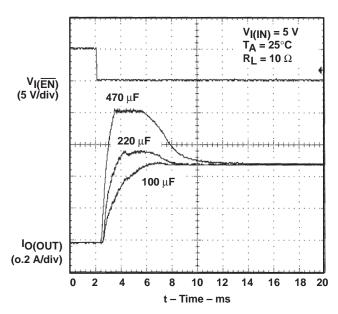


Figure 8. Inrush Current with 100-μF, 220-μF and 470-μF Load Capacitance

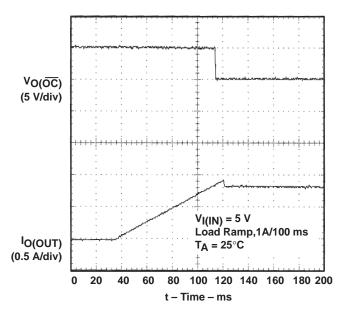


Figure 9. Ramped Load on Enabled Device

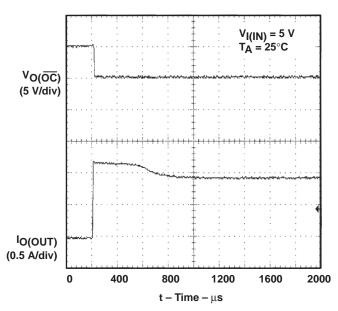


Figure 10. 4- Ω Load Connected to Enabled Device

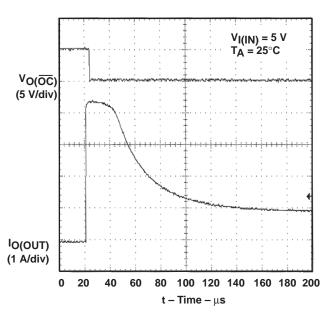
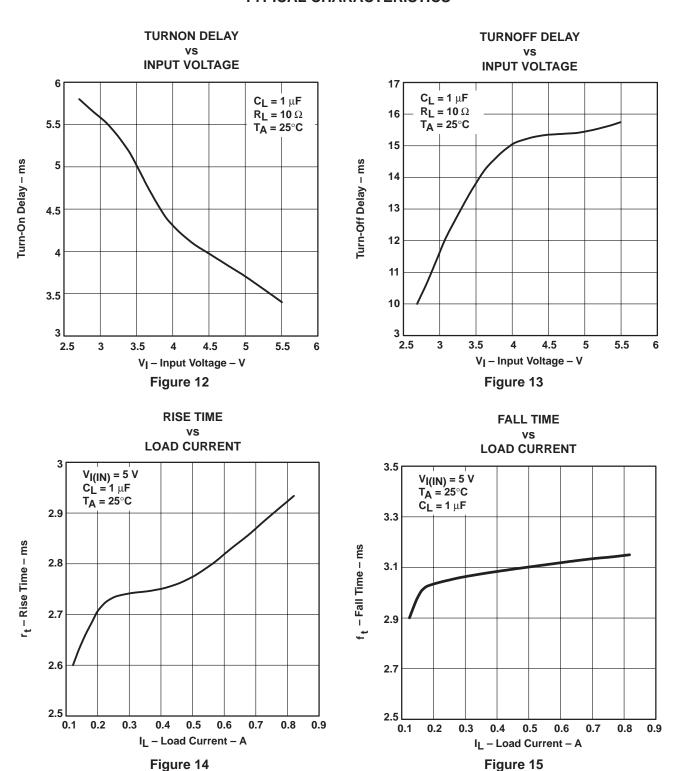


Figure 11. 1-Ω Load Connected to Enabled Device

TYPICAL CHARACTERISTICS





SUPPLY CURRENT, OUTPUT DISABLED

JUNCTION TEMPERATURE

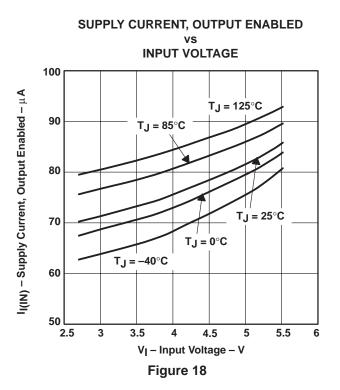
TYPICAL CHARACTERISTICS

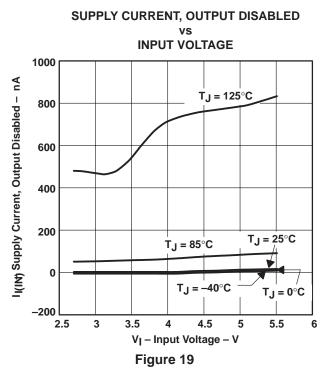
1000

SUPPLY CURRENT, OUTPUT ENABLED JUNCTION TEMPERATURE 100 II(IN)– Supply Current, Output Enabled $-\mu A$ $V_{I(IN)} = 5.5 V$ $V_{I(IN)} = 5 V$ 90 80 $V_{I(IN)} = 4 V$ $V_{I(IN)} = 2.7 V$ 70 $V_{I(IN)} = 3.3 V$ 60 50 125 150 -25 25 50 75 100 -50 T_J - Junction Temperature - °C

Figure 16

I(IN) - Supply Current, Output Disabled - nA 900 $V_{I(IN)} = 5.5 V$ 800 $V_{I(IN)} = 5 V$ 700 $V_{I(IN)} = 4 V^{-}$ 600 500 $V_{I(IN)} = 2.7 V$ 400 300 200 100 -100 -50 -25 25 50 75 100 125 150 T_J - Junction Temperature - °C Figure 17





 $^{\prime}$ DS(on) $^{-}$ Static Drain-Source On-State Resistance $^{-}$ m Ω

TYPICAL CHARACTERISTICS

STATIC DRAIN-SOURCE ON-STATE RESISTANCE JUNCTION TEMPERATURE 175 $I_0 = 0.5 A$ $V_{I(IN)} = 2.7$ 150 $V_{I(IN)} = 3.3 V$ 125 100 V_{I(IN)} = 4.5 V V_{I(IN)} = 5 V 75 50

50

T_J – Junction Temperature – °C

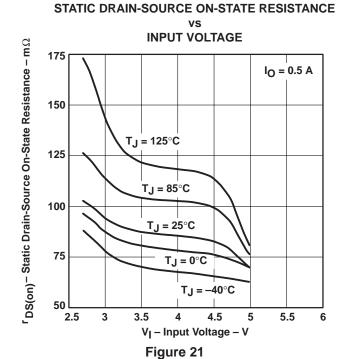
Figure 20

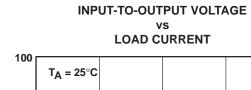
75

100

125

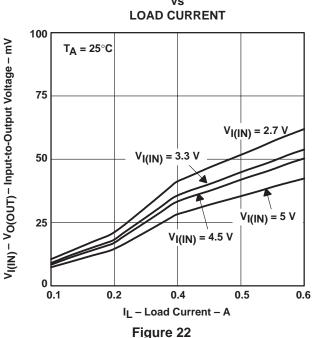
150

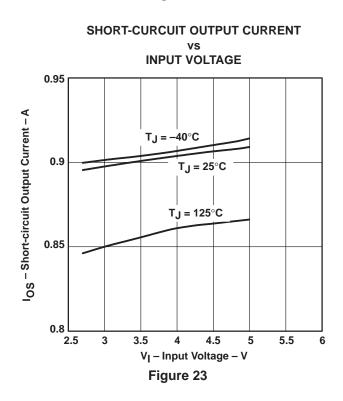




-25

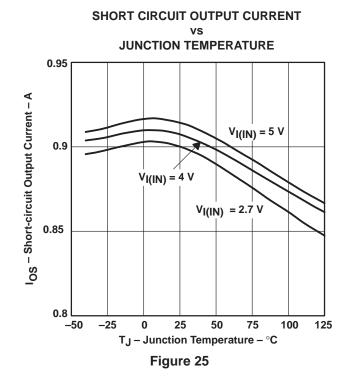
-50





TYPICAL CHARACTERISTICS

THRESHOLD TRIP CURRENT **INPUT VOLTAGE** 1.2 T_A = 25°C Load Ramp = 1 A/10 ms 1.175 Threshold Trip Current – A 1.15 1.125 1. 2.5 3 3.5 4.5 5 5.5 6 V_I - Input Voltage - V



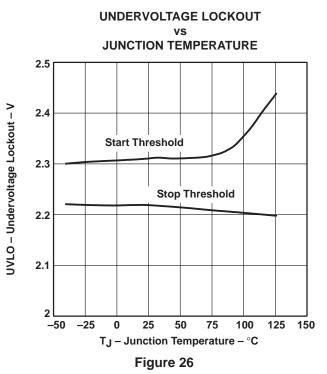
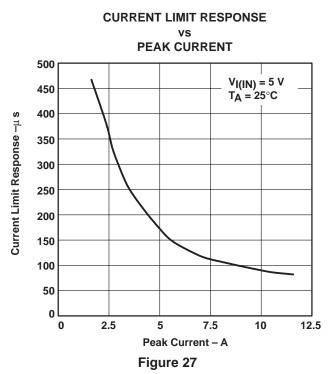


Figure 24



TYPICAL CHARACTERISTICS

OVERCURRENT RESPONSE TIME (OC) PEAK CURRENT 8 $V_{I(IN)} = 5 V$ T_A = 25°C 6 Response Time - µ s 2 0 2.5 5 7.5 10 12.5 Peak Current - A

APPLICATION INFORMATION

Figure 28

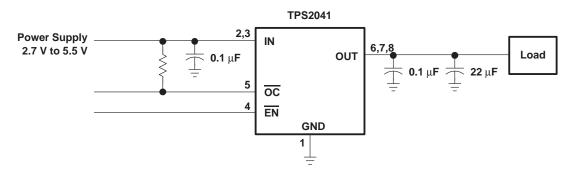


Figure 29. Typical Application

power-supply considerations

A 0.01-μF to 0.1-μF ceramic bypass capacitor between INx and GND, close to the device, is recommended. Placing a high-value electrolytic capacitor on the output pin(s) is recommended when the output load is heavy. This precaution reduces power-supply transients that may cause ringing on the input. Additionally, bypassing the output with a 0.01-μF to 0.1-μF ceramic capacitor improves the immunity of the device to short-circuit transients.



overcurrent

A sense FET is employed to check for overcurrent conditions. Unlike current-sense resistors, sense FETs do not increase the series resistance of the current path. When an overcurrent condition is detected, the device maintains a constant output current and reduces the output voltage accordingly. Complete shutdown occurs only if the fault is present long enough to activate thermal limiting.

Three possible overload conditions can occur. In the first condition, the output has been shorted before the device is enabled or before $V_{I(IN)}$ has been applied (see Figure 6). The TPS2041 and TPS2051 sense the short and immediately switch into a constant-current output.

In the second condition, the short occurs while the device is enabled. At the instant the short occurs, very high currents may flow for a short time before the current-limit circuit can react. After the current-limit circuit has tripped (reached the overcurrent trip threshhold) the device switches into constant-current mode.

In the third condition, the load has been gradually increased beyond the recommended operating current. The current is permitted to rise until the current-limit threshold is reached or until the thermal limit of the device is exceeded (see Figure 7). The TPS2041 and TPS2051 are capable of delivering current up to the current-limit threshold without damaging the device. Once the threshold has been reached, the device switches into its constant-current mode.

OC response

The \overline{OC} open-drain output is asserted (active low) when an overcurrent or overtemperature condition is encountered. The output will remain asserted until the overcurrent or overtemperature condition is removed. Connecting a heavy capacitive load to an enabled device can cause momentary false overcurrent reporting from the inrush current flowing through the device, charging the downstream capacitor. An RC filter of 500 μ s (see Figure 30) can be connected to the \overline{OC} pin to reduce false overcurrent reporting. Using low-ESR electrolytic capacitors on the output lowers the inrush current flow through the device during hot-plug events by providing a low-impedance energy source, thereby reducing erroneous overcurrent reporting.

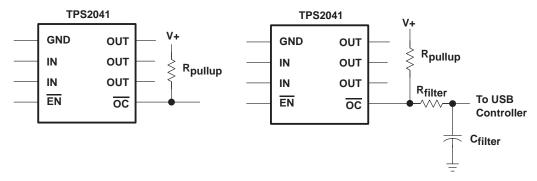


Figure 30. Typical Circuit for \overline{OC} Pin and RC Filter for Damping Inrush \overline{OC} Responses

power dissipation and junction temperature

The low on-resistance on the n-channel MOSFET allows small surface-mount packages, such as SOIC, to pass large currents. The thermal resistances of these packages are high compared to those of power packages; it is good design practice to check power dissipation and junction temperature. The first step is to find $r_{DS(on)}$ at the input voltage and operating temperature. As an initial estimate, use the highest operating ambient temperature of interest and read $r_{DS(on)}$ from Figure 21. Next, calculate the power dissipation using:

$$P_D = r_{DS(on)} \times I^2$$

Finally, calculate the junction temperature:

$$T_J = P_D \times R_{\theta JA} + T_A$$

Where:

 T_A = Ambient Temperature °C $R_{\theta JA}$ = Thermal resistance SOIC = 172°C/W, PDIP = 106°C/W

Compare the calculated junction temperature with the initial estimate. If they do not agree within a few degrees, repeat the calculation, using the calculated value as the new estimate. Two or three iterations are generally sufficient to get a reasonable answer.

thermal protection

Thermal protection prevents damage to the IC when heavy-overload or short-circuit faults are present for extended periods of time. The faults force the TPS2041 and TPS2051 into constant current mode, which causes the voltage across the high-side switch to increase; under short-circuit conditions, the voltage across the switch is equal to the input voltage. The increased dissipation causes the junction temperature to rise to high levels. The protection circuit senses the junction temperature of the switch and shuts it off. Hysteresis is built into the thermal sense circuit, and after the device has cooled approximately 20 degrees, the switch turns back on. The switch continues to cycle in this manner until the load fault or input power is removed.

undervoltage lockout (UVLO)

An undervoltage lockout ensures that the power switch is in the off state at powerup. Whenever the input voltage falls below approximately 2 V, the power switch will be quickly turned off. This facilitates the design of hot-insertion systems where it is not possible to turn off the power switch before input power is removed. The UVLO will also keep the switch from being turned on until the power supply has reached at least 2 V, even if the switch is enabled. Upon reinsertion, the power switch will be turned on, with a controlled rise time to reduce EMI and voltage overshoots.

universal serial bus (USB) applications

The universal serial bus (USB) interface is a 12-Mb/s, or 1.5-Mb/s, multiplexed serial bus designed for low-to-medium bandwidth PC peripherals (e.g., keyboards, printers, scanners, and mice). The four-wire USB interface is conceived for dynamic attach-detach (hot plug-unplug) of peripherals. Two lines are provided for differential data, and two lines are provided for 5-V power distribution.

USB data is a 3.3-V level signal, but power is distributed at 5 V to allow for voltage drops in cases where power is distributed through more than one hub across long cables. Each function must provide its own regulated 3.3 V from the 5-V input or its own internal power supply.



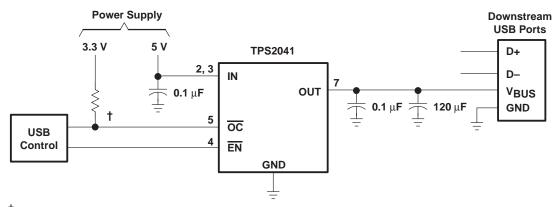
The USB specification defines the following five classes of devices, each differentiated by power-consumption requirements:

- Hosts/self-powered hubs (SPH)
- Bus-powered hubs (BPH)
- Low-power, bus-powered functions
- High-power, bus-powered functions
- Self-powered functions

Self-powered and bus-powered hubs distribute data and power to downstream functions. The TPS2041 and TPS2051 can provide power-distribution solutions for many of these classes of devices.

host/self-powered and bus-powered hubs

Hosts and self-powered hubs have a local power supply that powers the embedded functions and the downstream ports (see Figure 31). This power supply must provide from 5.25 V to 4.75 V to the board side of the downstream connection under full-load and no-load conditions. Hosts and SPHs are required to have current limit protection and must report overcurrent conditions to the USB controller. Typical SPHs are desktop PCs, monitors, printers, and stand-alone hubs.



[†] May need RC Filter (see Figure 34)

Figure 31. One-Port Solution

Bus-powered hubs obtain all power from upstream ports and often contain an embedded function. The hubs are required to power up with less than one unit load. The BPH usually has one embedded function, and power is always available to the controller of the hub. If the embedded function and hub require more than 100 mA on powerup, the power to the embedded function may need to be kept off until enumeration is completed. This can be accomplished by removing power or by shutting off the clock to the embedded function. Power switching the embedded function is not necessary if the aggregate power draw for the function and controller is less than one unit load. The total current drawn by the bus-powered device is the sum of the current to the controller, the embedded function, and the downstream ports, and it is limited to 500 mA from an upstream port.

low-power bus-powered functions and high-power bus-powered functions

Both low-power and high-power bus-powered functions obtain all power from upstream ports; low-power functions always draw less than 100 mA; high-power functions must draw less than 100 mA at powerup and can draw up to 500 mA after enumeration. If the load of the function is more than the parallel combination of 44Ω and 10μ F at powerup, the device must implement inrush current limiting (see Figure 32).

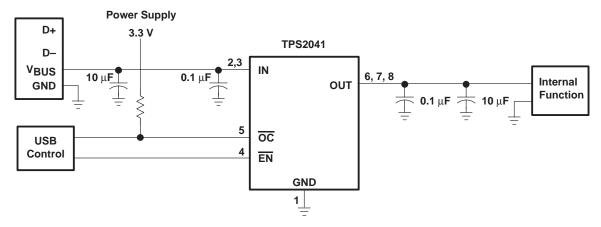


Figure 32. High-Power Bus-Powered Function

USB power-distribution requirements

USB can be implemented in several ways, and, regardless of the type of USB device being developed, several power distribution features must be implemented.

- Hosts/self-powered hubs must:
 - Current-limit downstream ports
 - Report overcurrent conditions on USB V_{BUS}
- Bus-powered hubs must:
 - Enable/disable power to downstream ports
 - Power up at <100 mA
 - Limit inrush current ($<44 \Omega$ and 10 μ F)
- Functions must:
 - Limit inrush currents
 - Power up at <100 mA

The feature set of the TPS2041 and TPS2051 allows them to meet each of these requirements. The integrated current-limiting and overcurrent reporting is required by hosts and self-powered hubs. The logic-level enable and controlled rise times meet the need of both input and output ports on bus-power hubs, as well as the input ports for bus-power functions (see Figure 33).



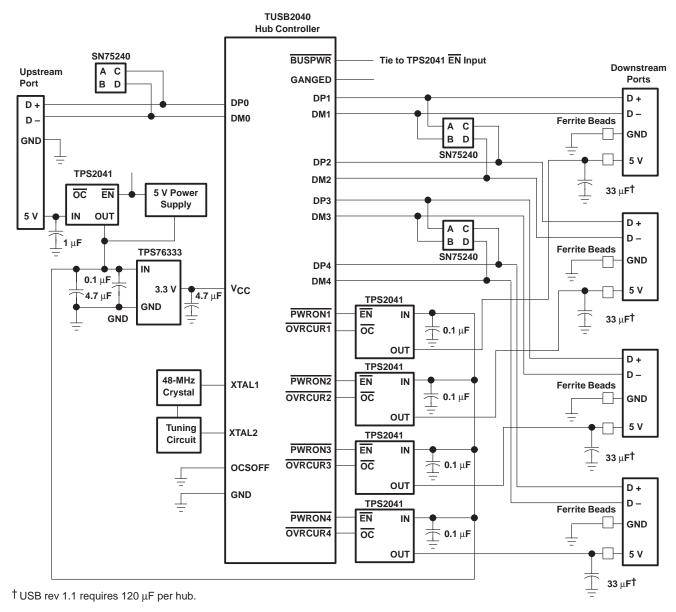


Figure 33. Hybrid Self/Bus-Powered Hub Implementation

generic hot-plug applications (see Figure 34)

In many applications it may be necessary to remove modules or pc boards while the main unit is still operating. These are considered hot-plug applications. Such implementations require the control of current surges seen by the main power supply and the card being inserted. The most effective way to control these surges is to limit and slowly ramp the current and voltage being applied to the card, similar to the way in which a power supply normally turns on. Due to the controlled rise times and fall times of the TPS2041 and TPS2051, these devices can be used to provide a softer start-up to devices being hot-plugged into a powered system. The UVLO feature of the TPS2041 and TPS2051 also ensures the switch will be off after the card has been removed, and the switch will be off during the next insertion. The UVLO feature guarantees a soft start with a controlled rise time for every insertion of the card or module.

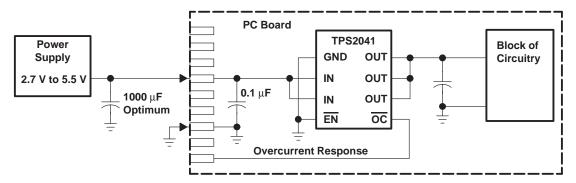


Figure 34. Typical Hot-Plug Implementation

By placing the TPS2041 and TPS2051 between the V_{CC} input and the rest of the circuitry, the input power will reach these devices first after insertion. The typical rise time of the switch is approximately 2.5 ms, providing a slow voltage ramp at the output of the device. This implementation controls system surge currents and provides a hot-plugging mechanism for any device.







6-Feb-2020

PACKAGING INFORMATION

Orderable Device	Status	Package Type	Package Drawing	Pins	Package Qty	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Device Marking (4/5)	Samples
TPS2041D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2041	Samples
TPS2041DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2041	Samples
TPS2041P	ACTIVE	PDIP	Р	8	50	Pb-Free (RoHS)	NIPDAU	N / A for Pkg Type	-40 to 85	TPS2041P	Samples
TPS2051D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2051	Samples
TPS2051DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2051	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

- (3) MSL, Peak Temp. The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead/Ball Finish Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.



PACKAGE OPTION ADDENDUM

6-Feb-2020

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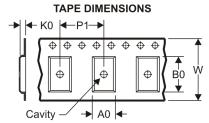
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PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing			Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS2041DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS2051DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

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*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS2041DR	SOIC	D	8	2500	340.5	338.1	20.6
TPS2051DR	SOIC	D	8	2500	340.5	338.1	20.6

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