HDMI

VIDEO CLOCK

VDD_3V3 H1 — REMOVE JUMPER TO DISABLE VIDEO CLOCK.

U6 ASDMB-12.000MHZ-LC-T: VCC, GND, C9 0.1uF, R14 100K, R15 22, VID_CLK

AUDIO CLOCK

U8 ASDMB-24.576MHZ-LC-T: VCC, GND, C10 0.1uF, R17 22, HDMI_CLKdis, AUDIO_CLK

I2C ADDRESSES
HDMI CORE: 0x70
CEC CORE: 0x68

U1 — TDA19988BHN/C1,557

Pin	Net
53	A0_I2C
54	A1_I2C
23	ACLK (SPI1_SCLK)
4	PCLK (LCD_PCLK)
20	DE/FREF (LCD_DE)
21	VSYNC/VREF (LCD_VSYNC)
22	HSYNC/HREF (LCD_HSYNC)
24	AP0 (SPI1_D0)
25	AP1 (SPI1_SC0)
26	AP2
27	OSC_IN/AP3 (VID_CLK)
28	AP4
63	VPA[0] (RGB11)
62	VPA[1] (RGB12)
61	VPA[2] (RGB13)
60	VPA[3] (RGB14)
59	VPA[4] (RGB15)
58	VPA[5]
57	VPA[6]
56	VPA[7]
9	VPB[0] (RGB5)
8	VPB[1] (RGB6)
7	VPB[2] (RGB7)
6	VPB[3] (RGB8)
3	VPB[4] (RGB9)
2	VPB[5] (RGB10)
1	VPB[6]
64	VPB[7]
18	VPC[0] (RGB0)
17	VPC[1] (RGB1)
16	VPC[2] (RGB2)
15	VPC[3] (RGB3)
13	VPC[4] (RGB4)
12	VPC[5]
11	VPC[6]
10	VPC[7]
35	VDDA(1V8)
36	VDDA(TX)(1V8)
41	VDDA(TX)(1V8)
46	VDDA(TX)(1V8)
47	VDDA(PLL)(1V8)
48	VDDA(PLL)(1V8)
5	VDDDC
29	VDDDC
14	VDDD(IO)(1V8)
55	VDDD(IO)(1V8)
34	EXT_SWING (R1 10K)
40	TX0+ (HDMI_TX0_P)
39	TX0- (HDMI_TX0_N)
43	TX1+ (HDMI_TX1_P)
42	TX1- (HDMI_TX1_N)
45	TX2+ (HDMI_TX2_P)
44	TX2- (HDMI_TX2_N)
38	TXC+ (HDMI_CLK_P)
37	TXC- (HDMI_CLK_N)
52	CSCL (I2C0_SCL)
51	CSDA (I2C0_SDA)
33	DSCL (HDMI_DSCL)
32	DSDA (HDMI_DSDA)
50	INT (HDMI_INT)
30	CEC (HDMI_CEC)
31	HPD (HDMI_HTPLG_DET)
49	TEST (R6 0)
65	EXP/GND
19	VPP

VDD_1V8 — FB1 100Ohm, 1A — VDD_HDMI

100-OHM DIFFERENTIAL IMPEDANCE
MATCH GROUP NET LENGTHS TO 100MILS.
MATCH DIFF PAIR NET LENGTHS TO 5MILS.

5V_HDMI — R2 1.5K, R3 1.5K — I2C0_SCL, I2C0_SDA

VDD_3V3 — R4 10K — HDMI_DSCL, HDMI_DSDA

D1 RB751V40,115 — R5 27K — VDD_3V3

HDMI_INT

DECOUPLING CAPACITORS

VDD_1V8 — C1 2.2uF, C2 2.2uF, C3 0.1uF, C4 0.1uF, C5 0.1uF, C6 0.1uF, C7 2.2uF, C8 2.2uF

HDMI DECOUPLING CAPACITORS
PLACE AS CLOSE AS POSSIBLE TO VDD PINS.

LOW-PASS FILTER CAPS FOR LCD DATA BUS.

NEED TO TEST IF NEEDED.

C11 47pF RGB0, C15 47pF RGB1, C16 47pF RGB2, C17 47pF RGB3, C18 47pF RGB4, C19 47pF RGB5, C20 47pF RGB6, C21 47pF RGB7, C22 47pF RGB8, C23 47pF RGB9, C24 47pF RGB10, C25 47pF RGB11, C26 47pF RGB12, C27 47pF RGB13, C28 47pF RGB14, C29 47pF RGB15

As per HDMI requirements:
- Short circuit protection, less than 0.5A
Fused at 0.25A.

SYS_5V — F1 1206L025YR — 5V_HDMI — J2

Pin	Net
18	5V
19	HOT_PLUG_DET (HDMI_HTPLG_DET)
1	HDMI_TX2_P
3	HDMI_TX2_N
2	TMDS2_SHLD
4	HDMI_TX1_P
6	HDMI_TX1_N
5	TMDS1_SHLD
7	HDMI_TX0_P
9	HDMI_TX0_N
8	TMDS0_SHLD
10	HDMI_CLK_P
12	HDMI_CLK_N
11	TMDS_CLK_SHLD
15	HDMI_DSCL
16	HDMI_DSDA
13	HDMI_CEC
14	RES
17	DDC_GND
S1–S4	SHIELD

10029449-001RLF — GND, CGND

U4 TPD4E05U06DQAR: HDMI_TX0_P, HDMI_TX0_N, HDMI_TX1_P, HDMI_TX1_N

U5 TPD4E05U06DQAR: HDMI_TX2_P, HDMI_TX2_N, HDMI_CLK_P, HDMI_CLK_N

Title	
Size	A4
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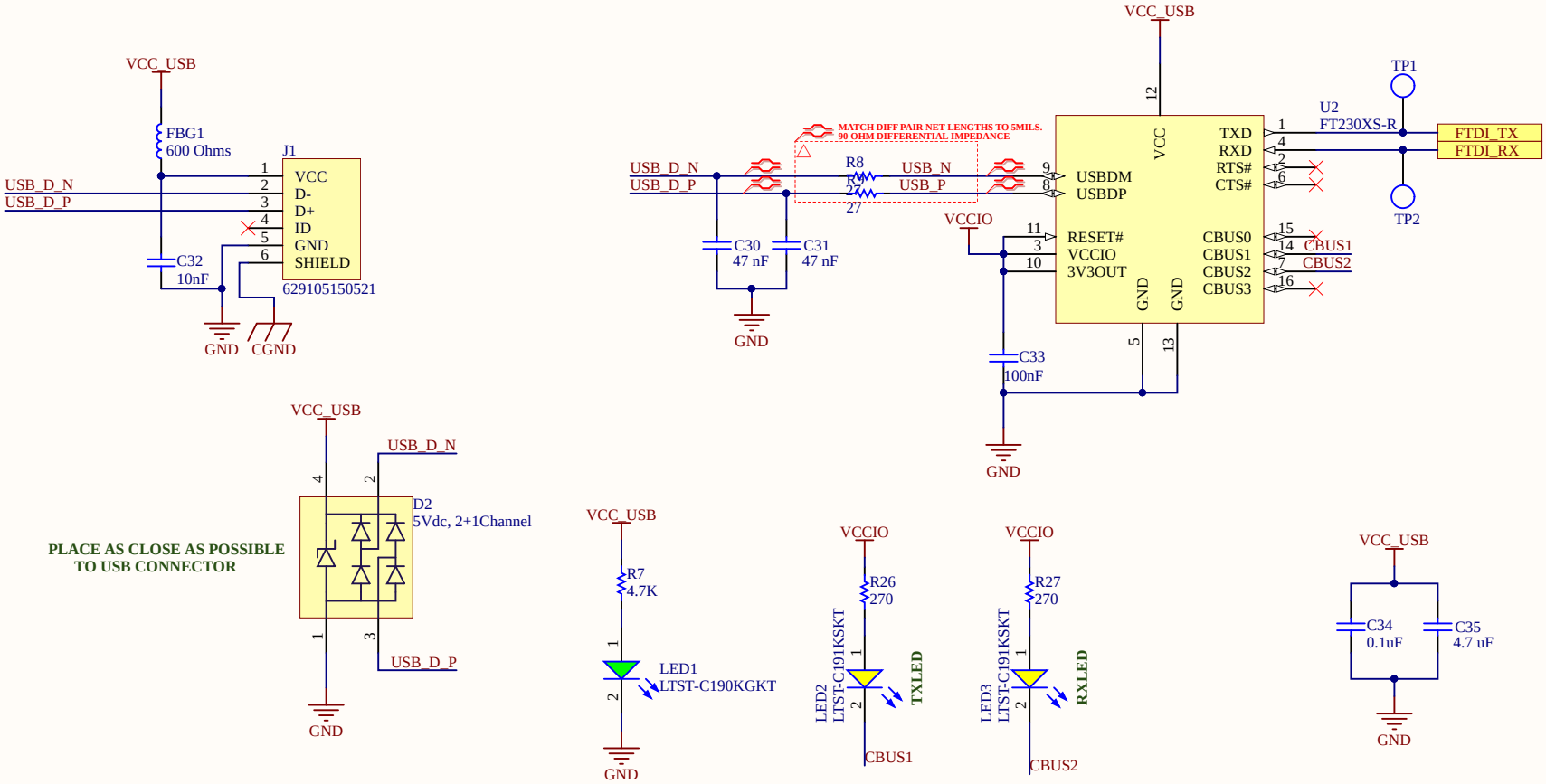
Date:	2020-02-17
Sheet	of
File:	D:\PROJECTS\..\HDMI.SchDoc
Drawn By:	

UART DEBUG: DEBUG PORT.



Title		
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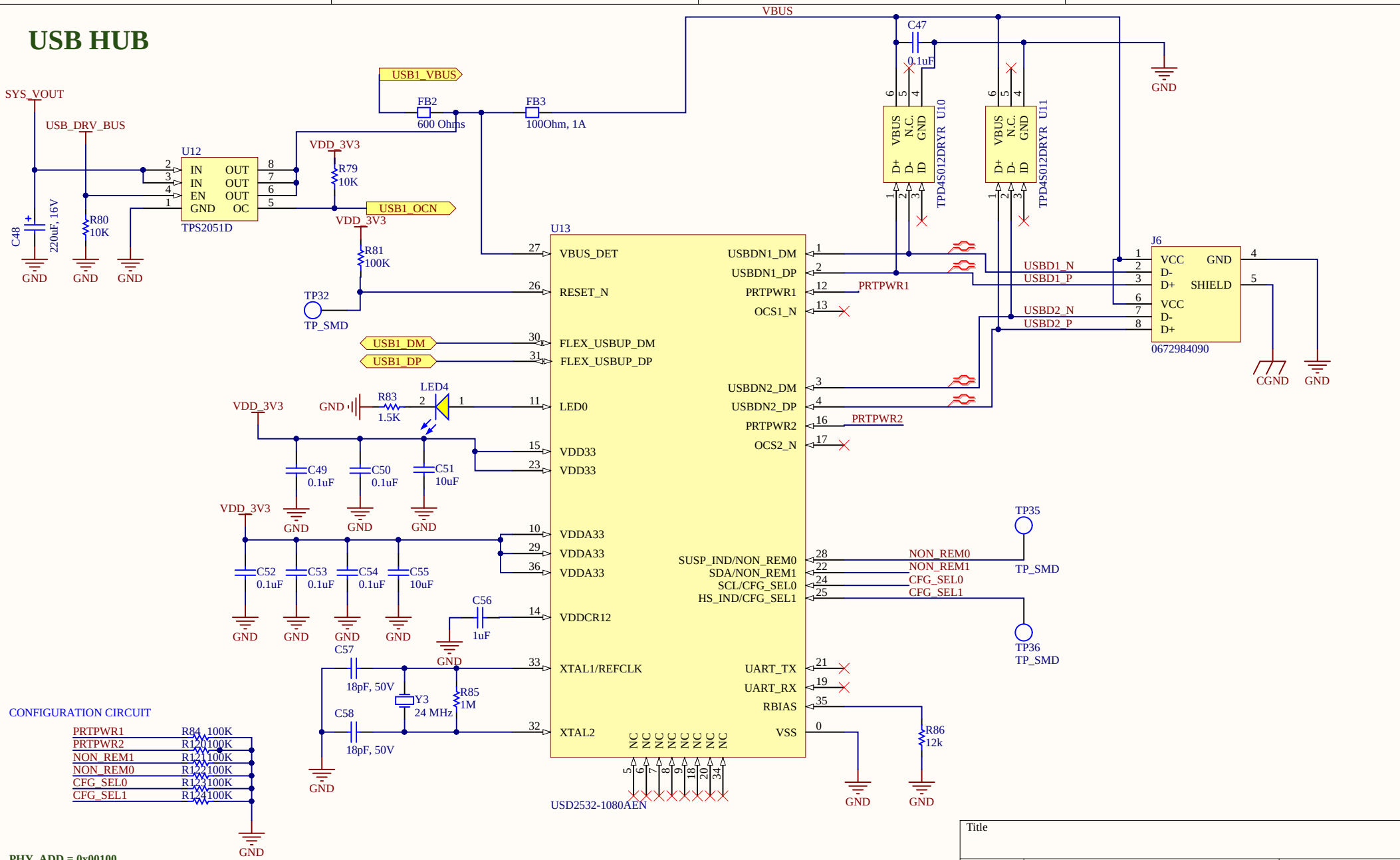
File: D:\PROJECTS\..\P03_UART_Debug.SchDoc	Drawn By:	

USB HUB



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Size: A4	Number	Revision
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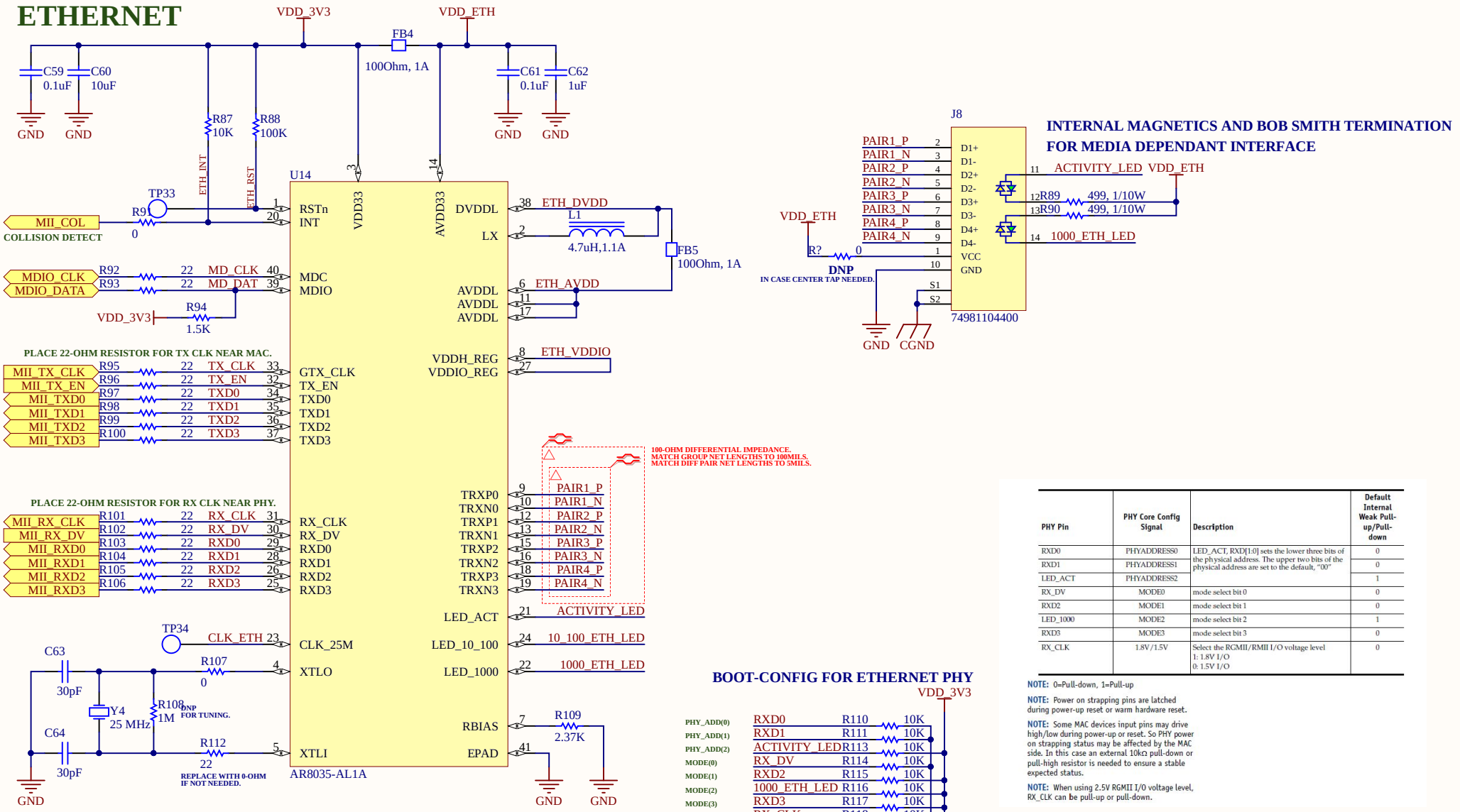
File: D:\PROJECTS\..\P04_USB_hub.SchDoc	Drawn By:	

ETHERNET



INTERNAL MAGNETICS AND BOB SMITH TERMINATION FOR MEDIA DEPENDANT INTERFACE

BOOT-CONFIG FOR ETHERNET PHY

PHY_ADD = 0x00100
MODE = 1100 = PLLON (25M OUT CONTINUOUS)
IO_VOLTAGE = 1.8V
10_100_LED PULLED UP = ACTIVE LOW.

PHY Pin	PHY Core Config Signal	Description	Default Internal Weak Pull-up/Pull-down
RXD0	PHYADDRESS0	LED_ACT, RXD[1:0] sets the lower three bits of the physical address. The upper two bits of the physical address are set to the default, "00"	0
RXD1	PHYADDRESS1		0
LED_ACT	PHYADDRESS2		1
RX_DV	MODE0	mode select bit 0	0
RXD2	MODE1	mode select bit 1	0
LED_1000	MODE2	mode select bit 2	1
RXD3	MODE3	mode select bit 3	0
RX_CLK	1.8V/1.5V	Select the RGMII/RMII I/O voltage level 1: 1.8V I/O 0: 1.5V I/O	0

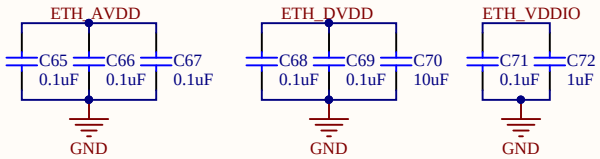
NOTE: 0=Pull-down, 1=Pull-up

NOTE: Power on strapping pins are latched during power-up reset or warm hardware reset.

NOTE: Some MAC devices input pins may drive high/low during power-up or reset. So PHY power on strapping status may be affected by the MAC side. In this case an external 10kΩ pull-down or pull-high resistor is needed to ensure a stable expected status.

NOTE: When using 2.5V RGMII I/O voltage level, RX_CLK can be pull-up or pull-down.

AR8035 DECOUPLING CAPACITORS
PLACE AS CLOSE AS POSSIBLE TO PINS MATCHING NET LABEL.



Title		
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SOM_IO1: UART, SPI, MMC, GPIO, ETC.

TP9
GND

U3C
OSD3358-512M-BSM
OSD3358-512M-BSM

FTDI_RX
FTDI_TX
UART0_CTS
UART0_RTS
TP3
TP8
H2
UART1_TXD
UART1_RXD
UART1_CTS
UART1_RTS
TP16
TP17
H3
SPI0_CLK
SPI0_D0
SPI0_D1
SPI0_CS0
SPI0_CS1
H4
MATCH NET LENGTHS TO 100MIL
MMC0_CLK
MMC0_CMD
MMC0_D0
MMC0_D1
MMC0_D2
MMC0_D3
50-OHM SINGLE-ENDED.
SDIO
SPI1_SCLK
SPI1_D0
SPI1_SC0
AUDIO_CLK

UART0_TXD
UART0_RXD
UART0_CTSN
UART0_RTSN
UART1_TXD
UART1_RXD
UART1_CTSN
UART1_RTSN
SPI0_SCLK
SPI0_D0
SPI0_D1
SPI0_CS0
SPI0_CS1
MMC0_CLK
MMC0_CMD
MMC0_DAT0
MMC0_DAT1
MMC0_DAT2
MMC0_DAT3
MCASP0_ACLKX
MCASP0_FSX
MCASP0_AXR0
MCASP0_AHCLKR
MCASP0_ACLKR
MCASP0_FSR
MCASP0_AXR1
MCASP0_AHCLKX
XDMA_EVENT_INTR0
XDMA_EVENT_INTR1
ECAP0_IN_PWM0_OUT

GPMC_CLK
GPMC_A0
GPMC_A1
GPMC_A2
GPMC_A3
GPMC_A4
GPMC_A5
GPMC_A6
GPMC_A7
GPMC_A8
GPMC_A9
GPMC_A10
GPMC_A11
GPMC_BEN1
GPMC_WAIT0
GPMC_WPN
GPMC_CSN0
GPMC_CSN1
GPMC_CSN2
GPMC_CSN3
GPMC_AD0
GPMC_AD1
GPMC_AD2
GPMC_AD3
GPMC_AD4
GPMC_AD5
GPMC_AD6
GPMC_AD7
GPMC_AD8
GPMC_AD9
GPMC_AD10
GPMC_AD11
GPMC_AD12
GPMC_AD13
GPMC_AD14
GPMC_AD15
GPMC_ADVN_ALE
GPMC_BEN0_CLE
GPMC_WEN
GPMC_OEN_REN

HDMI_INT
USB1_OCN
HDMI_CLKdis
MMC1_CLK_SOM
MMC1_CMD
MMC1_D0
MMC1_D1
MMC1_D2
MMC1_D3
MMC1_D4
MMC1_D5
MMC1_D6
MMC1_D7
MATCH NET LENGTHS TO 100MIL
50-OHM SINGLE-ENDED.
SDIO

MMC1 SD CARD STORAGE FOR LINUX IMAGE BOOT.

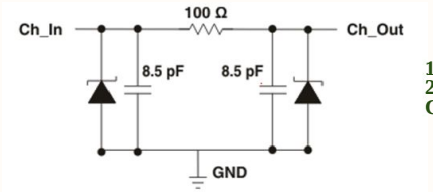
VDD_3V3
C36 10uF
C37 0.1uF
GND
J4
MMC1_D2
MMC1_D3
MMC1_CMD
MMC1_CLK
MMC1_D0
MMC1_D1
MMC1_CD
R28 0
0-OHM AND TEST POINT PROVIDED ON CARD DETECT MECHANISM IF NEEDED.
DATA2
CD/DAT3
CMD
VDD
CLK
VSS
DAT0
DAT1
DT
SW
DETECT SWITCH
SHIELD
5031821852
CGND

DETECT SWITCH

カード挿入時 CARD INSERTING POSITION	クローズ CLOSED
カード未挿入時 NO CARD POSITION	オープン OPEN

VDD_3V3
R29 10K
R30 10K
R31 10K
R32 10K
R33 10K
R34 10K
R35 10K
MMC1_CLK_SOM
R36 22
TP19
U9
CH1_IN CH1_OUT
CH2_IN CH2_OUT
CH3_IN CH3_OUT
CH4_IN CH4_OUT
CH5_IN CH5_OUT
CH6_IN CH6_OUT
CH7_IN CH7_OUT
CH8_IN CH8_OUT
EPAD
TPD8F003DQDR
GND

EMI AND ESD FILTER BLOCK DIAGRAM



12 kV ESD PROTECTION (CONTACT)
25dB @ 1GHz FILTER FOR EMI
CUT-OFF FREQUENCY @ 200MHz

Title		
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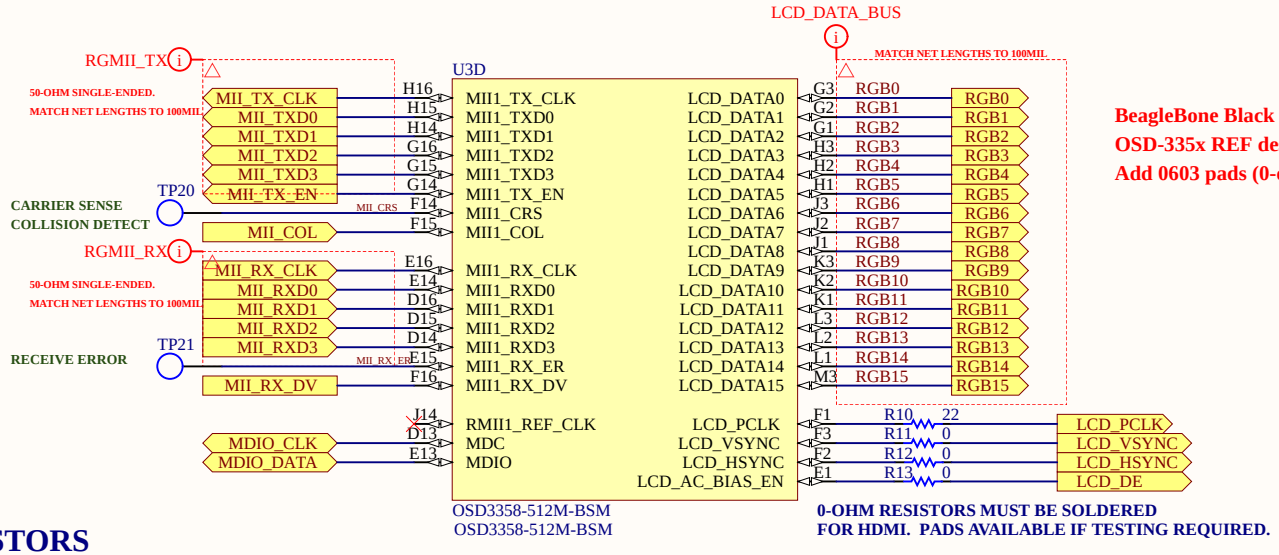
SOM_IO2: ETHERNET AND HDMI.

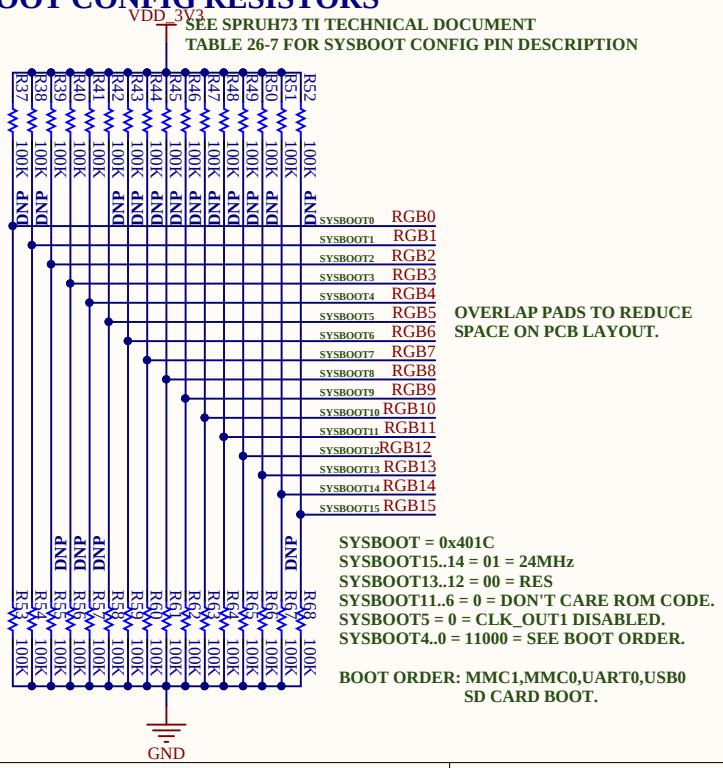


BeagleBone Black Ref design uses 33-ohm resistors in series for each line.
OSD-335x REF design uses none.
Add 0603 pads (0-ohm) for safety?

OSD3358-512M-BSM

0-OHM RESISTORS MUST BE SOLDERED FOR HDMI. PADS AVAILABLE IF TESTING REQUIRED.

BOOT CONFIG RESISTORS



OVERLAP PADS TO REDUCE SPACE ON PCB LAYOUT.

SYSBOOT = 0x401C
SYSBOOT15..14 = 01 = 24MHz
SYSBOOT13..12 = 00 = RES
SYSBOOT11..6 = 0 = DON'T CARE ROM CODE.
SYSBOOT5 = 0 = CLK_OUT1 DISABLED.
SYSBOOT4..0 = 11000 = SEE BOOT ORDER.

BOOT ORDER: MMC1,MMC0,UART0,USB0
SD CARD BOOT.

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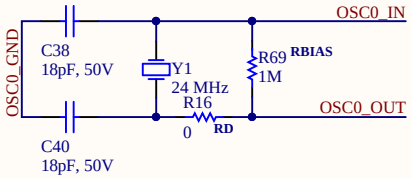
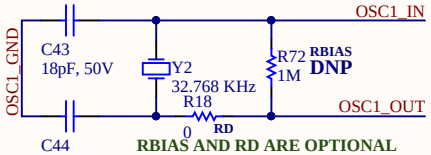
SOM_IO3: CLOCK CRYSTALS, JTAG, USB PORTS, AND ANALOG.

MAIN CLOCK OSCILLATOR



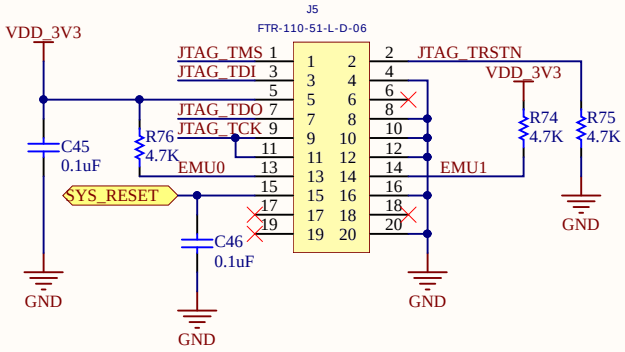
RTC OSCILLATOR



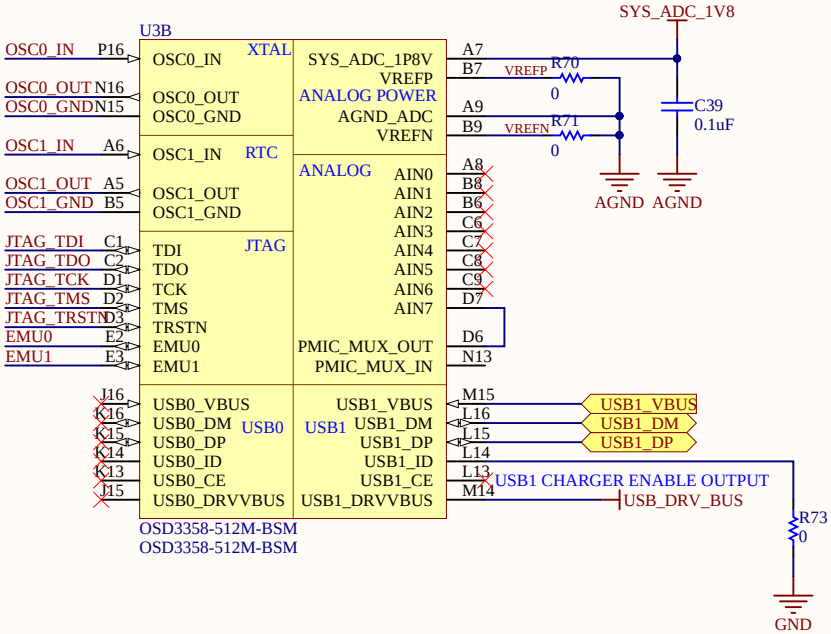
RBIAS AND RD ARE OPTIONAL AND USED TO TUNE THE CRYSTALS.
RD = 0-OHM BY DEFAULT.
RBIAS = DNP BY DEFAULT.

SEE AM335x DATASHEET Tables 6.2 AND 6.5 FOR CRYSTAL REQUIREMENTS.

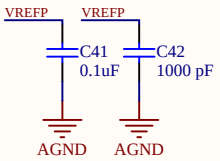
JTAG DEBUG PORT



ADVANCED JTAG FEATURES NOT SUPPORTED
EMU2, EMU3, AND EMU4 NOT CONNECTED.



ANALOG REFERENCE DECOUPLING CAPACITORS



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SOM_POWER: POWER CONNECTIONS AND TEST POINTS.

CONNECT CGND AND GND THROUGH 1206 FOOTPRINT NEAR BARREL JACK CONNECTION.

R82 0 CGND GND

INPUT POWER FROM EXTERNAL POWER SUPPLY.

5V DC IN

J3 PJ-102BH VIN_RAW D3 B520C-13-F F2 2A

MAX SYSTEM POWER SHOULD BE APPROX. 0.8A
MAX POWER DRAW ON VIN_AC = 2A.

5V_IN D4 SMBJ15A C12 220uF, 25V VCC_USB GND GND

SYS VOUT MINIMUM 50uF BULK CAPACITANCE
220uF PLACED NEAR USB HUB.
FOOTPRINT PROVIDED FOR ANOTHER 220uF CAP
RIGHT AT SYS_VOUT OUTPUT.

SYS_5V C13 220uF, 16V GND

TEST POINTS FOR POWER RAILS.

TP10 GND
TP22 5V_IN
TP23 VCC_USB
TP24 SYS_5V
TP25 VDD_3V3
TP26 SYS_RTC_1V8
TP27 SYS_VDD3_3V3
TP28 VDD_1V8
TP29 VDD2_3V3
TP30 SYS_VDD3_3V3
TP31 VDD_1V8

MOUNTING HOLES

M1 MOUNTING_HOLE_4MM
M2 MOUNTING_HOLE_4MM
M3 MOUNTING_HOLE_4MM
M4 MOUNTING_HOLE_4MM
CGND

U3A

P10 R10 T10	VIN_AC VIN_AC VIN_AC	SYS_VOUT SYS_VOUT SYS_VOUT SYS_VOUT	K6 K7 L6 L7
P9 R9 T9	VIN_USB VIN_USB VIN_USB	SYS_VDD1_3P3V SYS_VDD1_3P3V SYS_VDD1_3P3V SYS_VDD1_3P3V	F6 F7 G6 G7
P8 R8 T8	VIN_BAT VIN_BAT VIN_BAT	SYS_VDD2_3P3V SYS_VDD2_3P3V	F11 G11
N7 N6	PMIC_BAT_SENSE PMIC_TS	SYS_RTC_1P8V SYS_RTC_1P8V	K11 L11
T11	PMIC_PB_IN	SYS_VDD3_3P3V SYS_VDD3_3P3V SYS_VDD3_3P3V SYS_VDD3_3P3V SYS_VDD3_3P3V SYS_VDD3_3P3V SYS_VDD3_3P3V SYS_VDD3_3P3V	F8 G8 H7 H8 J7 J8 K8 L8
M13	PMIC_NRESET		
N11 N10	PMIC_PWR_EN PMIC_POWER_EN		
N4 N5	PMIC_LDO_PGOOD RTC_PWRONRSTN		
L4 M4	PMIC_NWAKEUP EXT_WAKEUP	VDDSHV1 VDDSHV2 VDDSHV3 VDDSHV4 VDDSHV5 VDDSHV6	J9 K9 L9 F9 G9 H9
E4 D4	PMIC_NINT EXTINTN		
D10 C10	PMIC_SCL I2C0 I2C0_SCL	SYS_VDD_1P8V SYS_VDD_1P8V SYS_VDD_1P8V SYS_VDD_1P8V SYS_VDD_1P8V SYS_VDD_1P8V SYS_VDD_1P8V SYS_VDD_1P8V	F10 G10 H10 H11 J10 J11 K10 L10
D11 C11	PMIC_SDA I2C0_SDA		
M2	EEPROM_WP *GND to PGM EEPROM		
M16	RTC_KALDO_ENN		
		PMIC_PGOOD PWRONRSTN WARMRSTN	N12 P11 R11

OSD3358-512M-BSM
OSD3358-512M-BSM

POWER BUTTON

PWR_BUTTON S1 GND

FROM DATASHEET: WHEN VIN_BAT NOT USED, CONNECT TO BAT_SENSE. AND LEAVE PMIC_TS FLOATING.

VDD_3V3 R19 1.5K R20 1.5K

I2C0_SCL
I2C0_SDA

4.7K INTERNAL PULL-UPS.
1.5K RESISTORS INCLUDED TO CHANGE PULL-UP VALUE IF NEEDED.

R21 10K GND

TP11 TP12 TP14 TP15 TP16

POR RESET TP18 SYS_RESET

U3F

TP4 TP5 TP6 TP7

F4 G4 F13 G13	VDDS_DDR VDD_CORE VDD_MPU VDDS_PLL	*TEST POINTS ONLY
D5 H6 D12	CAP_VDD_RTC VPP NC	*DO NOT CONNECT NC NC J6 K4

OSD3358-512M-BSM
OSD3358-512M-BSM

U3E

D8 D9 E5 E6 E7 E8 E9 E10 E11 E12 F5 F12 G5 G12 H4 H5 H12 H13	DGND	DGND	J4 J5 J12 J13 K5 K12 L5 L12 M5 M6 M7 M8 M9 M10 M11 M12 N8 N9

OSD3358-512M-BSM
OSD3358-512M-BSM
GND GND

SYS_VDD3_3V3 R22 499, 1/10W R23 10K Q1 MMBT2907A-7-F D5 TLVH431AIDBZR R24 40.2K, 1/10W SYS_RTC_1V8

CLAMPING CIRCUIT IN ORDER TO MAINTAIN 1.55V DIFFERENCE BETWEEN VDD3_3V3 AND RTC_1V8 RAILS DURING POWER DOWN.

WARMRSTN USE CASE #2 ON OCTAVO DESIGN GUIDE.

RESET BUTTON

VDD_3V3 R25 10K R77 0 RESET S2 C14 2.2uF GND GND

POWER ON RESET ELECTRONIC CONTROL

SYS_RTC_1V8 U7 POR NC A GND VCC Y R78 0 RESET SN74LVC1G07DCKR GND

Title			
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