

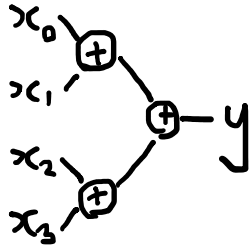
Adding 4 Numbers

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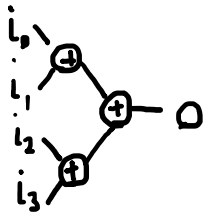
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Algorithm

$$y = x_0 + x_1 + x_2 + x_3$$



Hardware

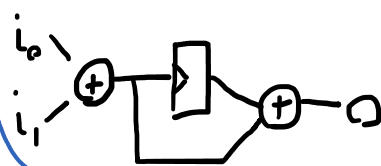


Mapping

i_0	i_1	i_2	i_3	o
x_0	x_1	x_2	x_3	y

transform

Hardware



Mapping

i_0	i_1	o
x_0	x_1	
x_2	x_3	y

For any function there is a simple corresponding combinatorial circuit.

The mapping from the function inputs and outputs to the circuit inputs and outputs is direct.

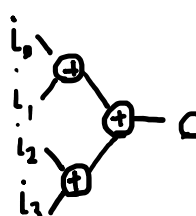
We can make transformations of the (hardware, mapping) pair into a form that doesn't map as directly on the function.

In this example we're changing from feeding in all 4 inputs on the same clock cycle to feeding them in over 2 clock cycles.

Adding 4 Numbers (2)

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Hardware

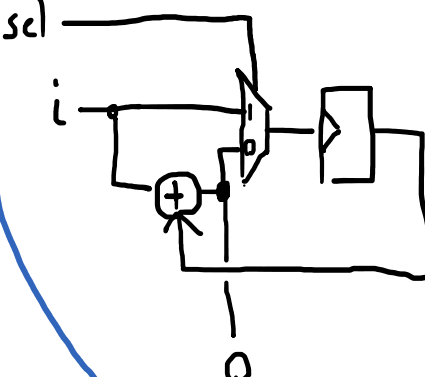


Mapping

i_0	i_1	i_2	i_3	O
x_0	x_1	x_2	x_3	y

More complex transformations can introduce control signals into the mapping.

Hardware

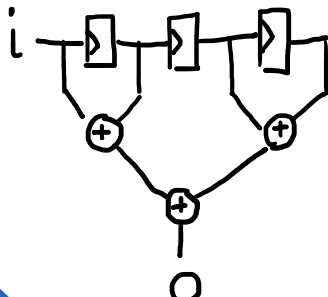


Mapping

i	sel	O
x_0	1	-
x_1	0	-
x_2	0	-
x_3	0	y

A simple inefficient mapping to use 1 input per clock cycle.

Hardware



Mapping

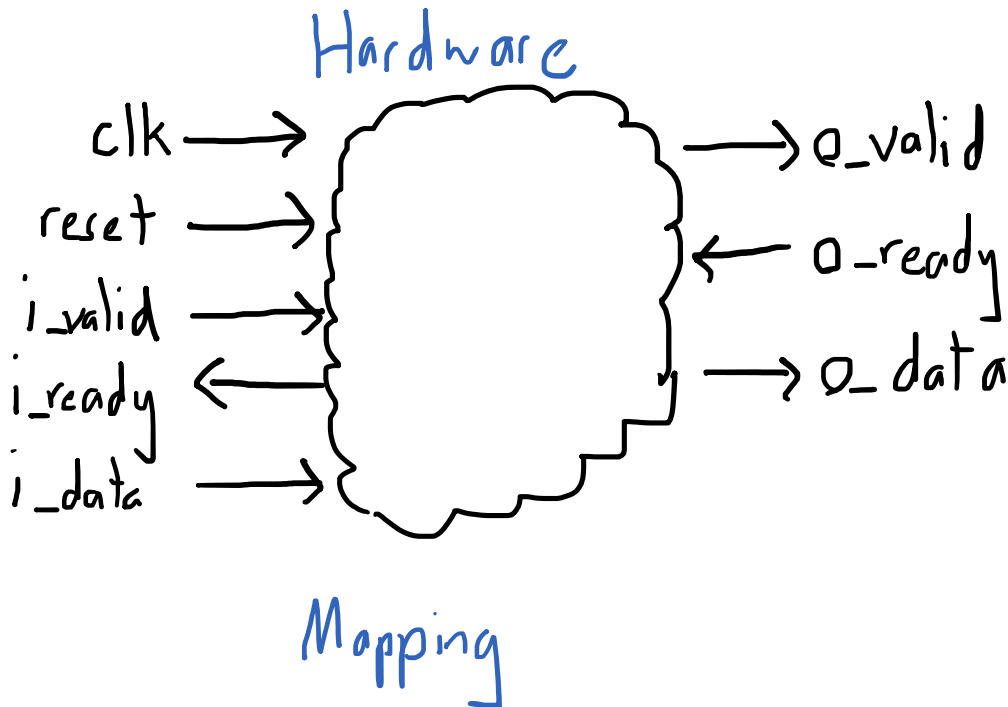
i	O
x_0	-
x_1	-
x_2	-
x_3	y

Adding 4 Numbers (3)

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Once we start getting more complex interface such as valid/ready handshaking the mapping tables that we've been showing become insufficient.

Now the mapping becomes a program itself where which algorithm inputs and outputs correspond to which hardware ports can depend on the input and output control signals of the hardware.



x_0 is the content of i_data after reset the first time i_valid and i_ready are both high.

x_1 is the content of i_data after reset the second time i_valid and i_ready are both high.

...

y is the content of o_data after reset the first time o_valid and o_ready are both high.

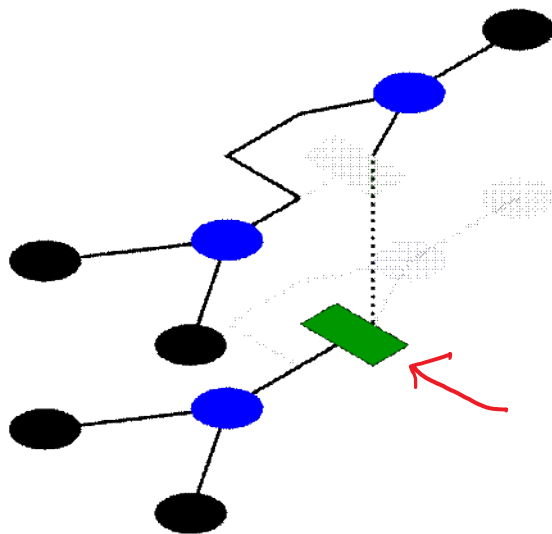
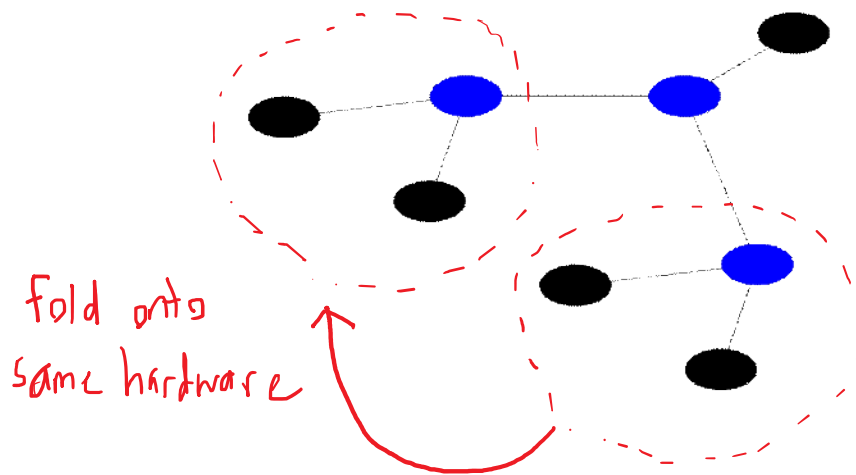
i_valid is unconstrained

o_ready is unconstrained

reset is unconstrained

Hardware reuse visualization

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Introduce register to bridge cycles.