Lab 6

Stopwatch

Design and implement a stopwatch on the FPGA board. Your stopwatch should have the following minimum specifications:

- The time should be displayed on the seven segment display
- The displayed time should be formatted as MM.SS.FF
    - MM: 00 →59 (minutes)
    - SS: 00→59 (seconds)
    - FF: 00→99 (hundredth of a second)
    - Use the decimal point as a separator
- The middle push button should be used as a start/pause/continue
- The CPU reset push button should be used to reset the stopwatch

You are free to decide on any other specification; in other words, make whatever assumption necessary to complete your design.

The provided starter code contains Verilog modules for timers, modulus counters, up/down/load counter, BCD counter, and a three-digit decade counter. Feel free to use any, all, or none of it in your implementation.

Submission check list:

[ ] All Verilog code you generated or modified
[ ] All testbenches written
[ ] Embed all screenshot of your testbench output in your README.md
[ ] Embed all block diagram generated in your README.md
[ ] Short videos demonstrating each of the parts you implemented on the FPGA