Lab 8
Parking lot occupancy counter

Consider a parking lot with a single entry and exit gate. Two pairs of sensors (a, b) are used to monitor the activity of cars. When an object is detected by a sensor, its output is asserted to 1. By monitoring the events of two sensors, we can determine whether a car is entering or exiting or whether a pedestrian is passing through. For example, the following sequence indicates that a car enters the lot:

- Initially, both sensors are off (i.e., the a and b signals are 00)
- Sensor a is triggered (i.e., the a and b signals are 10)
- Both sensors are triggered (i.e., the a and b signals are 11)
- Sensor a is off (i.e., the a and b signals are 01)
- Both sensors become off (i.e., the a and b signals are 00)

Design a parking lot occupancy counter as follows:

1. Design a FSM with two input signals, a and b, and two output signals, `car_enter` and `car_exit`. The `car_enter` and `car_exit` signals assert one clock cycle when a car enters and one clock cycle when a car exists the lot, respectively
2. Include your state diagram or ASM chart with your submission
3. Derive the HDL code for the FSM
4. Figure out a way to use the `car_enter` and `car_exit` signals along with a single up/down counter to show the total number of cars in the parking lot
5. Implement the system on the FPGA board. Use two debounced pushbuttons to mimic the operation of the two sensor outputs. Display the content of the counter on the seven-segment display.

Submission check list:
[ ] All Verilog code you generated or modified
[ ] All testbenches written
[ ] Embed all screenshot of your testbench output in your README.md
[ ] Embed all block diagram or state diagrams generated in your README.md
[ ] Short videos demonstrating each of the parts you implemented on the FPGA