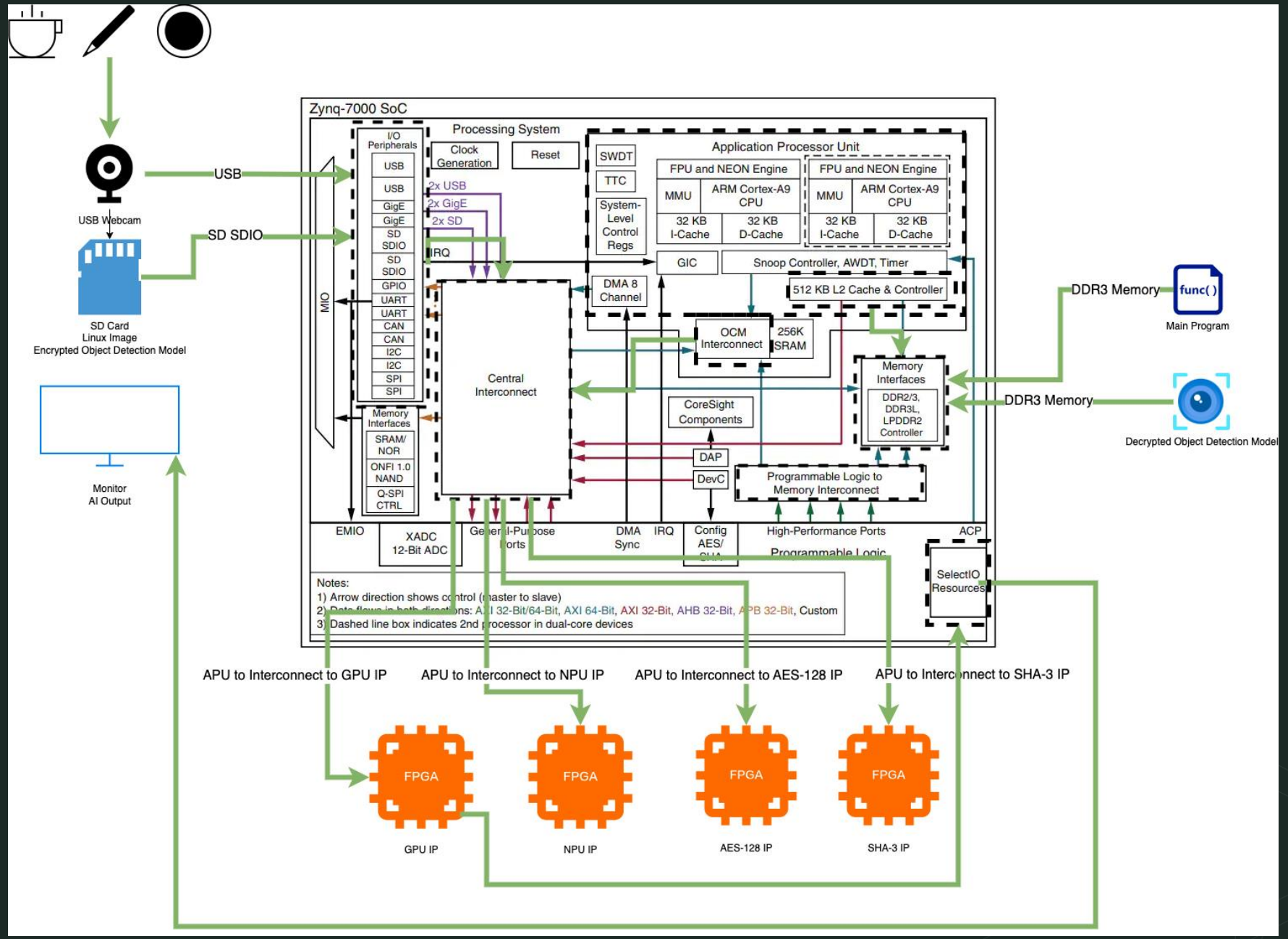
Internal Block Diagram


USB
USB Webcam
SD SDIO
SD Card
Linux Image
Encrypted Object Detection Model
Monitor
AI Output
Zynq-7000 SoC
Processing System
I/O Peripherals
USB
USB
GigE
GigE
SD SDIO
SD SDIO
GPIO
UART
UART
CAN
CAN
I2C
I2C
SPI
SPI
MIO
Clock Generation
Reset
2x USB
2x GigE
2x SD
IRQ
Memory Interfaces
SRAM/ NOR
ONFI 1.0 NAND
Q-SPI CTRL
Central Interconnect
SWDT
TTC
System-Level Control Regs
DMA 8 Channel
Application Processor Unit
FPU and NEON Engine
MMU
ARM Cortex-A9 CPU
32 KB I-Cache
32 KB D-Cache
FPU and NEON Engine
MMU
ARM Cortex-A9 CPU
32 KB I-Cache
32 KB D-Cache
GIC
Snoop Controller, AWDT, Timer
512 KB L2 Cache & Controller
OCM Interconnect
256K SRAM
Memory Interfaces
DDR2/3, DDR3L, LPDDR2 Controller
CoreSight Components
DAP
DevC
Programmable Logic to Memory Interconnect
EMIO
XADC 12-Bit ADC
General-Purpose Ports
DMA Sync
IRQ
Config AES/ SHA
High-Performance Ports
ACP
Programmable Logic
SelectIO Resources
Notes:
1) Arrow direction shows control (master to slave)
2) Data flows in both directions: AXI 32-Bit/64-Bit, AXI 64-Bit, AXI 32-Bit, AHB 32-Bit, APB 32-Bit, Custom
3) Dashed line box indicates 2nd processor in dual-core devices
DDR3 Memory
func( )
Main Program
DDR3 Memory
Decrypted Object Detection Model
APU to Interconnect to GPU IP
APU to Interconnect to NPU IP
APU to Interconnect to AES-128 IP
APU to Interconnect to SHA-3 IP
FPGA
FPGA
FPGA
FPGA
GPU IP
NPU IP
AES-128 IP
SHA-3 IP

Requirements

- (SYS_001) The system shall contain a RoT and performance processor.
- (SYS_002) The RoT shall be an FPGA.
- (SEC_011) The application software shall be encrypted using AES-128 Electronic Code Boot (ECB) (T)
- (SYS_012) The system shall contain a screen that shows the processed image.
- (SYS_019) Upon detection of a person, the system shall illuminate an LED (T), erase the object detection algorithm from the processor and put the system in reset (O).

Progress

- ✓ AES-128 IP
- ✓ GPU IP
- ✓ Camera and Monitor I/O

Next Steps

- NPU IP (Performance Processor)
- SHA-3 IP
- PUF
- LED I/O