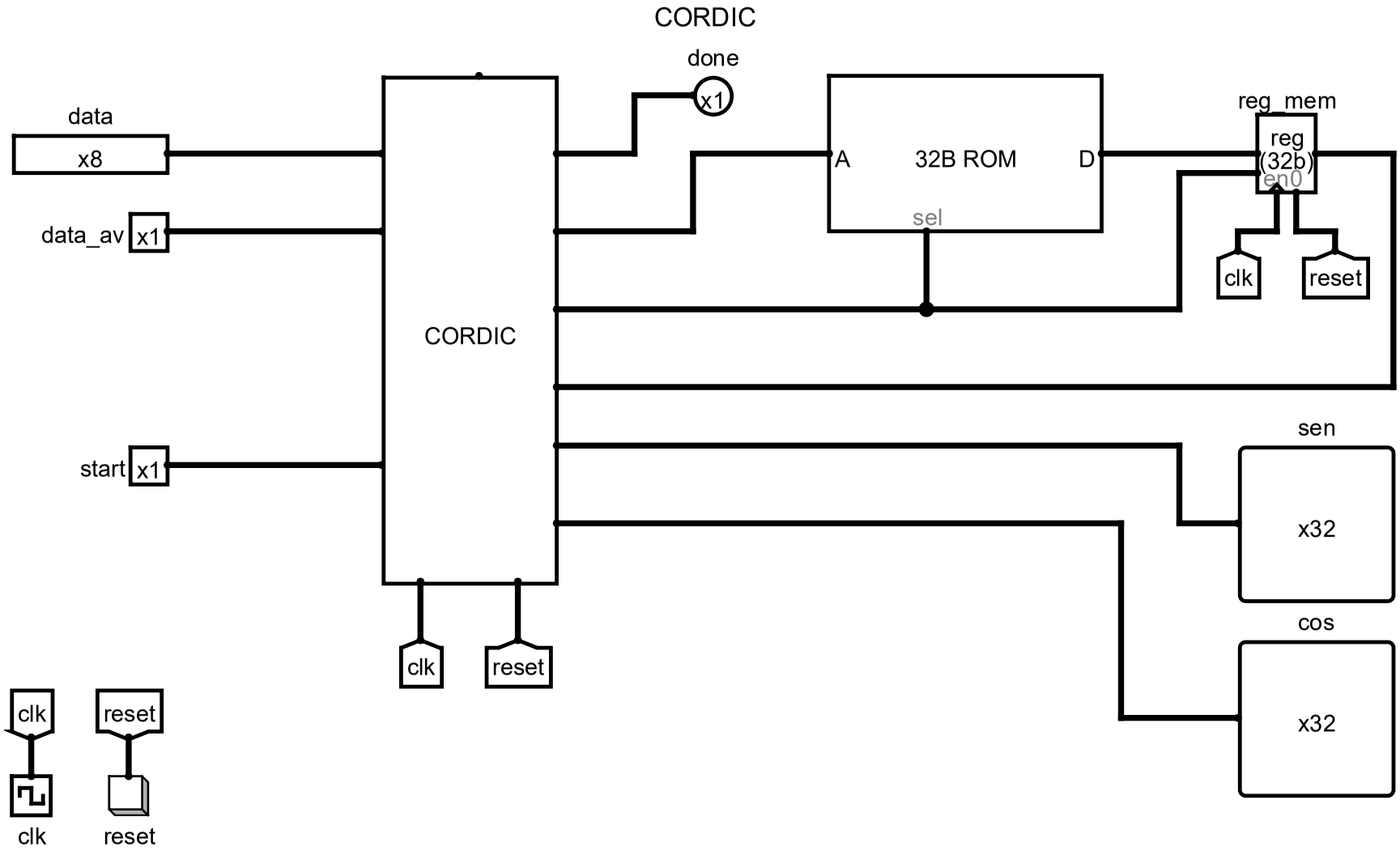
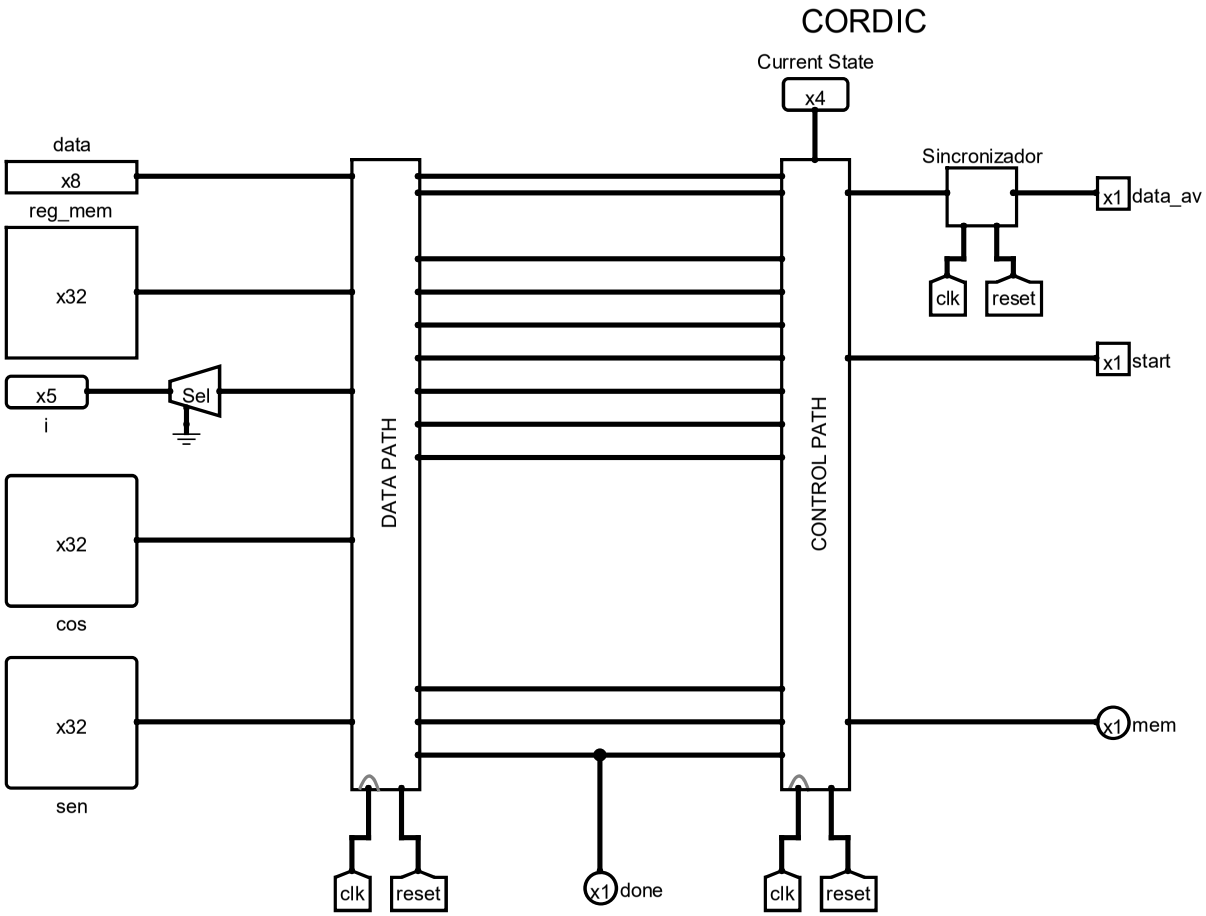
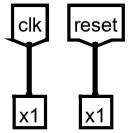
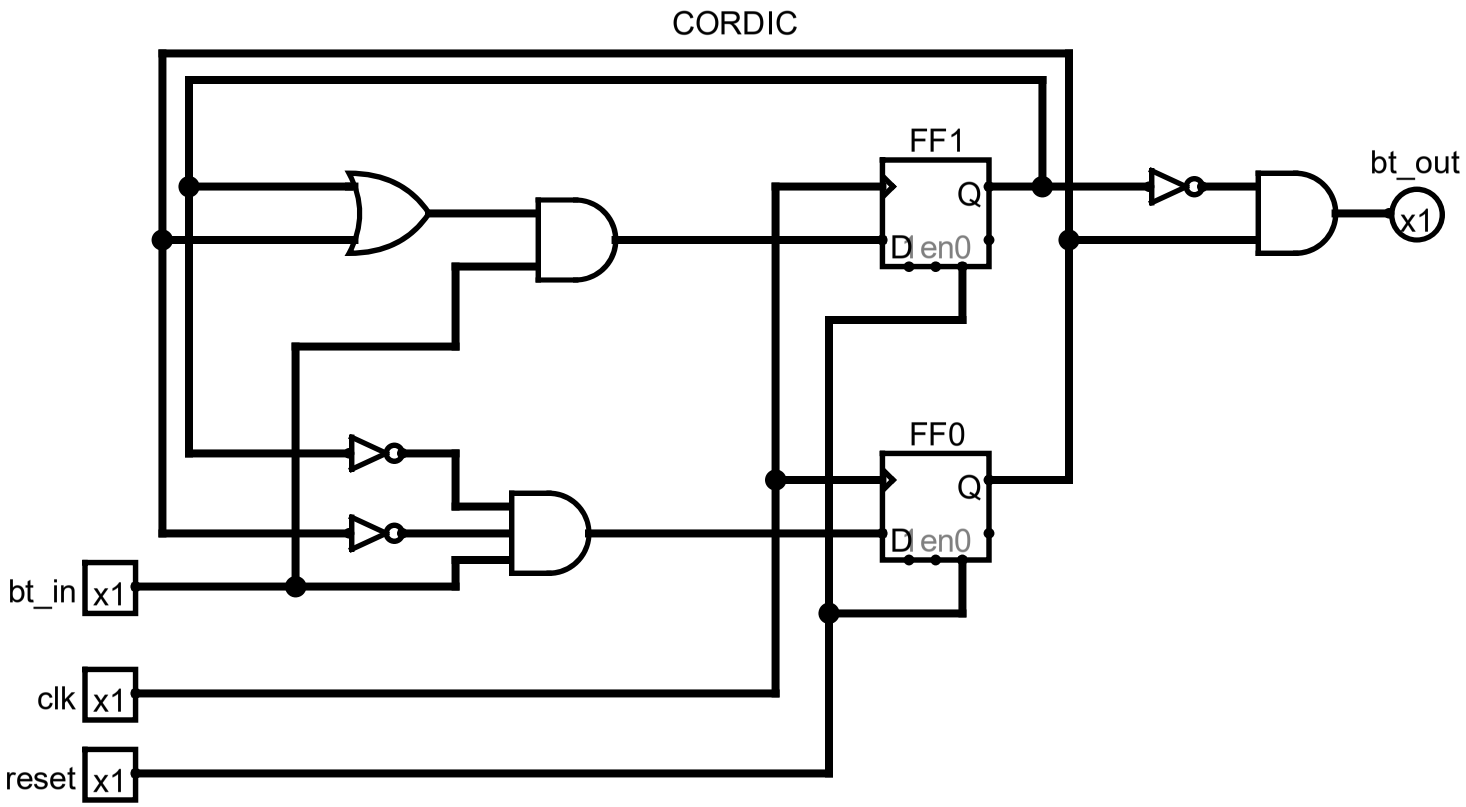
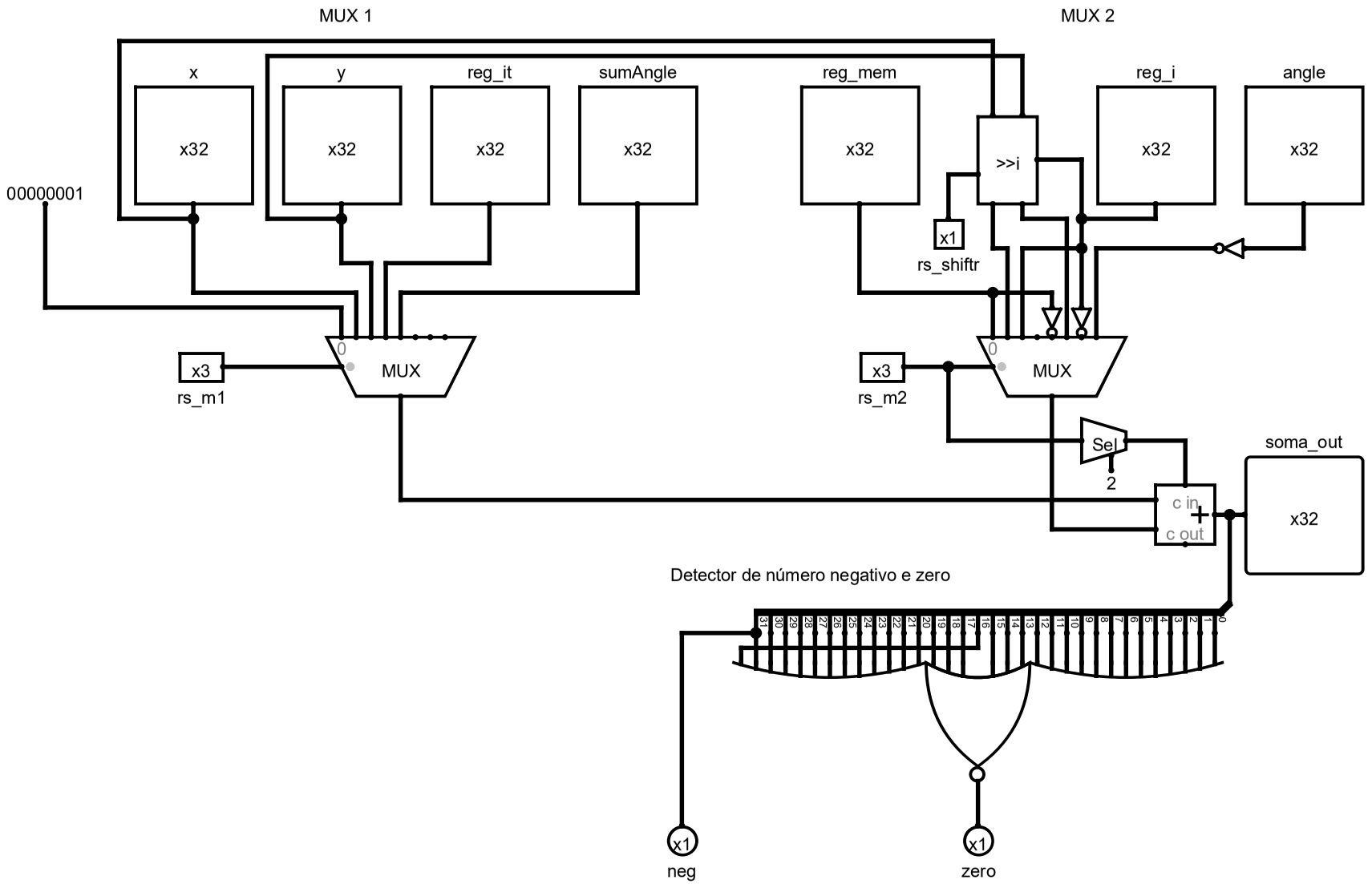

CORDIC
done
x1
data
x8
data_av
x1
start
x1
CORDIC
clk
reset
A
32B ROM
D
sel
reg_mem
reg
(32b)
en0
clk
reset
sen
x32
cos
x32
clk
reset
clk
reset


CORDIC
Current State
x4
data
x8
reg_mem
x32
x5
i
Sel
x32
cos
x32
sen
DATA PATH
CONTROL PATH
Sincronizador
x1
data_av
clk
reset
x1
start
x1
mem
clk
reset
x1
done
clk
reset

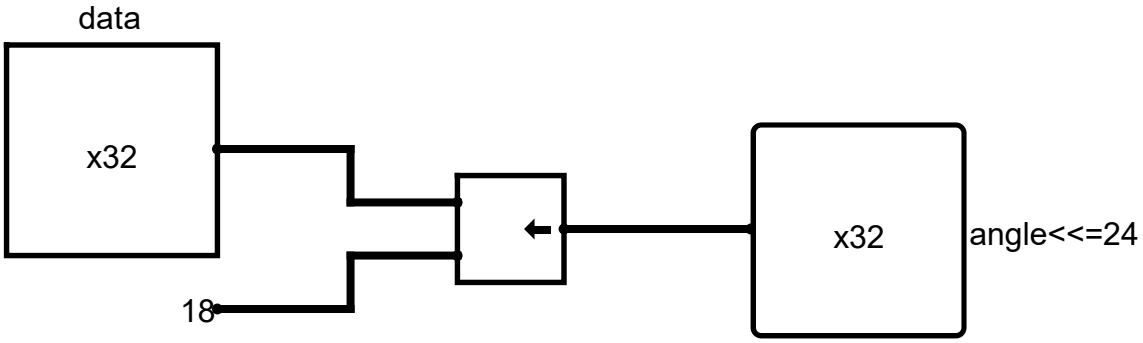

clk
reset
x1
x1

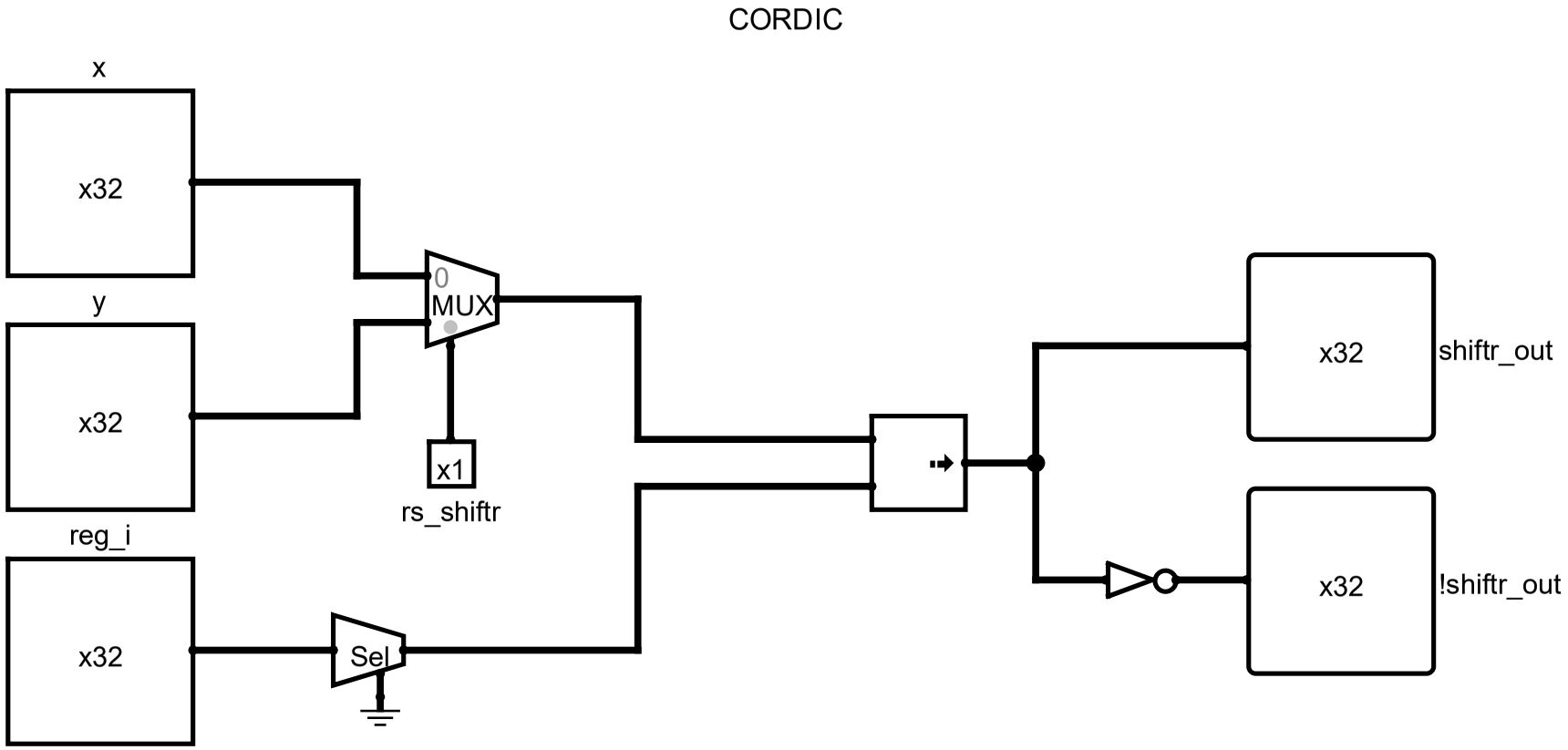

CORDIC
FF1
Q
D
en0
FF0
Q
D
en0
bt_out
x1
bt_in
x1
clk
x1
reset
x1

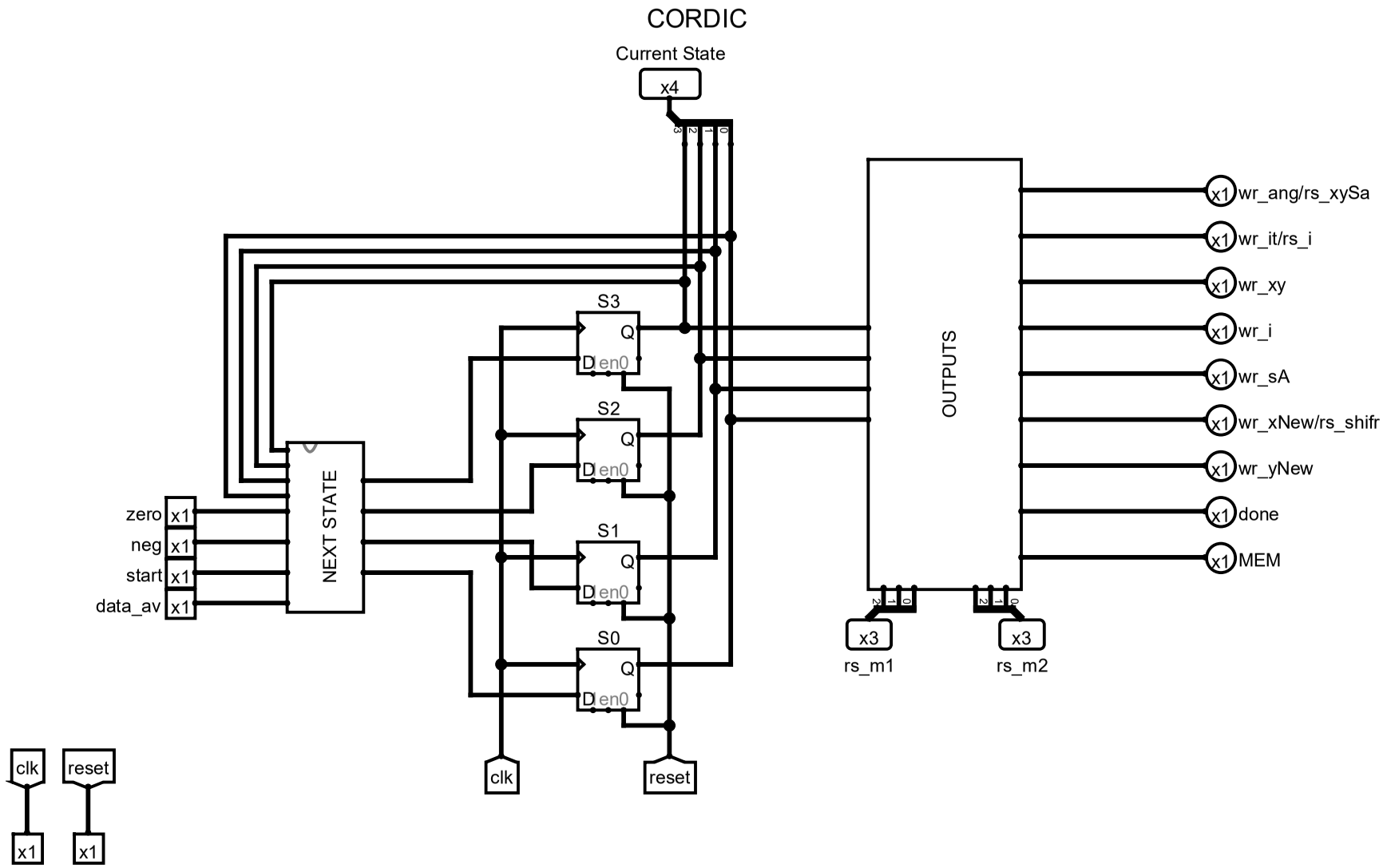
CORDIC


MUX 1
MUX 2
x
y
reg_it
sumAngle
reg_mem
reg_i
angle
x32
x32
x32
x32
x32
>>i
x32
x32
00000001
x1
rs_shiftr
0
MUX
x3
rs_m1
0
MUX
x3
rs_m2
Sel
2
soma_out
c in
c out
x32
Detector de número negativo e zero
31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
x1
neg
x1
zero

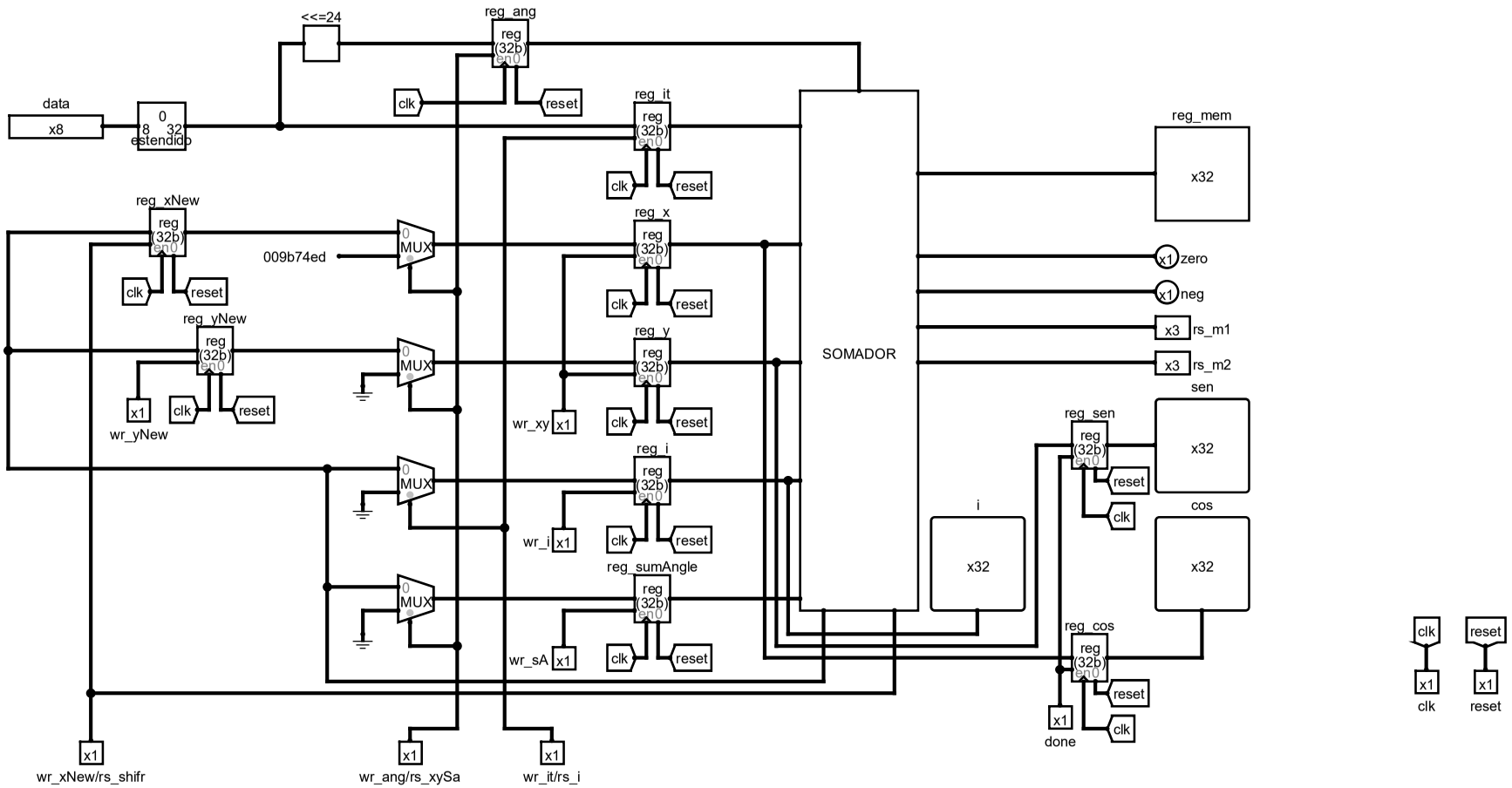
CORDIC



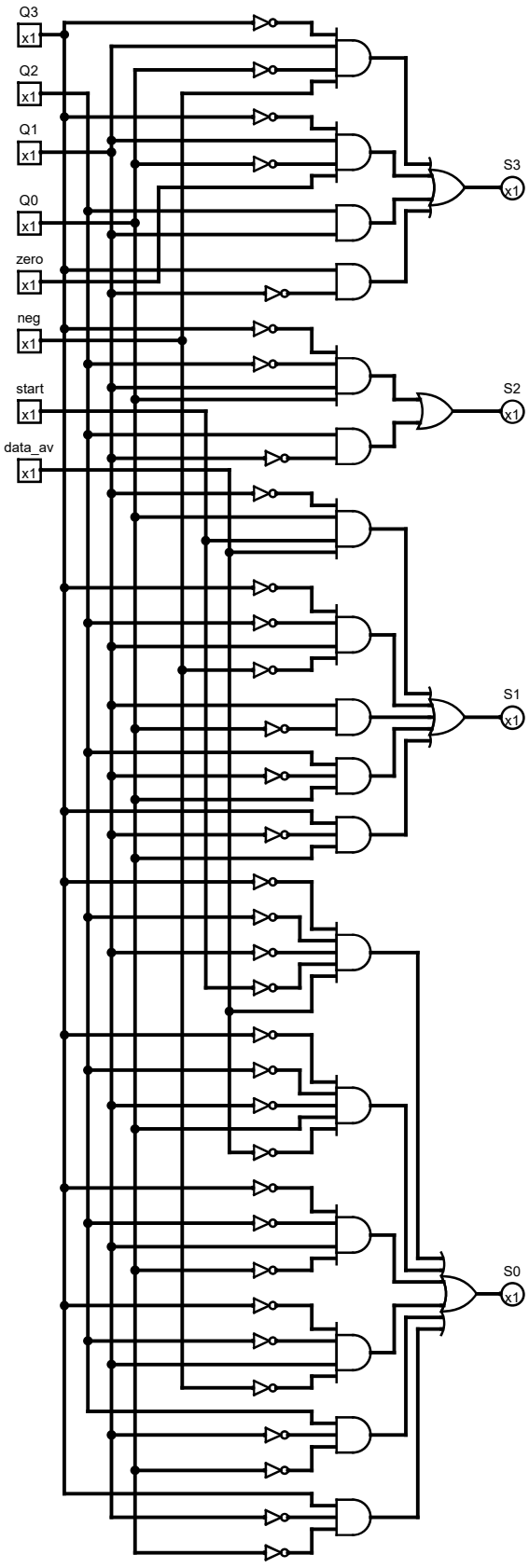

CORDIC
x
x32
y
x32
reg_i
x32
0
MUX
x1
rs_shiftr
Sel
x32
shiftr_out
x32
!shiftr_out


CORDIC
Current State
x4
NEXT STATE
zero
neg
start
data_av
x1
S3
S2
S1
S0
Q
D
en
0
clk
reset
OUTPUTS
wr_ang/rs_xySa
wr_it/rs_i
wr_xy
wr_i
wr_sA
wr_xNew/rs_shifr
wr_yNew
done
MEM
x3
rs_m1
rs_m2

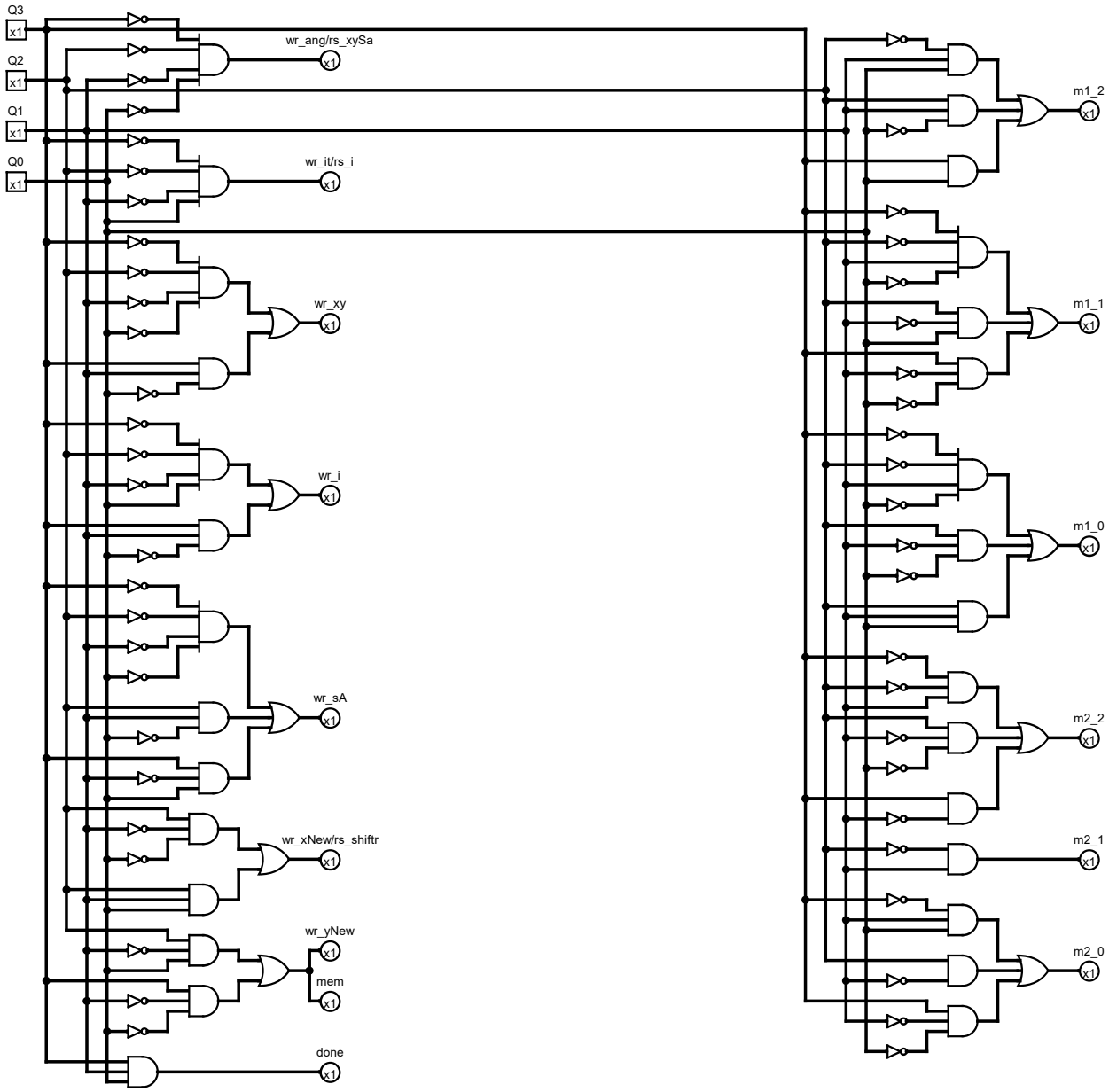
CORDIC


data
x8
0
8 32
estendido
<<=24
reg_ang
reg
(32b)
en0
clk
reset
reg_it
reg_mem
x32
reg_xNew
009b74ed
MUX
reg_x
zero
neg
rs_m1
rs_m2
reg_yNew
reg_y
SOMADOR
wr_yNew
wr_xy
sen
reg_sen
reg_i
wr_i
reg_sumAngle
i
cos
reg_cos
wr_sA
done
wr_xNew/rs_shifr
wr_ang/rs_xySa
wr_it/rs_i

CORDIC


Q3
x1
Q2
x1
Q1
x1
Q0
x1
zero
x1
neg
x1
start
x1
data_av
x1
S3
x1
S2
x1
S1
x1
S0
x1

CORDIC


Q3
x1
Q2
x1
Q1
x1
Q0
x1
wr_ang/rs_xySa
x1
wr_it/rs_i
x1
wr_xy
x1
wr_i
x1
wr_sA
x1
wr_xNew/rs_shiftr
x1
wr_yNew
x1
mem
x1
done
x1
m1_2
x1
m1_1
x1
m1_0
x1
m2_2
x1
m2_1
x1
m2_0
x1