Wii Video + Sound to LCD

logic FPGA design (Phase 1)

picorv32 for GUI management
double frame buffer for LCD (24bit 640x480 = 7,372,800 bits)
GC video lite for controlling protocol

x2 = 16 MB

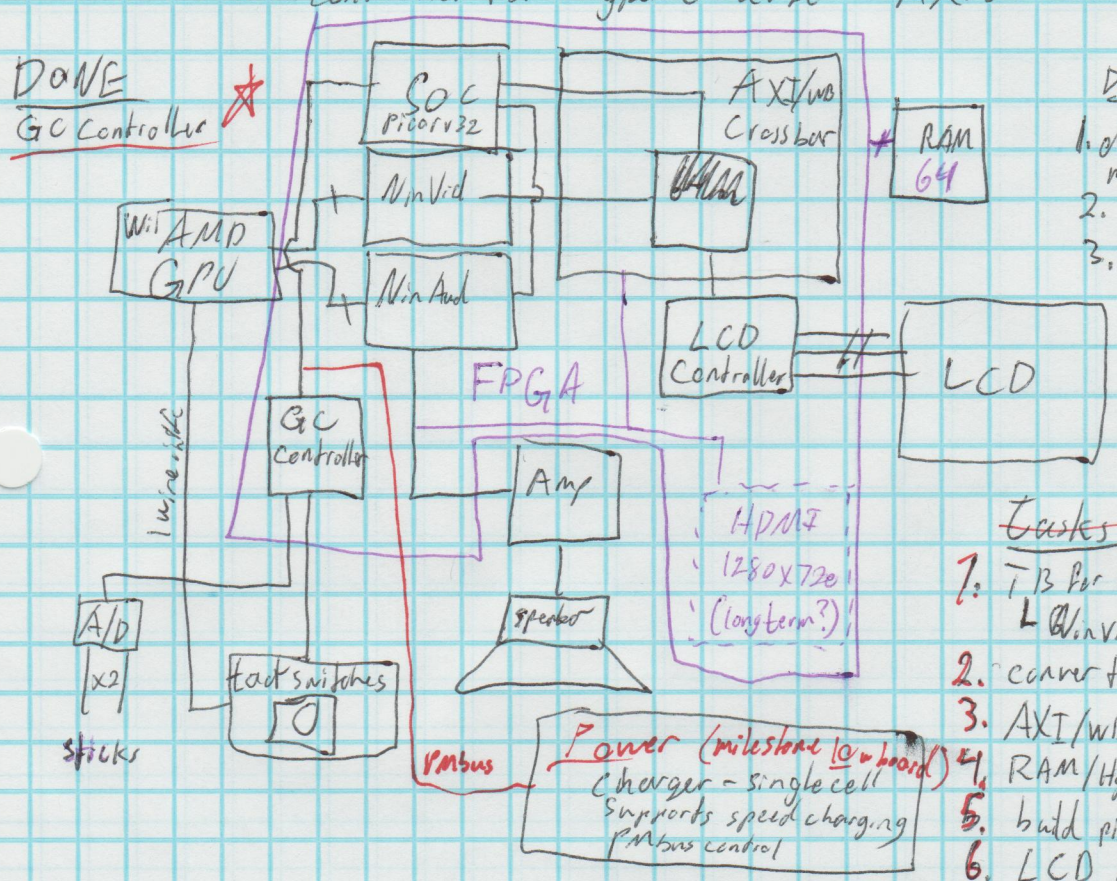
64 Mb = 2^23 bit at least

long term support
1280 x 720 x 24bit = 22,118,400 bits

~~To be done~~

High level

Ram controller for framebuffer AXI or WB crossbar



Done
1. download source materials
2. mixed language sim
3. Git repository

~~Tasks~~ milestones
1. TB for GC video lite
   - Vinvidgen/LCD displays
2. convert GC video to verilog
3. AXI/WB interconnect
4. RAM/Hyperram controller
5. build picorv32 with RAM
6. LCD controller (RAM to LCD)
7. Audio component
8. GC analog conv
9. - 10

Milestone 9

Development board with features to test
10. build board

Memory layout 64 Mbit 0x0 <-> 0x7FFFFF word address
8 Mbytes exactly 8,388,607 bytes

Reserve	0x 0 0 0 0 0 0 <-> 0x 0 F F F F F
Frame Buffer 1	0x 1 0 0 0 0 0 <-> 0x 1 F F F F F
Frame Buffer 2	0x 2 0 0 0 0 0 <-> 0x 2 F F F F F
PicoRV32	0x 3 0 0 0 0 0 <-> 0x 3 F F F F F
Hardware Reserve	0x 4 0 0 0 0 0 <-> 0x 4 F F F F F
HD reserve 3MB	0x 5 0 0 0 0 0 <-> 0x 5 F F F F F
	0x 6 0 0 0 0 0 <-> 0x 6 F F F F F
	0x 7 0 0 0 0 0 <-> 0x 7 F F F F F

Phase 2 is adapting ~~wii~~ onto Devboard