MERCURY WHITE PAPER

Cell Architecture Advantages for Computationally Intensive Applications

Computer Systems, Inc.
MERCURY

THE CELL BE PROCESSOR

The Cell Broadband Engine (BE) processor is the result of collaboration among the Sony Group, IBM, and Toshiba companies. Because traditional processors could not deliver the computational power required for next-generation digital media devices such as game consoles and interactive televisions, these companies set out to design a new multicore processor that would achieve a quantum leap in performance for these applications.

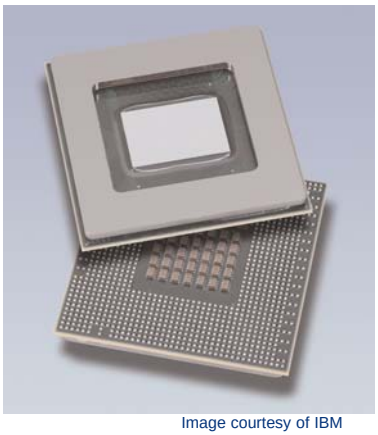

Image courtesy of IBM

Figure 1. Cell BE Processor

The original project was driven by the entertainment industry's needs. The companies recognized, however, that the characteristics of the design promised dramatic performance advantages for a much wider range of applications. With that in mind, they decided to develop an open, Linux®-based software development environment to encourage a broad adoption of this new multicore architecture.

In 2004, IBM and Mercury Computer Systems joined forces to develop Cell-based solutions with dramatically improved performance for signal and image processing, computationally intensive applications. Mercury and IBM have begun working together to develop Cell-based products for challenging applications such as radar, sonar, MRI, digital X-ray, and many others, which can now be taken to new heights of sophistication and performance.

CELL BE PROCESSOR ARCHITECTURE

A Multicomputer-on-a-Chip

The architecture of the Cell BE processor features nine microprocessors on just one chip: eight synergistic processor elements (SPEs) and a Power Architecture™ compliant core, the power processor element (PPE), which orchestrates their activities. The element interconnect bus (EIB) provides the internal communication among the processors and is capable of moving 96 bytes/cycle. The heterogeneous, high-performance processing elements on a common interconnect have a structure that is designed for distributed processing. This revolutionary architecture is essentially a multicomputer-on-a-chip.

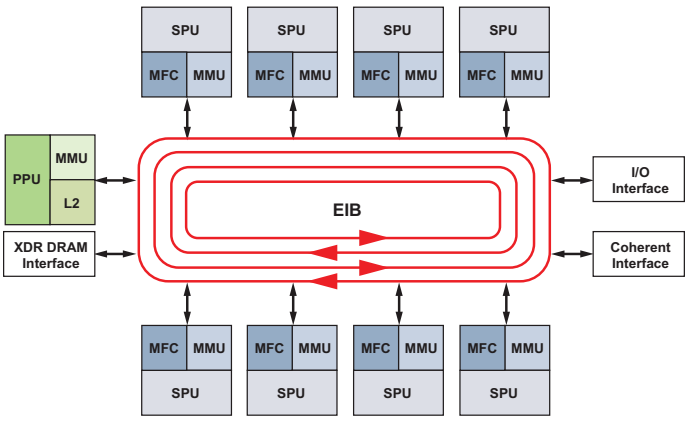

Figure 2. Cell BE Processor functional block diagram

The Cell BE processor has well balanced I/O and memory bandwidth. In addition to the 96 bytes/cycle of internal I/O provided by the EIB, the XDR™ DRAM memory controller is capable of a peak rate of 24 GB/s to main memory. Aggressive packaging and I/O technology from Rambus provide a large amount of off-chip bandwidth. The Flex™ I/O interface has both a cache-coherent interface for connecting two Cell BE processors together and a non-coherent I/O interface, for a combined 60 GB/s of bandwidth.

The most impressive performance is achieved for 32-bit floating-point math operations, with peak performance of 192 GFLOPS from just the 8 SPEs alone. Because the SPEs are full 128-bit SIMD (single instruction, multiple data) units, data sizes include 32-bit and 64-bit double-precision floating-point, with 8-bit and 16-bit integer also possible. When mapping real applications onto the Cell BE processor, Mercury has seen performance improvements of 5 to 100 times that of currently available high-volume processors and estimated performance-per-watt improvements ranging from 3 to 10 times that of other available solutions.

CELL ARCHITECTURE ADVANTAGES

The processing power of the Cell BE processor results from its performance-leading architectural design, which provides a number of advantages for computationally intensive applications. The Cell BE processor has peak performance in excess of 200 GFLOPS, or 200 billion floating-point operations per second.

Faster Processing of Compute-Intensive Algorithms

With the combination of single-precision 32-bit floating-point and 16-bit integer (or fixed-point) processing, the Cell BE processor handles compute-intensive algorithms and is particularly impressive for those requiring many floating-point calculations. SAR (synthetic aperture radar) is an example of a compute-intensive algorithm that can be accelerated by the Cell BE processor. The Cell BE processor can also enable advanced SAR techniques with higher resolution.

Bandwidth and Interconnect Flexibility inside the Chip

Each SPE contains a 256 KB high-speed local store and a DMA (direct memory access) engine for moving data and code to and from XDR memory and even to other SPEs – all via the EIB interconnect. The DMA engine can simultaneously read and write at the rate of 24 GB/s to and from the EIB and can handle numerous outstanding DMA requests.

Backward Compatibility with PowerPC Applications
Because the Cell architecture is compatible with PowerPC® processors, existing PowerPC applications can run on the Cell BE processor without modification. This flexibility provides a convenient entry point for programmers with symmetric multiprocessor (SMP) experience and eases the porting of existing software, including the operating system, to the Cell architecture.

Low Voltage/Low Power with High Performance/High Frequency
The small number of gates per cycle enables the Cell BE processor to operate at low voltage and low power while maintaining high performance and high frequency. By using the SIMD architecture for both the vector media extensions (VMX) on the PPE and the instruction set of the SPEs, both performance and power efficiency are improved. These attributes contribute to the usefulness of the Cell architecture for the space-constrained, weight- and power-sensitive applications required on many airborne, ocean-going, and land-based platforms in the aerospace and defense industry.

Massive I/O Data Bandwidth
Each SPE resembles a floating-point SIMD DSP chip with 128 registers, 256 KB of local memory, and asynchronous coherent DMA to the global address space. For the massive number crunching required in seismic applications, this acceleration of data movement can increase the effectiveness and speed of image reconstruction by an order of magnitude.

Efficient Communication and Ease of Programming
The Cell BE processor's high-bandwidth memory and on-chip, coherent, high-bandwidth EIB deliver higher performance on memory bandwidth-intensive applications by enabling high-bandwidth internal interactions among the SPEs and the PPE. This coherency allows the SPEs and the PPE to share a single address space for efficient communication and ease of programming.

The flexible, high-bandwidth I/O can be configured to support many different system designs, including a single-chip configuration with dual I/O interfaces or a coherent dual-processor configuration without the need for switch chips to connect the two processors.

Maximized Performance per Watt and per Square Millimeter of Silicon
The Cell architecture includes support for chip power management, thermal management, manufacturing test, hardware and software debugging, and performance analysis. To help satisfy the design requirements, a high-performance, low-cost packaging technology and high-performance, low-power 90-nm SOI technology are implemented.

These features are particularly important for telecommunications base stations, for which Mercury's expertise in providing high performance/watt and high computer power/area can now be enhanced by the Cell BE processor to more efficiently satisfy these requirements.

CELL BE PROCESSOR APPLICATION ADVANTAGES

The Cell BE processor is well suited to the related requirements of image and signal processing algorithms. In particular, it easily handles many floating-point calculations such as physics computations, video rendering, large arrays, and compute-intensive algorithms. These algorithms increase video resolution, resulting in clearer pictures and video in real time. They also make possible large FFT processing; higher-resolution medical images; advanced SAR; improved quality and yield in semiconductor wafer inspection; and real-time surveillance, security, and reconnaissance. Future promising applications include aerospace tracking and imaging; remote transmission and analysis of digital X-rays, MRIs, and ultrasounds; real-time accident avoidance for vehicles, vessels and aircraft; and other as yet unknown applications that will become technically feasible and affordable.

Medical Imaging
In medical image reconstruction, the complexity of the computation arises from two issues:

- De-noising of the input data and enhancement of edges – Current techniques adopt multi- dimensional adaptive filtering to enable taking the very nature of the noise into account to filter it out of the input data, and then keeping the relevant information in the images.

- Reconstruction of a 3D or 4D volume from 2D views – Current systems have an acquisition rate of several GB/s, which makes real-time processing almost impossible for traditional PC-based systems. 4D volumes are even more challenging, because they incorporate three dimensions in space plus one dimension in time for the display of moving 3D images such as a beating heart.

The advantages of the Cell architecture directly address the major requirements of current medical imaging modalities. The Cell BE processor can deliver high-quality images at an unprecedented rate. Radiologists and surgeons will be able to make accurate diagnosis and surgery decisions faster, based on better quality images with higher resolution in real-time.

To take full advantage of the high-resolution anatomic images generated by CT scanners, powerful visualization and analysis tools are essential. The reconstruction process has traditionally been viewed as the bottleneck in the diagnostic workflow. However, Cell technology-based reconstruction can deliver higher-resolution images at order-of-magnitude faster reconstruction times over existing technologies.

Aerospace and Defense
With its high performance per watt, the Cell BE processor is appropriate for portable, weight-sensitive and airborne applications (portable ultrasound, unmanned surveillance, and military identification and targeting). Automatic target recognition (ATR), time-sensitive targeting, network-centric warfare, and real-time continual surveillance and reconnaissance (ISR) are all enhanced with the faster image processing the Cell BE processor delivers. The ATR algorithm, used for classifying radar images such as a tank, bus, or track vehicle, includes as many as 140 different threat models running on a system with 64 conventional processors. Other defense algorithms use up to 480 conventional processors.

The Cell BE processor can dramatically reduce the size of these systems by providing greater density, enabling large algorithms to run efficiently. For example, synthetic aperture radar (SAR) systems create images of the ground from moving aerial or spaceborne platforms. These systems provide rich information, but require exceptional computational power to execute their sophisticated processing algorithms. SAR is critical for many all-weather tactical operations such as weapon targeting, but formation of a SAR image can require billions of arithmetic operations. The Cell BE processor can enable advanced SAR techniques and higher resolutions, providing war fighters with higher quality actionable information from a system sized as much as 10 times smaller than systems with comparable processing capabilities.

Semiconductor Inspection
For semiconductor wafer inspection, mask inspection, and mask writing, the Cell BE processor's high density and large I/O memory bandwidth facilitate development and reduce the cost of the inspection process, enabling the development of denser dies manufactured at a lower cost.

Telecommunications
In telecommunications, heat dissipation, power requirements, cooling requirements, and size are the relevant design constraints. The density of the Cell BE processor and its performance per watt enable additional processing performance for added channels with streaming content in base stations and cell phone repeaters.

Multimedia
Providing multimedia images in near real-time can expedite informed decision-making and enable the recipients to receive the images and decisions sooner. The Cell BE processor can make many multimedia applications possible and cost-effective, including high-resolution image and video transmission of security, surveillance, homeland security, and natural disasters.

Future Applications
The Cell BE processor can process algorithms that were previously limited by performance constraints. It virtually eliminates the need for custom ASICs and reduces chip count by satisfying many processing requirements on-chip. Complex problems that either required hundreds of processors or ran too slowly for time-sensitive applications can run on the Cell BE processor up to two orders-of-magnitude faster. This enables more complex applications to obtain faster, more useful results at higher resolution.

For many applications, the Cell BE processor reduces the size, number, and power requirements of the processors needed. On a processor-by-processor basis, the Cell BE processor is an order-of-magnitude faster than other types of processors. This results in a single Cell BE processor outperforming many individual processors, doing more processing, or running applications that developers have only dreamed as possible.

Researchers are continually developing algorithms that can produce clearer pictures or improved results, but these algorithms are sometimes too computationally complex to field; the computation costs more than the users can afford to pay, or it cannot be run at an acceptable performance level. With the Cell BE processor, these algorithms that are "waiting in the wings" may eventually deliver the increased price performance to make them affordable.

THE MERCURY/IBM PARTNERSHIP

While IBM and Mercury have been working together over the years, the relationship has been strengthened by our recent partnership to jointly develop solutions based on the Cell BE processor. Both firms are committed to customer success. Our highly complementary capabilities can benefit customers as we join forces to solve challenging problems for computationally intensive applications. IBM contributes the Cell technology; Mercury brings unique domain expertise in several industries. IBM has an unmatched portfolio of technology and IP; Mercury has been optimizing compute-intensive algorithms for 20 years. IBM offers a broad software infrastructure; Mercury has developed a set of libraries and tools to map challenging applications to specialized processing elements.

THE MULTICORE PLUS™ ADVANTAGE

Multicore processors have arrived. All the major silicon manufacturers have included multicore processors on their roadmaps as they battle the barriers of physics. Along with the quantum leap in processing power and the extreme density of these chips come new programming, cooling, and optimization challenges. With our many years of experience developing and programming complex multicomputer systems, Mercury's expertise is ideally suited to assist with these challenges.

Mercury's MultiCore Plus Advantage employs sophisticated middleware that abstracts hardware capabilities and manages the distribution of data across multiple computing elements working in tandem. By leveraging the MultiCore Plus Advantage from Mercury, our customers can benefit from our patented cooling technologies, lightweight SOC management software, multicore implementations of key algorithms, visualization tools designed for clusters, algorithm tuning, and more.

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