Results

Results for "DebraizeFixed_Wrapper" entity:

A) Resource Utilizations

Component	Value
LUTS	521
Slices	187
Flip-Flops	169
LUT-FF pairs	--
BRAMs	0
DSP units	0

- The results are generated for n=4 and k=8.
- The results are based on implementation reports.
- After synthesizing the design by a dual-port RAM the resource utilization exceeds in terms of LUTs. Therefore, the design has been changed to use 2 RAMs to store the table. The results are based on new architecture.

B) Timing Analysis

Parameter	Value
Minimum Clock Period	9.198ns
Maximum Clock Frequency	108 MHz
Maximum Throughput	Varys based on n, k and the circuit of generating test-vectors