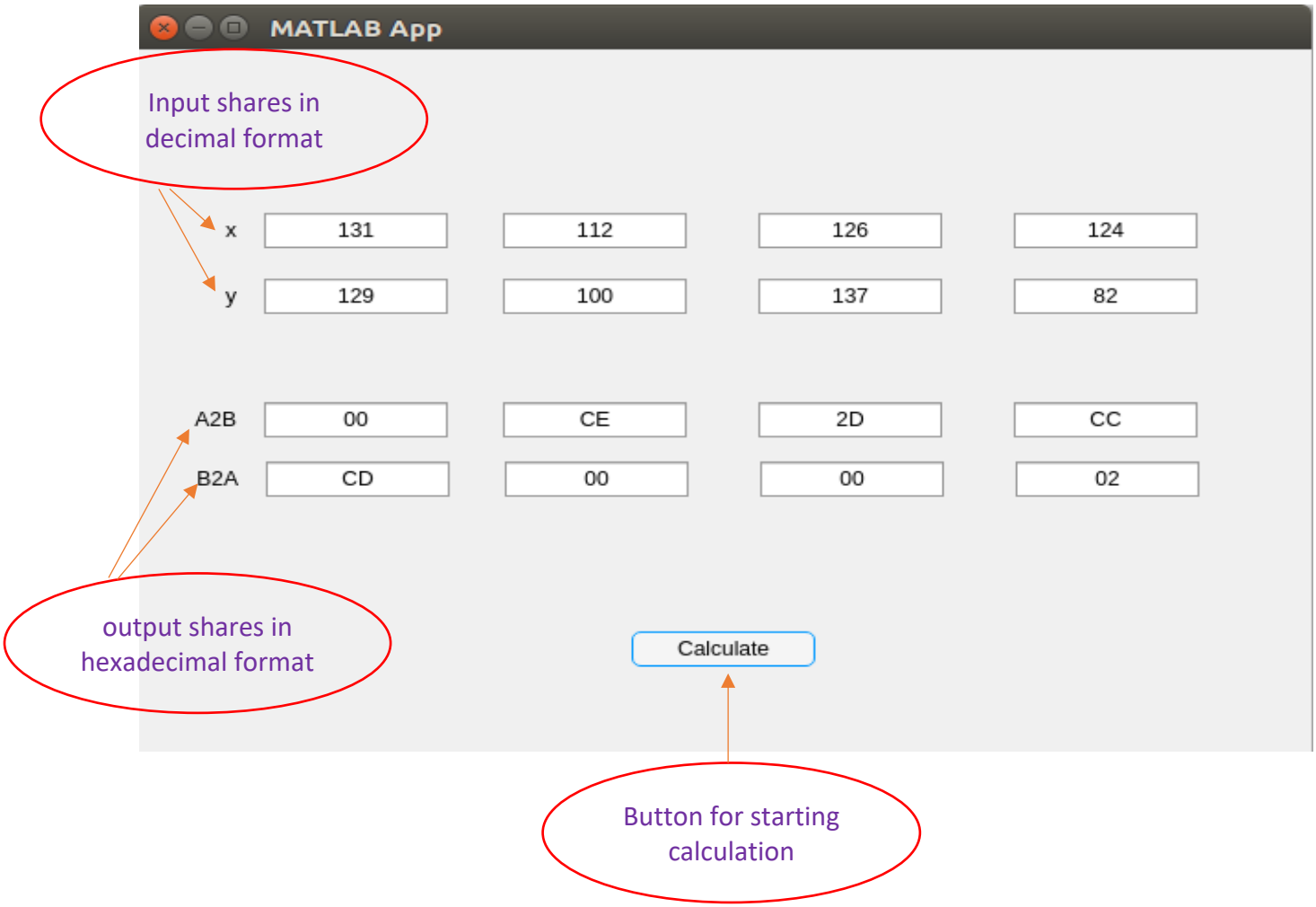
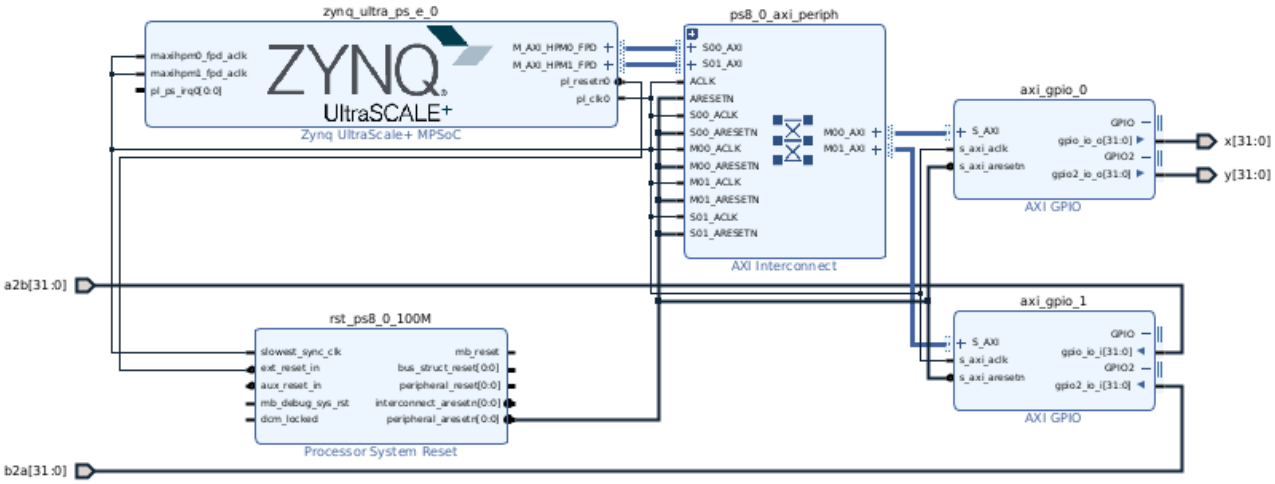
Block Diagrams

As all functions in this design are combinational circuits, the implementation of A2B and B2A on Xilinx Ultrascale+ ZCU104 has been described in this document.

In this implementation, shares of inputs (x(i), y(i), i = 0..3) are captured by a GUI in Matlab and passed to Cortext-A53 which is one of four ARM cores in Zynq FPGA through serial communication (UART). After processing on data, the input data send to GPIO (General Purpose I/O) for calculating secure add based Arithmetic to Boolean conversion and vice versa. the output of A2B and B2A are connected to another GPIO and collected data after processing on Cortext-A53 sends to the host machine and display in Matlab GUI. The following figures depict the Matlab GUI and blocks used in FPGA to create the platform.

Matlab codeand c and code for Cortext-A53 are available in 5_source_code/zynq




zynq_ultra_ps_e_0
maxihpm0_fpd_aclk
maxihpm1_fpd_aclk
pl_ps_irq[0:0]
M_AXI_HPM0_FPD
M_AXI_HPM1_FPD
pl_resetn0
pl_clk0
Zynq UltraScale+ MPSoC
psB_0_axi_periph
S00_AXI
S01_AXI
ACLK
ARESETN
S00_ACLK
S00_ARESETN
M00_ACLK
M00_ARESETN
M01_ACLK
M01_ARESETN
S01_ACLK
S01_ARESETN
M00_AXI
M01_AXI
AXI Interconnect
axi_gpio_0
S_AXI
s_axi_aclk
s_axi_aresetn
GPIO
gpio_io_o[31:0]
GPIO2
gpio2_io_o[31:0]
AXI GPIO
x[31:0]
y[31:0]
a2b[31:0]
rst_psB_0_100M
slowest_sync_clk
ext_reset_in
aux_reset_in
mb_debug_sys_rst
dcm_locked
mb_reset
bus_struct_reset[0:0]
peripheral_reset[0:0]
interconnect_aresetn[0:0]
peripheral_aresetn[0:0]
Processor System Reset
axi_gpio_1
gpio_io_i[31:0]
gpio2_io_i[31:0]
AXI GPIO
b2a[31:0]