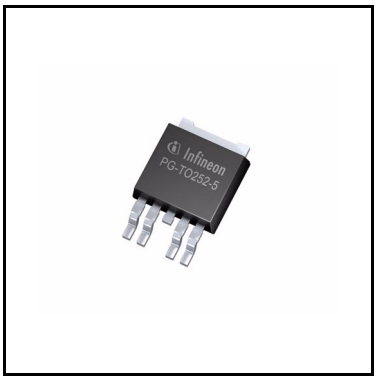
# BTS50025-1TEA

## Smart High-Side Power Switch

AEC Qualified RoHS




## 1 Overview

### Features

- One channel device
- Low Stand-by current
- Current controlled input
- Reverse battery protection
- Electrostatic discharge protection (ESD)
- Optimized Electromagnetic Compatibility (EMC)
- Compatible to cranking pulses (Severe cold start E11 in LV124)
- Embedded diagnostic functions
- Embedded protection functions
- Green Product (RoHS compliant)

### Applications

- Suitable for resistive, inductive and capacitive loads
- Replaces electromechanical relays, fuses and discrete circuits
- Most suitable for application with high current loads, such heating system, fan and pump
- PWM applications with low frequency

### Product validation

Qualified for automotive applications. Product validation according to AEC-Q100.

### Description

The BTS50025-1TEA is a 2.5mΩ single channel Smart High-Side Power Switch, embedded in a PG-TO-252-5-11 package, providing protective functions and diagnosis. It contains Infineon® ReverSave™ functionality. The power transistor is built by an N-channel MOSFET with charge pump. It is specially designed to drive high current loads up to 65A, for application like heaters, glow plugs, fan and pump in the harsh automotive environment.

## Overview

**Table 1 Product Summary**

| Parameter | Symbol | Values |
|---|---|---|
| Operating Voltage | $V_{S(OP)}$ | 5.8 V … 18 V |
| Extended supply voltage range | $V_{S(EXT)}$ | 3.1 V ...27 V |
| Maximum ON-State Resistance ($T_j$ = 150 °C) | $R_{DS(ON)}$ | 5 mΩ |
| Nominal Load Current ($T_A$ = 85°C) | $I_{L(NOM)}$ | 24 A |
| Typical current sense differential ratio | $dk_{ILIS}$ | 18000 |
| Minimum short circuit current threshold | $I_{CL(0)}$ | 65 A |
| Maximum reverse battery voltage | $-V_{S(REV)}$ | -16 V |
| Maximum Stand-by Current at $T_j$ = 25 °C | $I_{vs(off)}$ | 4 µA |

### Embedded Diagnostic Functions

- Proportional load current sense
- Short circuit / Overtemperature detection
- Latched status signal after short circuit or overtemperature detection

### Embedded Protection Functions

- Infineon® ReverSave™: Reverse battery protection by self turn ON of power MOSFET
- Short circuit protection with latch
- Overtemperature protection with latch
- Enhanced short circuit operation
- Infineon® SMART CLAMPING

| Type | Package | Marking |
|---|---|---|
| BTS50025-1TEA | PG-TO-252-5-11 | S50025A |

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# 2 Block Diagram

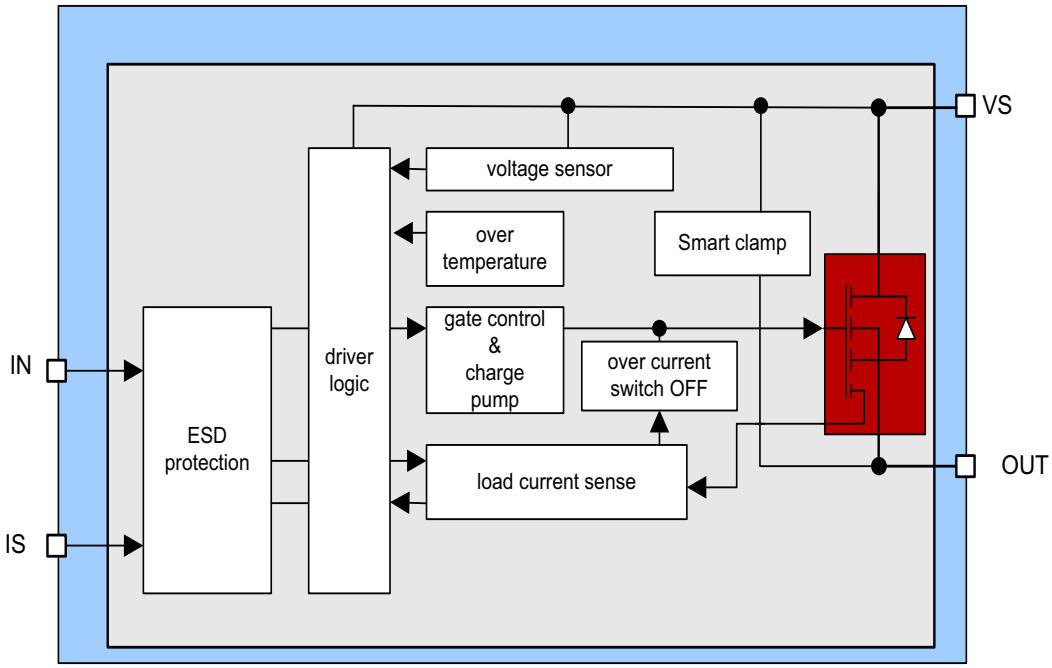



**Figure 2-1 Block Diagram for the BTS50025-1TEA**

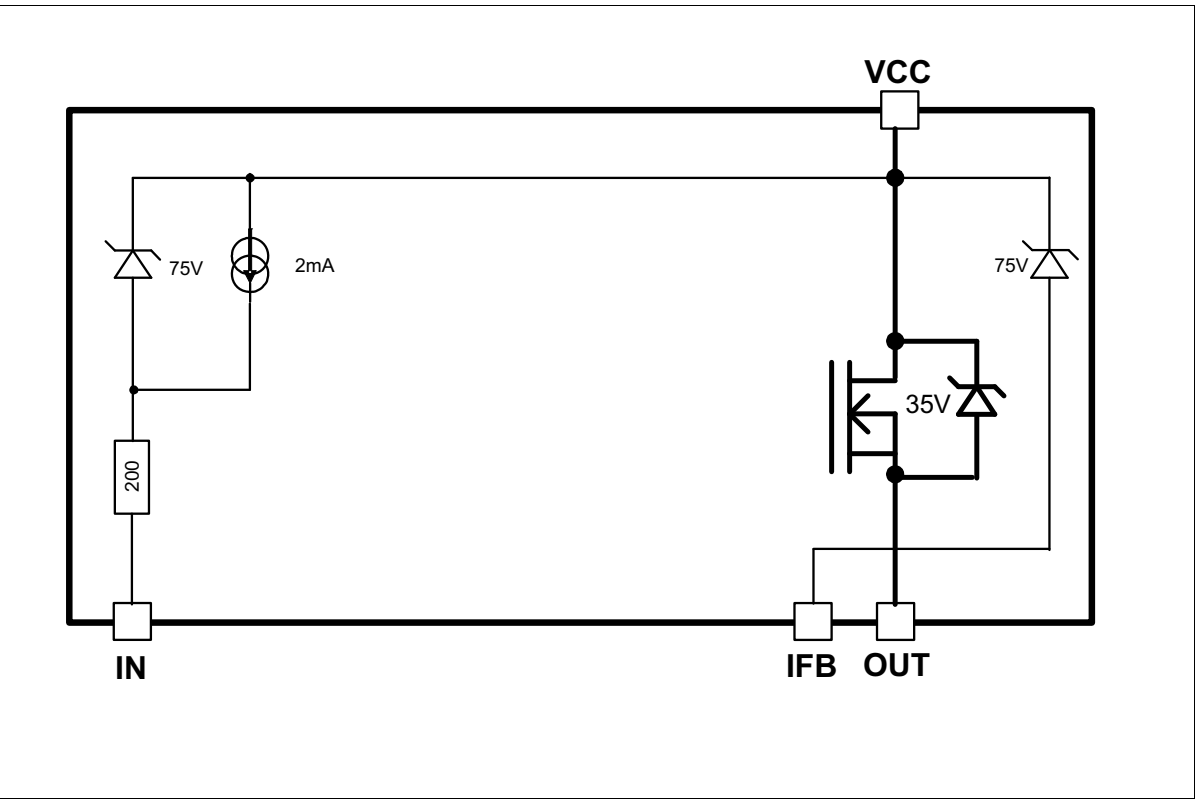



**Figure 2-2 Internal diode diagram**

# 3 Pin Configuration

## 3.1 Pin Assignment

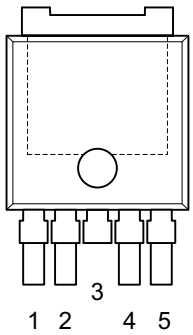



**Figure 3-1 Pin Configuration**

## 3.2 Pin Definitions and Functions

| Pin | Symbol | Function |
|---|---|---|
| 1 | OUT | OUTput; Protected high side power output channel[1)] |
| 2 | IN | **INput;** Digital signal to switch ON channel with Bipolar or Mosfet (active “low”) |
| 3, Cooling tab | VS | **Supply Voltage;** Battery voltage |
| 4 | IS | Sense; Analog/Digital signal for diagnosis, if not used: left open |
| 5 | OUT | OUTput; Protected high side power output channel[1)] |

1) All output pins are internally connected and they also have to be connected together on the PCB. Not shorting all outputs on PCB will considerably increase the ON-state resistance and decrease the current sense / overcurrent tripping accuracy. PCB traces have to be designed to withstand the maximum current.
Exact path resistance matching on both outputs to common point is needed also for short circuit robustness and reliability at high current.

## 3.3 Voltage and Current Definition

**Figure 3-2** shows all terms used in this data sheet, with associated convention for positive values.

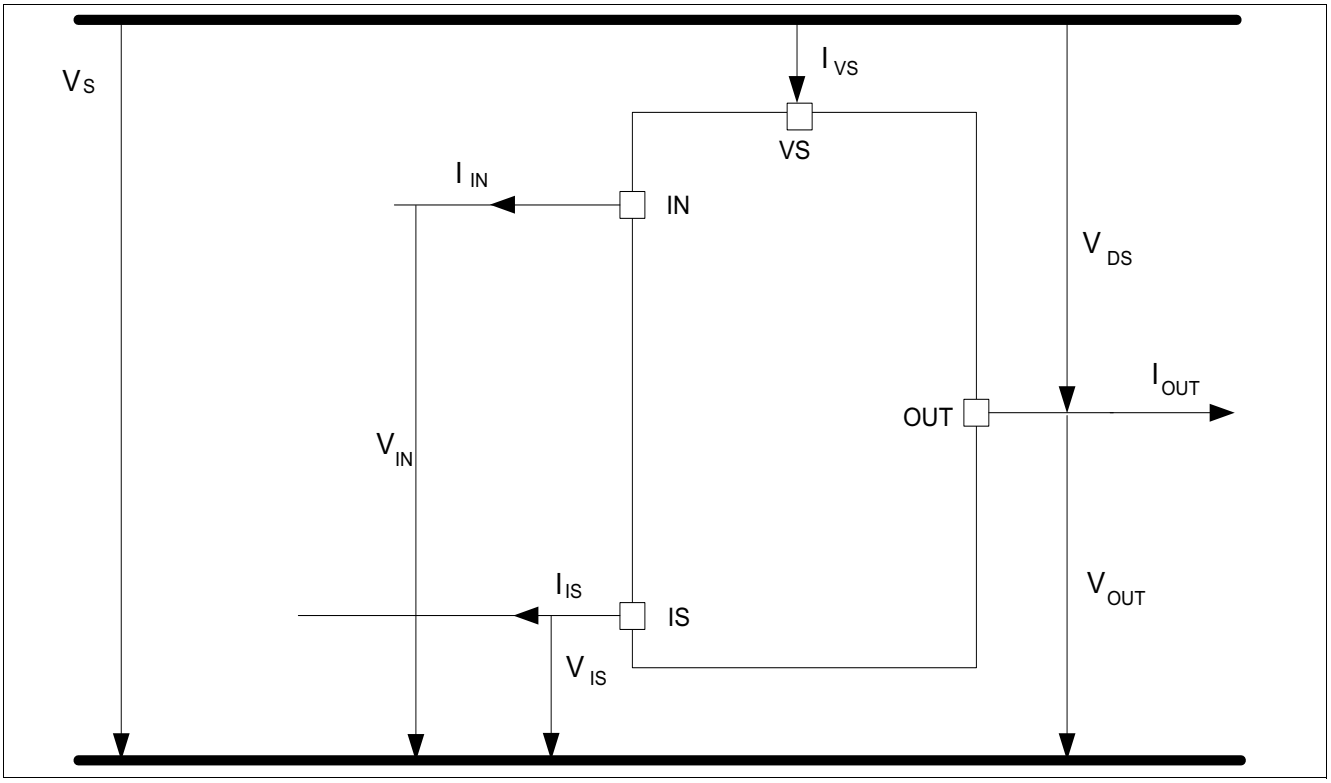



**Figure 3-2 Voltage and Current Definition**

# 4 General Product Characteristics

## 4.1 Absolute Maximum Ratings

**Table 2 Absolute Maximum Ratings[1)]**

$T_j$ = -40°C to +150°C; (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| **Supply Voltages** | | | | | | | |
| Supply Voltage | $V_S$ | -0.3 | – | 35 | V | – | P_4.1.1 |
| Reverse Polarity Voltage | $-V_{S(REV)}$ | 0 | – | 18 | V | [2)]$V_{in}$=0 V<br>$T_A$ = 25°C<br>$R_L$ ≥ 0.68 Ω<br>t < 5 min. | P_4.1.2 |
| Load Dump Voltage | $V_{S(LD)}$ | – | – | 45 | V | Suppressed Load Dump acc. to ISO16750-2<br>$R_I$ = 2 Ω<br>td=200ms<br>Us=100V<br>$R_L$ = 0.68 Ω<br>$R_{IS}$ = 1 kΩ<br>$V_{S(LD)} = U_S$* | P_4.1.3 |
| **Short Circuit Capability** | | | | | | | |
| Supply Voltage for Short Circuit Protection | $V_{S(SC)}$ | 3.1 | – | 27 | V | In accordance to AEC Q100-012, Figure-1 Test Circuit. | P_4.1.4 |
| **Input Pin** | | | | | | | |
| Voltage at IN pin | $V_s$ - $V_{in}$ | -16 | – | 75 | V | – | P_4.1.6 |
| Current through IN pin | $I_{IN}$ | -50 | – | 50 | mA | – | P_4.1.20 |
| Maximum Input Frequency | $F_{in}$ | – | – | 200 | Hz | 5.8V<$V_S$ - $V_{IN}$<27V | P_4.1.7 |
| Maximum Retry Cycle Rate in Fault Condition | $F_{fault}$ | – | – | 200 | Hz | – | P_4.1.8 |

**Table 2 Absolute Maximum Ratings[1)]** (cont'd)

$T_j$ = -40°C to +150°C; (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| **Sense Pin** | | | | | | | |
| Voltage at IS pin | $V_S$ - $V_{is}$ | -0.3 | – | 75 | V | – | P_4.1.9 |
| Current through IS Pin | $I_{IS}$ | -50 | – | 50 | mA | – | P_4.1.10 |
| **Power Stage** | | | | | | | |
| Maximum Energy Dissipation by Switching Off Inductive Load Single Pulse over Lifetime | $E_{AS}$ | – | – | 600 | mJ | $V_S$ = 13.5 V<br>$I_L$ = 19 A<br>$T_{J(0)} \leq$ 150°C<br>See **Figure 1** | P_4.1.11 |
| Maximum Energy Dissipation Repetitive Pulse | $E_{AR}$ | – | – | 130 | mJ | [3)] $V_S$ = 13.5 V<br>$I_L$ = 19A<br>$T_{J(0)} \leq$ 105°C<br>See **Figure 1** | P_4.1.12 |
| Maximum Energy Dissipation Repetitive Pulse | $E_{AR}$ | – | – | 80 | mJ | [3)] $V_S$ = 13.5 V<br>$I_L$ =40 A<br>$T_{J(0)} \leq$ 105°C<br>See **Figure 1** | P_4.1.13 |
| Voltage at OUT Pin | $V_S$ - $V_{OUT}$ | -0.3 | – | 35 | V | – | P_4.1.14 |
| **Temperatures** | | | | | | | |
| Junction Temperature | $T_J$ | -40 | – | 150 | °C | – | P_4.1.15 |
| Dynamic Temperature Increase while Switching | $\Delta T_J$ | – | – | 60 | K | – | P_4.1.16 |
| Storage Temperature | $T_{STG}$ | -55 | – | 150 | °C | – | P_4.1.17 |
| **ESD Susceptibility** | | | | | | | |
| ESD Susceptibility (all Pins) | $V_{ESD(HBM)}$ | -2 | – | 2 | kV | HBM[4)] | P_4.1.18 |
| ESD Susceptibility OUT Pin vs. $V_S$ | $V_{ESD(HBM)}$ | -4 | – | 4 | kV | HBM[4)] | P_4.1.19 |
| ESD Susceptibility (all Pins) | $V_{ESD(CDM)}$ | -500 | – | 500 | V | CDM[5)] | P_4.1.21 |
| ESD Susceptibility (corner Pins) | $V_{ESD(CD}$ | -750 | – | 750 | V | CDM[5)] | P_4.1.22 |

1) Not subject to production test, specified by design.
2) The device is mounted on a FR4 2s2p board according to Jedec JESD51-2,-5,-7 at natural convection.
3) Setup with repetitive EAR and superimposed TC conditions (like AEC-Q100-PTC, ≤ $10^6$ pulses with E ≤ $E_{AR}$, ≤$10^3$ passive temperature cycles), parameter drift within datasheet limits possible
4) ESD susceptibility, Human Body Model "HBM" according to AEC Q100-002.
5) ESD susceptibility, Charged Device Model "CDM" according to AEC Q100-011.

**Notes**

1. *Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*
2. *Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.*

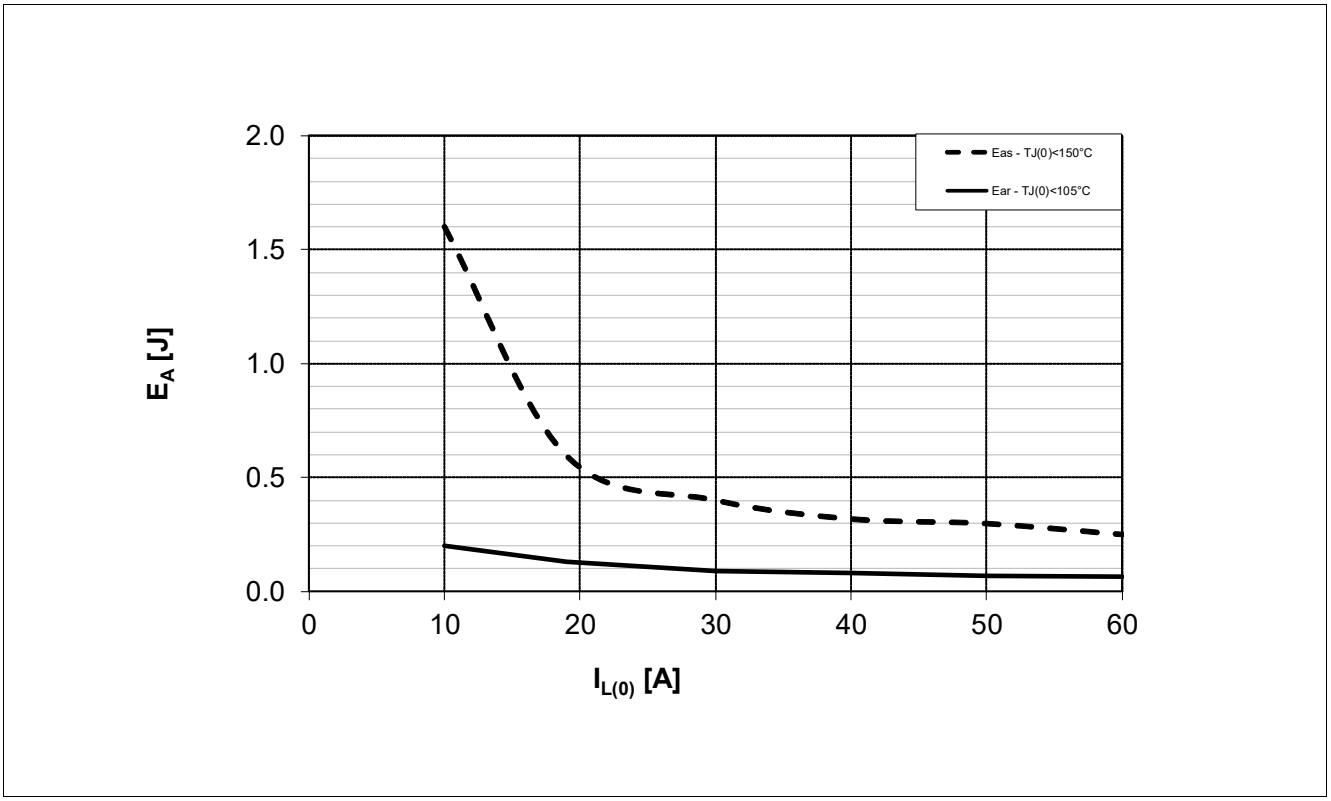



**Figure 1 Maximum Energy Dissipation for Inductive Switch OFF, $E_{AS/AR}$ vs. $I_L$ at $V_S$ = 13.5 V**

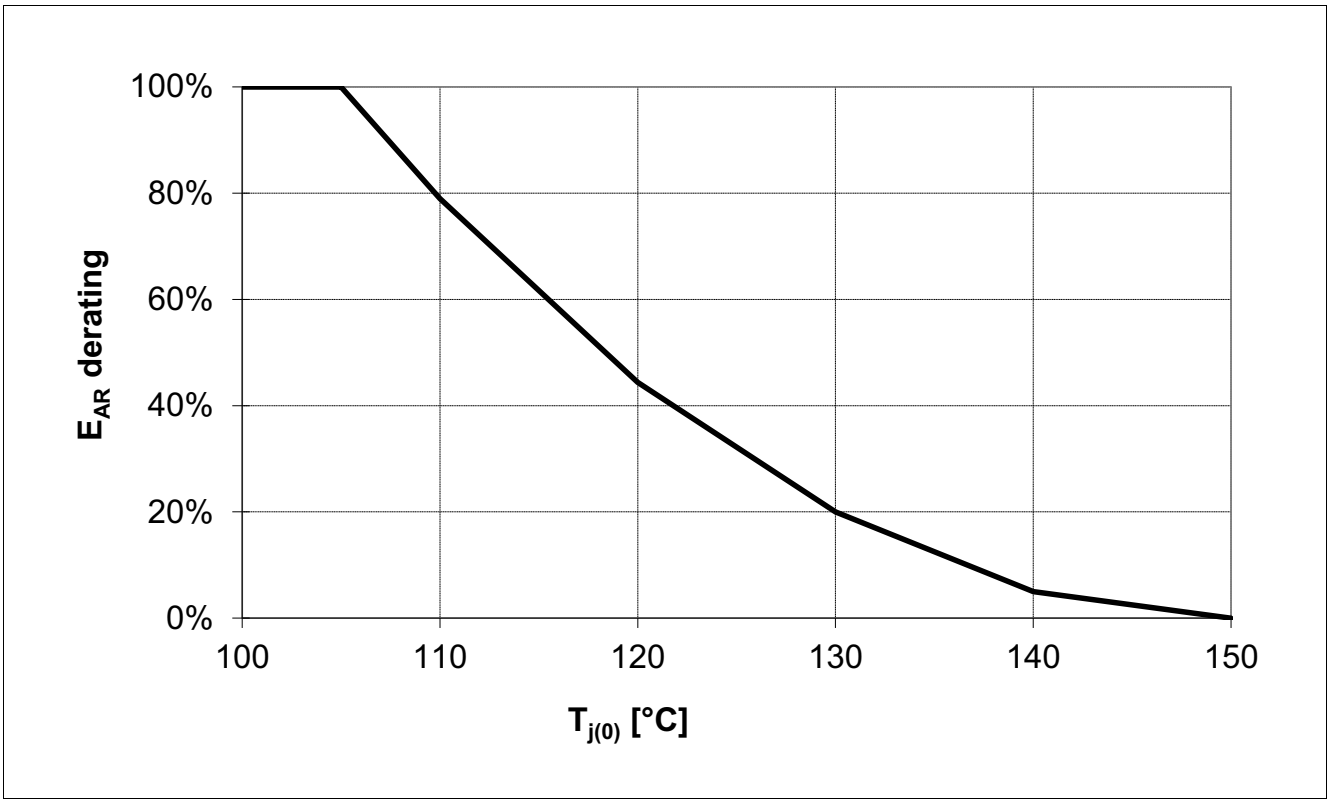



**Figure 2 Maximum Energy Dissipation Repetitive Pulse temperature derating**

## 4.2 Functional Range

**Table 3 Functional Range**

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| Supply Voltage Range for Nominal Operation | $V_{S(NOM)}$ | 5.8 | – | 18 | V | – | P_4.2.1 |
| Supply Voltage Range for Extended Operation | $V_{S(EXT)}$ | 3.1 | – | 27 | V | 1) Parameter deviation possible | P_4.2.2 |

1) Protection functions still operative

*Note: Within the functional or operating range, the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the Electrical Characteristics table.*

## 4.3 Thermal Resistance

*Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to **www.jedec.org**.*

**Table 4 Thermal Resistance**

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| Junction to Case | $R_{thJC}$ | – | – | 0.8 | K/W | 1) | P_4.3.1 |
| Junction to Ambient | $R_{thJA(2s2p)}$ | – | 22 | – | K/W | 1)2) | P_4.3.2 |
| Junction to Ambient | $R_{thJA(1s0p/600\ mm^2)}$ | – | 35 | – | K/W | 1)3) | P_4.3.3 |

1) Not subject to production test, specified by design.

2) Specified $R_{thJA}$ value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board; The Product (Chip+Package) was simulated on a 76.2 × 114.3 × 1.5 mm board with 2 inner copper layers (2 × 70 µm Cu, 2 × 35 µm Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer. $T_A$ = 25°C. Device is dissipating 2 W power.

3) Specified $R_{thJA}$ value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 1s0p board; the Product (Chip+Package) was simulated on a 76.2 × 114.3 × 1.5 mm board with only one top copper layer 1 × 70 µm. $T_A$ = 25°C. Device is dissipating 2 W power.

**Figure 3** is showing the typical thermal impedance of BTS50025-1TEA mounted according to JEDEC JESD51-2,-5,-7 at natural convection on FR4 1s0p and 2s2p boards.

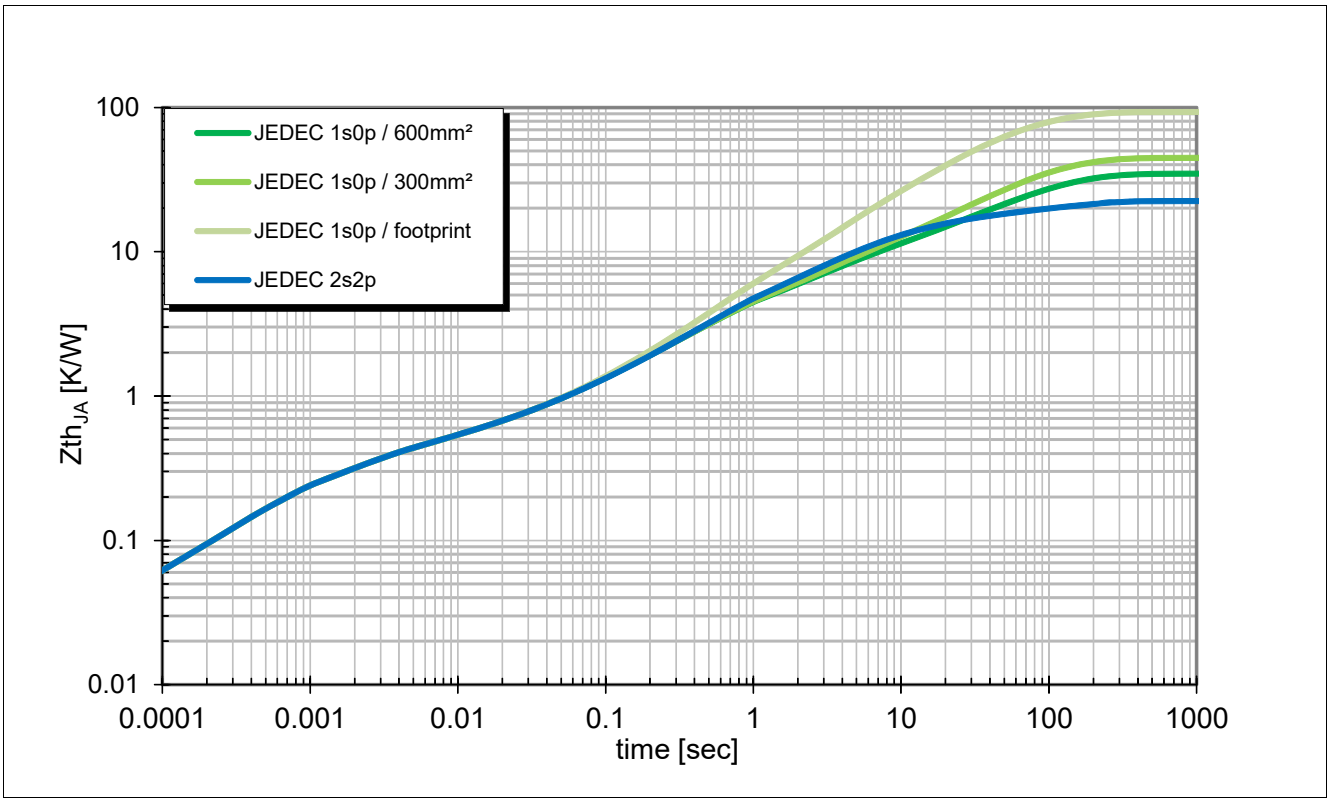



**Figure 3 Typical Transient Thermal Impedance $Z_{th(JA)}$ = f(time) for Different PCB Conditions**

# 5 Functional Description

## 5.1 Power Stage

The power stage is built by a N-channel power MOSFET (DMOS) with a charge pump.

### 5.1.1 Output ON-State Resistance

The ON-state resistance $R_{DS(ON)}$ depends on the supply voltage as well as the junction temperature $T_J$. **Page 35** shows the dependencies in terms of temperature and supply voltage, for the typical ON-state resistance. The behavior in reverse polarity is described in **Chapter 5.2.1**.

A LOW signal (see **Chapter 5.1.2**) at the input pin causes the power DMOS to switch ON with a dedicated slope, which is optimized in terms of EMC emission.

### 5.1.2 Switching Resistive Loads

**Figure 5-1** shows the typical timing when switching a resistive load. The power stage has a defined switching behavior. Defined slew rates results in lowest EMC emission at minimum switching losses.

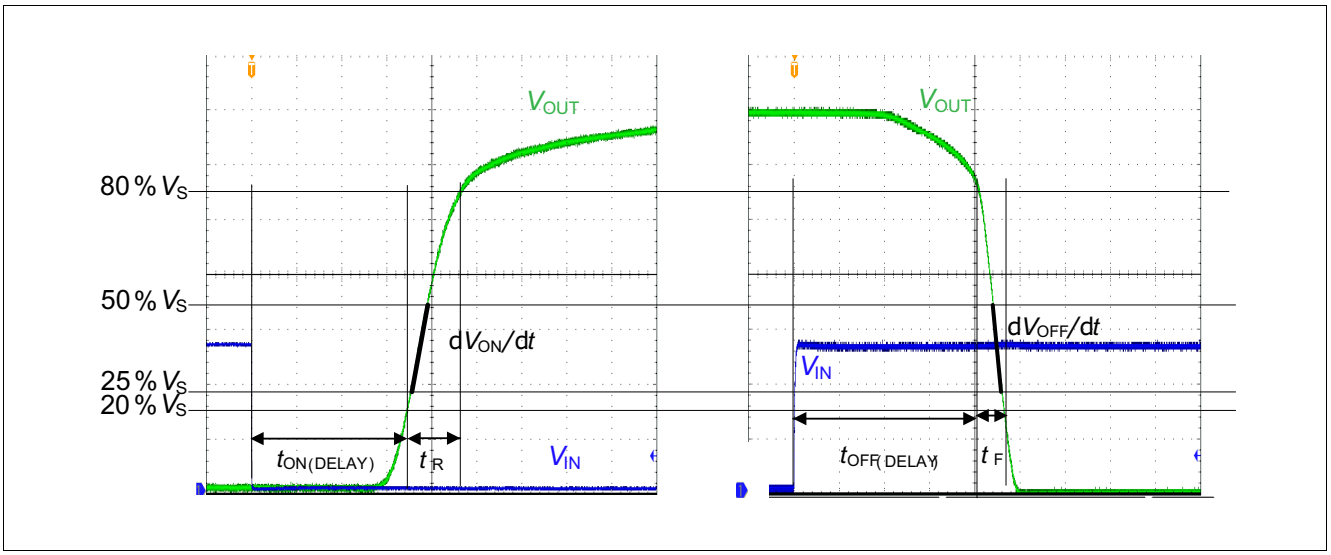



**Figure 5-1 Switching a Resistive Load: Timing**

### 5.1.3 Switching Inductive Loads

#### 5.1.3.1 Output Clamping

When switching OFF inductive loads with high side switches, the voltage $V_{OUT}$ drops below ground potential, because the inductance intends to continue driving the current. To prevent the destruction of the device due to high voltages, there is a Infineon® SMART CLAMPING mechanism implemented that keeps negative output voltage to a certain level ($V_S$ - $V_{DS(CL)}$). Please refer to **Figure 5-2** and **Figure 5-3** for details. Nevertheless, the maximum allowed load inductance remains limited.

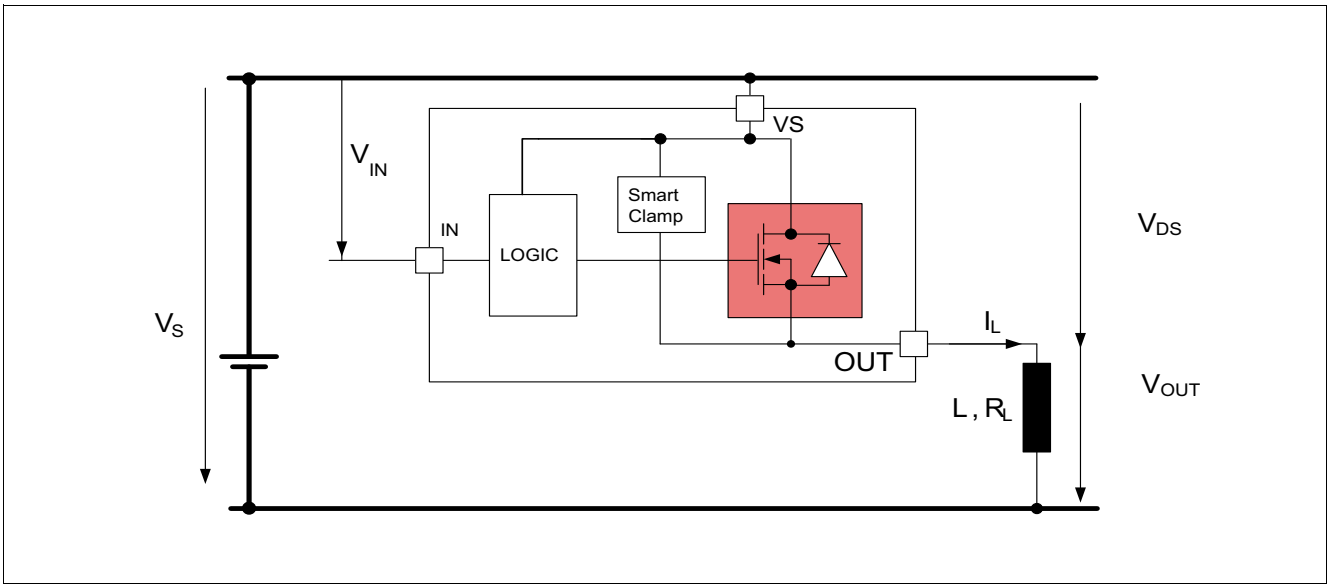



**Figure 5-2 Output Clamp**

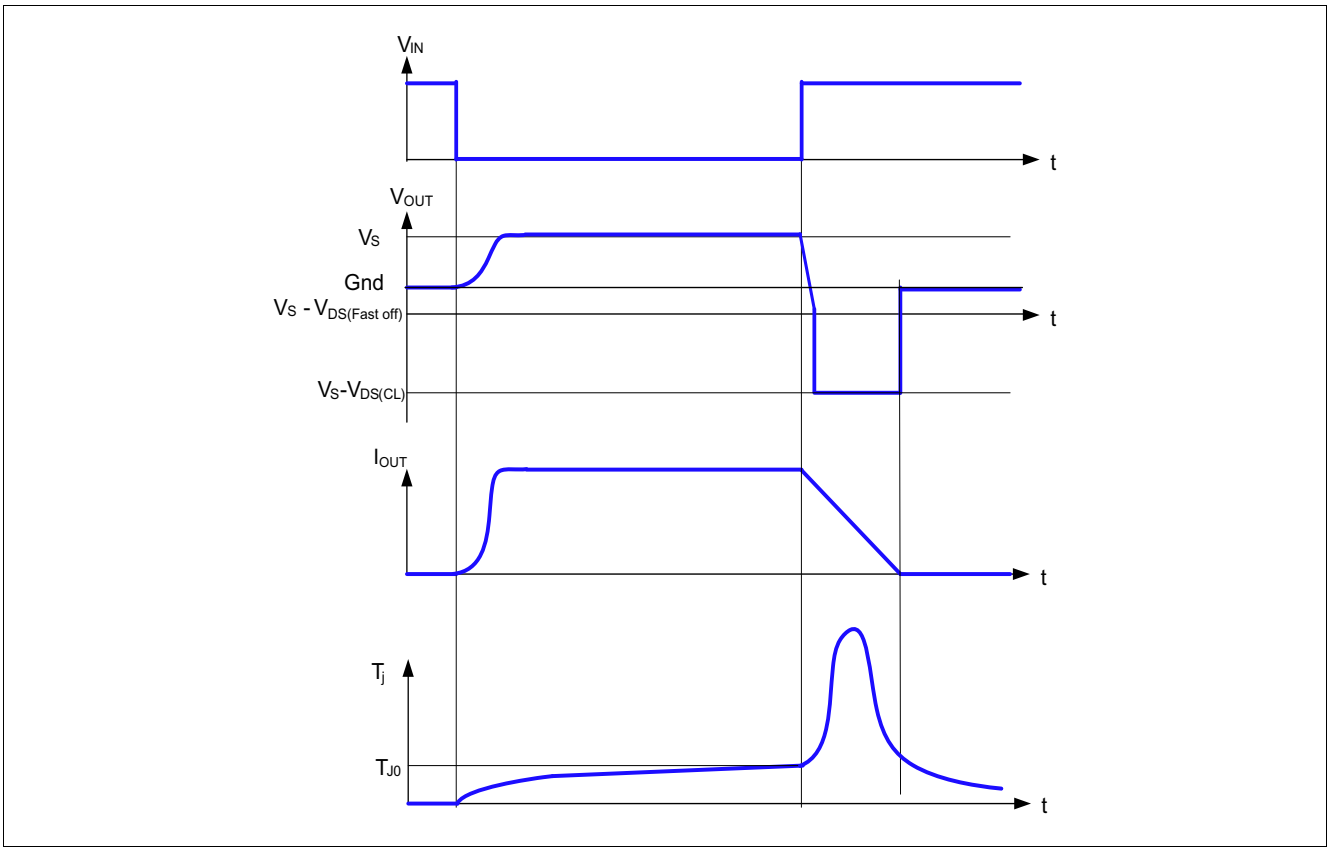



**Figure 5-3 Switching an Inductance**

The BTS50025-1TEA provides Infineon® SMART CLAMPING functionality. To increase the energy capability, the clamp voltage $V_{DS(CL)}$ increases with junction temperature $T_J$ and with load current $I_L$. Refer to **Page 37**.

### 5.1.3.2 Maximum Load Inductance

During demagnetization of inductive loads, energy must be dissipated in the BTS50025-1TEA. This energy can be calculated with following equation:

$$E = V_{DS(CL)} \times \frac{L}{R_L} \times \left[ \frac{V_S - V_{DS(CL)}}{R_L} \times \ln\left(1 - \frac{R_L \times I_L}{V_S - V_{DS(CL)}}\right) + I_L \right] \tag{5.1}$$

Following equation simplifies under the assumption of $R_L = 0\ \Omega$.

$$E = \frac{1}{2} \times L \times I_L^2 \times \left(1 - \frac{V_S}{V_S - V_{DS(CL)}}\right) \tag{5.2}$$

The energy, which is converted into heat, is limited by the thermal design of the component. See **Figure 1** for the maximum allowed energy dissipation as function of the load current.

### 5.1.4 PWM Switching

The switching losses during this operation should be properly considered (see following equation):

$P_{TOTAL}$ = (switching_ON_energy + switching_OFF_energy + $I_L^2 \times R_{DS(ON)} \times t_{DC}$) / period

In the event of a fault condition it has to be ensured, that the PWM frequency will not exceed a maximum retry frequency of $f_{FAULT}$ (parameter P_4.1.9). With this measure the short circuit robustness $n_{RSC1}$ (parameter P_4.1.4) can be utilized. Operation at nominal PWM frequency can only be restored, once the fault condition is overcome.

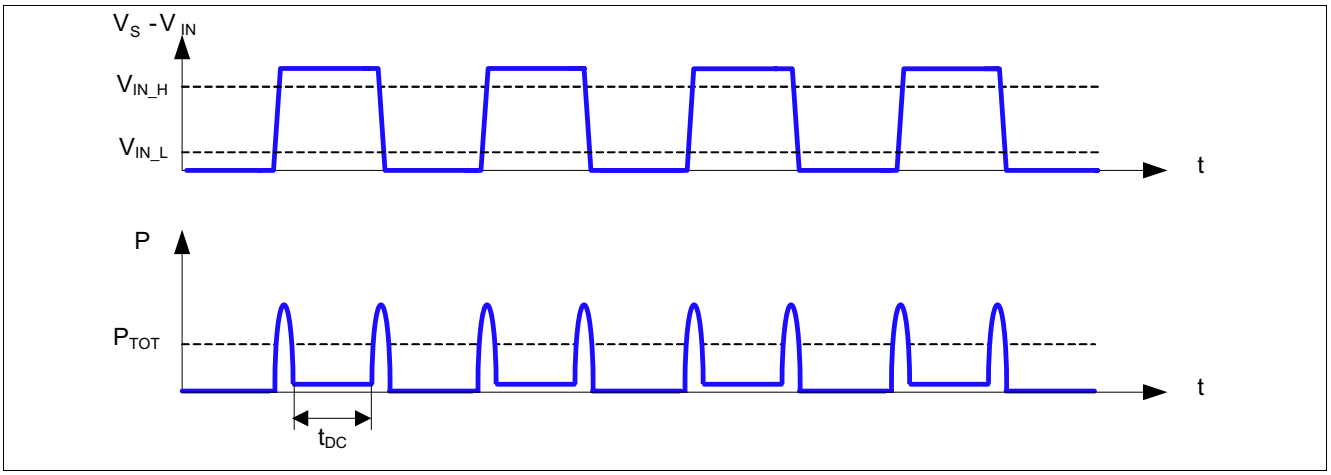



**Figure 5-4 Switching in PWM**

### 5.1.5 Advanced switch-off behavior

In order to reduce device stress when switching OFF Inductive and critical loads, the device provides an advanced switch off functionality which results in a faster switch off behavior. This fast switch off functionality is triggered by one the following conditions:

- The device is commanded off by applying $V_{IN(L)}$ at the IN pin. During the switch OFF operation the OUT pins' voltage in respect to VS pin drops below $V_{ds(fast\ off)}$. See **Figure 5-3**.
- The device is commanded on or is already in on-state. The device then detects a short circuit condition ($I_L \geq I_{CL(0)}$) and initiates a protective switch off. Please refer to **Chapter 5.3.1.1** and **Chapter 5.3.1.2** for details.
- The device is commanded on or is already in on-state. The device then detects an over-temperature condition.

## 5.2 Input Pins

### 5.2.1 Input Circuitry

The input circuitry is referenced to VS. To turn on the device $V_S$ - $V_{IN}$ must be higher than $V_{IN(H)}$ and lower than $V_{IN(L)}$ to turn off the device. The most common way is to use a bipolar transistor to connect the input pin to the ground. When the device is latched in protection mode $V_S$ - $V_{IN}$ must be lower than $V_{IN(L)}$ and $I_{in}$ lower than $I_{IN(L)}$ in order to reset the latch. The device provides Infineon® ReverSave™ functionality which turns on the power mosfet in reverse polarity. This functionality required to have a diode in parallel of the bipolar transistor. **Figure 5-5** shows the electrical equivalent input circuitry.

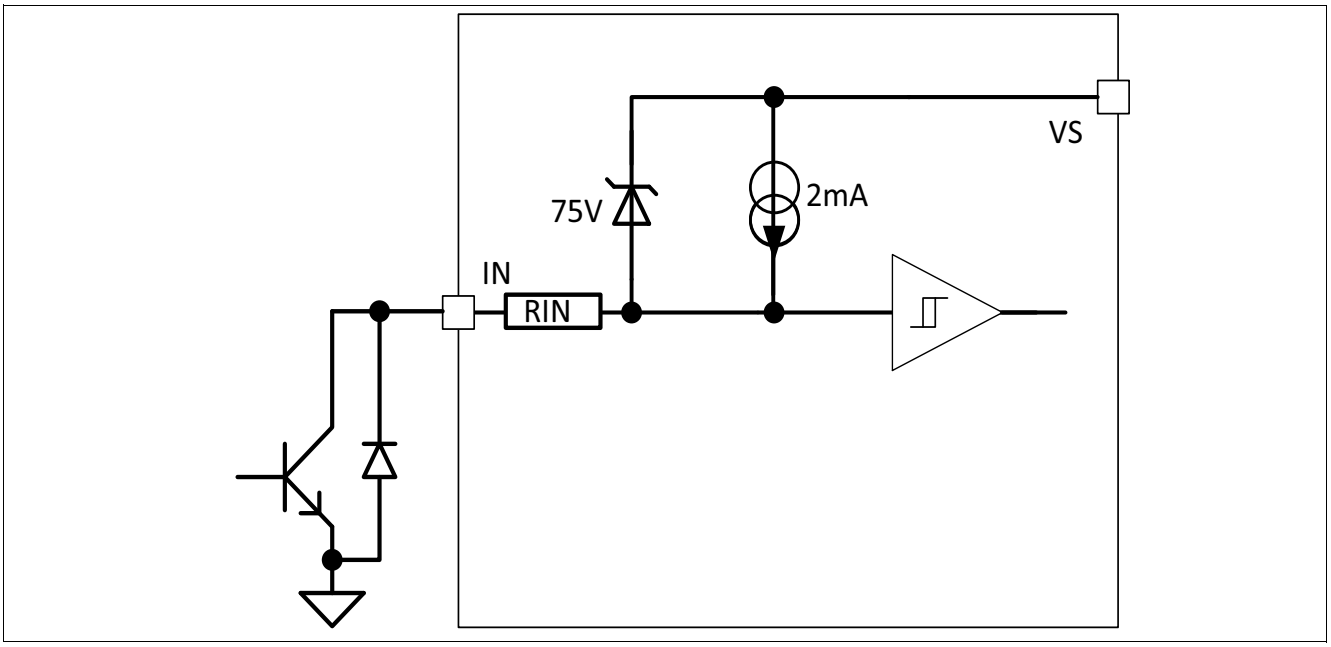



**Figure 5-5 Input Pin Circuitry**

## 5.3 Protection Functions

The device provides embedded protective functions. Integrated protection functions are designed to prevent the destruction of the IC from fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are designed neither for continuous nor for repetitive operation.

**Figure 5-6** describes the typical functionality of the diagnosis and protection block.

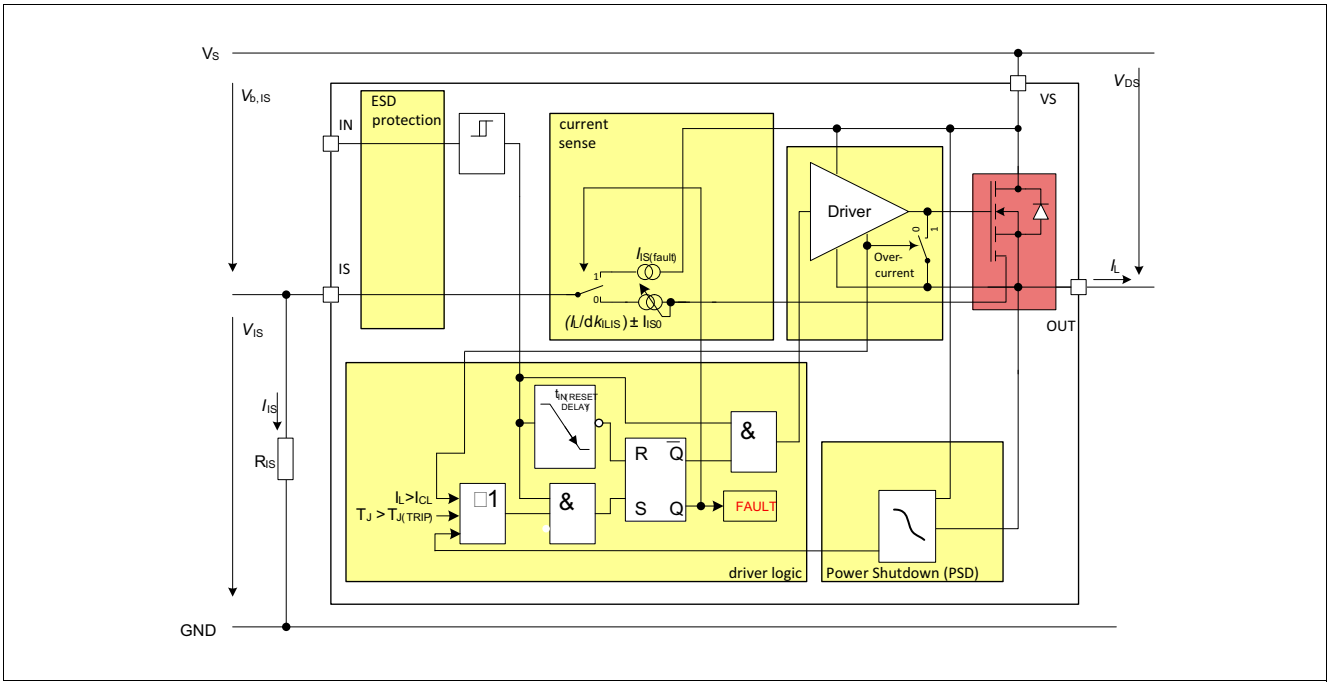



**Figure 5-6 Diagram of Diagnosis & Protection Block**

### 5.3.1 Overload Protection

In case of overload, high inrush current or short circuit to ground, the BTS50025-1TEA offers several protection mechanisms. Any protective switch OFF latches the output. To restart the device, it is necessary to set $V_s$ - $V_{in}$ < $V_{in(l)}$ and $I_{in}$ lower than $I_{IN(L)}$ for $t > t_{IN(RESETDELAY)}$. This is a latch behavior. **Figure 5-9** gives a sketch of the situation.

#### 5.3.1.1 Activation of the Switch into Short Circuit (Short Circuit Type 1)

When the switch is activated into short circuit, the current will raise. When the output current reaches $I_{CL(0)}$ value, the device is latched and will turn off after $t_{OFF(TRIP)}$ regardless the output current value. For overload (short circuit or overtemperature), the maximum retry cycle ($f_{fault}$) under fault condition must be considered.

#### 5.3.1.2 Short Circuit Appearance when the Device is already ON (Short Circuit Type 2)

When the device is in ON state and a short circuit to ground appears at the output (SC2) with an overcurrent higher than $I_{CL(0)}$, the device automatically turns OFF and latches the device.

#### 5.3.1.3 Over-power shutdown (PSD)

The BTS50025-1TEA integrates an over-power shutdown protection in order to limit the power dissipation. This protection intends to limit the maximum junction temperaturee in case of soft short circuit(IL < $I_{CL(0)}$), repetitive short circuit or short circuit at low voltage.

In case of a short circuit at low voltage with high resistor or inductor in the battery line, Vs can drop below $V_{VS-VIN(PSD)}$ and the load current will not reach the $I_{CL(0)}$ . In such condition the over-power shutdown protection will be activated and will latch the device after $t_{PSD(UV)}$ .

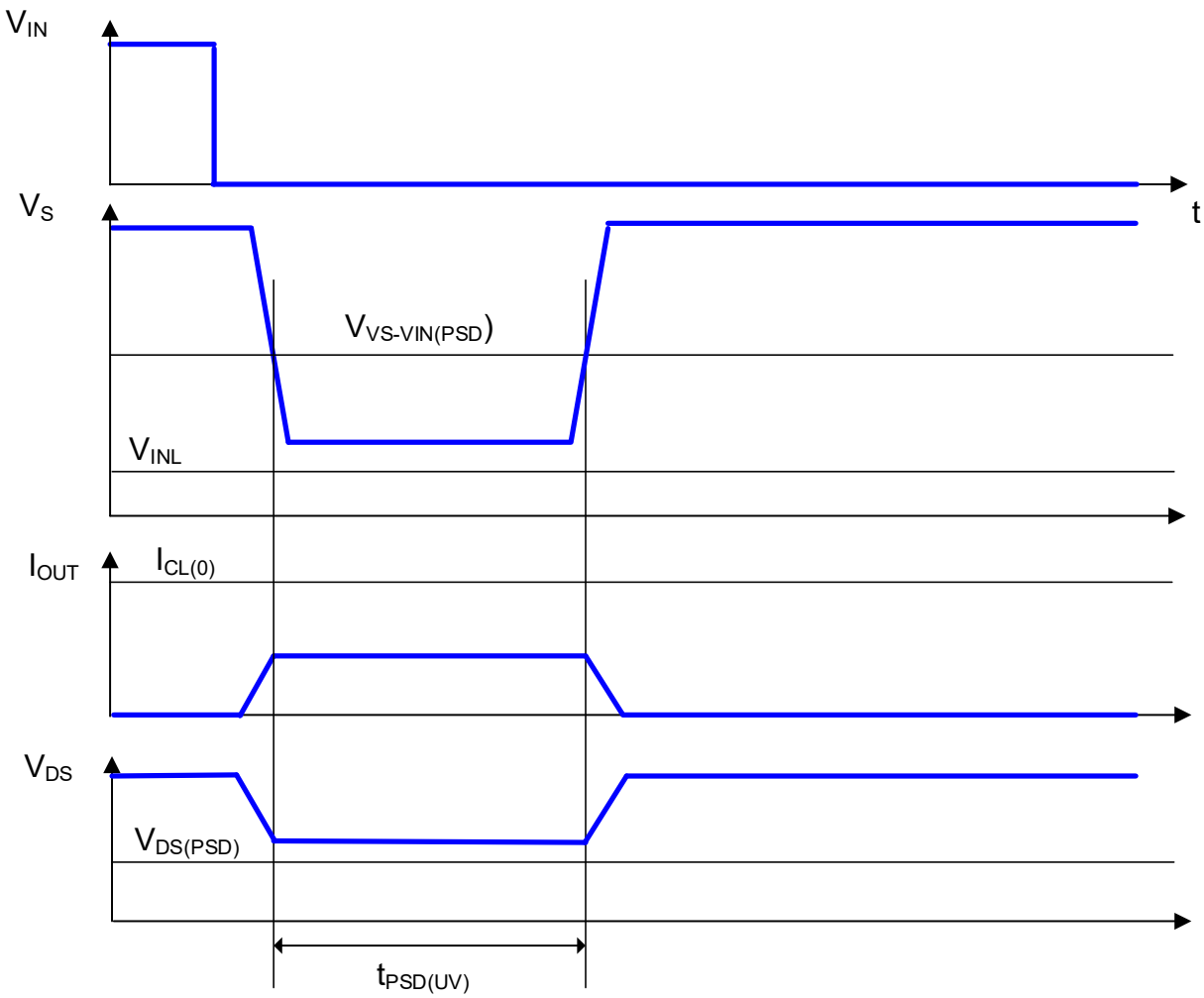



**Figure 5-7 Over Power Shutdown behavior at low voltage**

It also limits the maximum PWM frequency below $F_{IN}$. See **Figure 5-8**

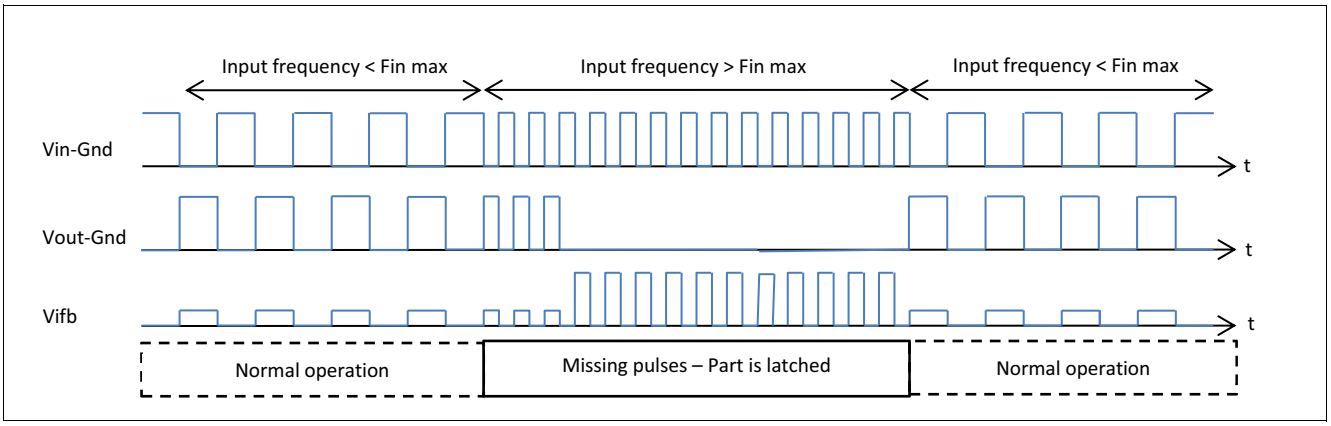



**Figure 5-8 Behavior of the BTS50025-1TEA during PWM operation above $F_{IN}$ max**

## 5.3.2 Temperature Limitation in the Power DMOS

The BTS50025-1TEA incorporates a temperature sensor. Triggering the over-temperature ($T_{J(TRIP)}$) will switch OFF the Power Mosfet to prevent destruction and latches the device.

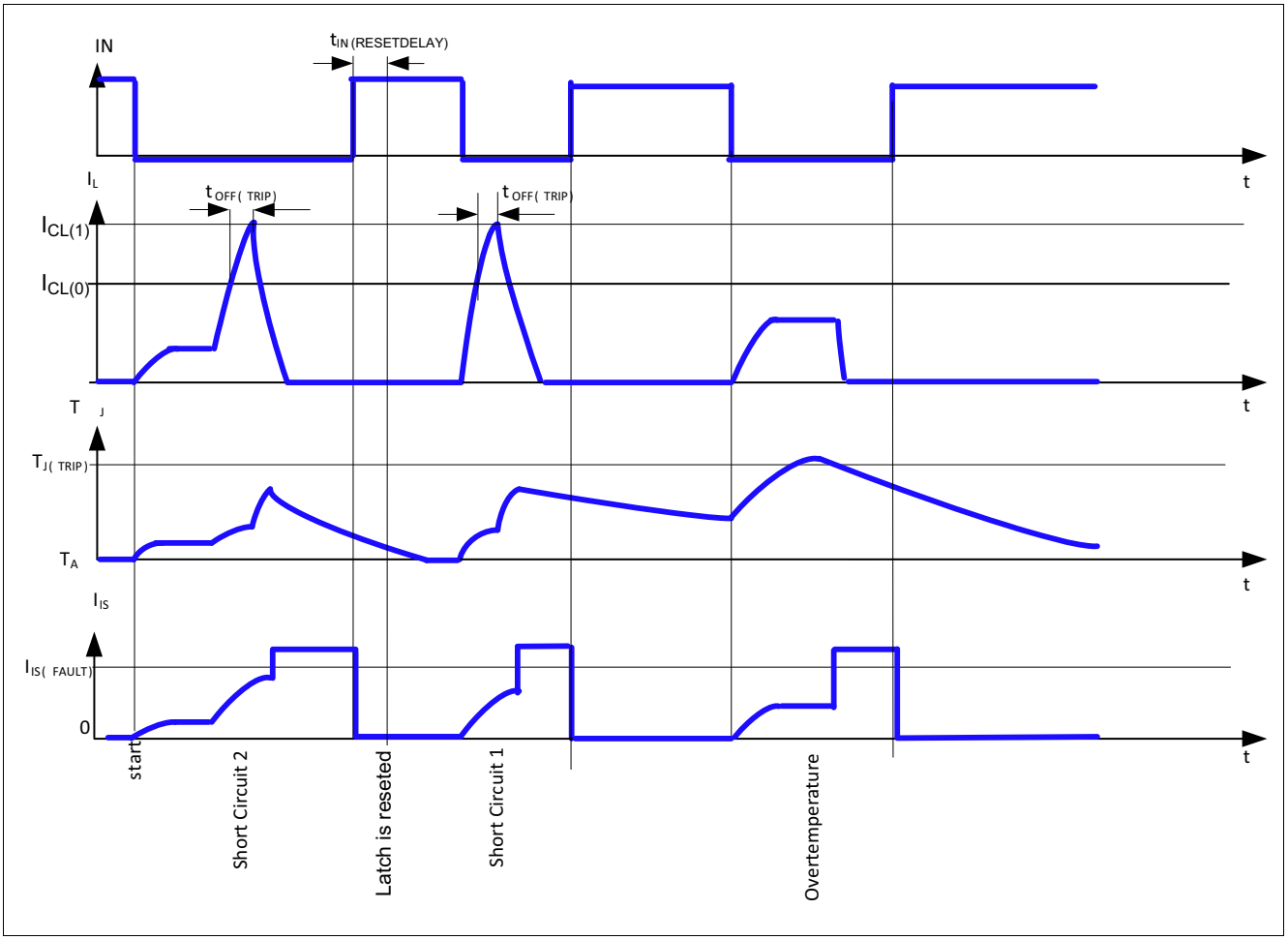



**Figure 5-9 Overload Protection**

The current sense exact signal timing can be found in the **Chapter 5.4.3.2**. It is represented here only for device's behavior understanding.

## 5.4 Diagnostic Functions

For diagnosis purposes, the BTS50025-1TEA provides a combination of digital and analog signal at pin IS.

### 5.4.1 IS Pin

The BTS50025-1TEA provides an enhanced current sense signal called $I_{IS}$ at pin IS. As long as no "hard" failure mode occurs (short circuit to GND / overcurrent / overtemperature) and the condition $V_{IS} \leq V_{OUT}$ - 3.5 V is fulfilled, a proportional signal to the load current is provided. The complete IS pin and diagnostic mechanism is described in **Figure 5-10**. The accuracy of the sense current depends on temperature and load current. In case of failure, a fixed $I_{IS(FAULT)}$ is provided. In order to get the fault current in the specified range, the condition $V_S$ - $V_{IS} \geq 3.5$ V must be fulfilled.

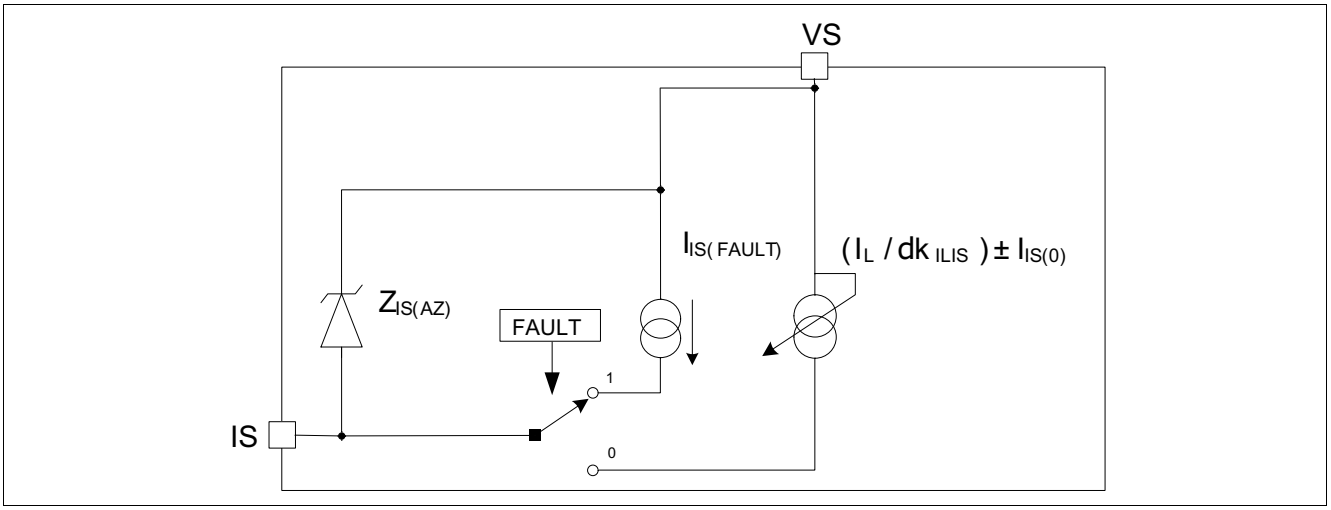



**Figure 5-10 Diagnostic Block Diagram**

## 5.4.2 SENSE Signal in Different Operation Modes

**Table 5-1 Sense Signal, Function of Operation Mode[1)]**

| Operation mode | Input Level | Output Level $V_{OUT}$ | Diagnostic Output (IS)[2)] |
|---|---|---|---|
| Normal operation | HIGH (OFF) | GND | $I_{IS(OFF)}$ |
| Short circuit to GND | | GND | $I_{IS(OFF)}$ |
| Overtemperature | | GND | $I_{IS(OFF)}$ |
| Short circuit to VS | | $V_S$ | $I_{IS(OFF)}$ |
| Open Load | | Z | $I_{IS(OFF)}$ |
| Normal operation | LOW (ON) | ~ $V_S$ | $I_{IS} = (I_L / dk_{ILIS}) \pm I_{IS0}$ |
| Short circuit to GND | | GND | $I_{IS(FAULT)}$ |
| Overtemperature (after the event) | | GND | $I_{IS(FAULT)}$ |
| Short circuit to VS | | $V_S$ | $I_{IS} < I_L / dk_{ILIS} \pm I_{IS0}$ |
| Open Load | | $V_S$ | $I_{IS0}$ |

1) Z = High Impedance
2) See **Chapter 5.4.3** for Current Sense Range and Improved Current Sense Accuracy.

## 5.4.3 SENSE Signal in the Nominal Current Range

**Figure 5-11** and **Figure 5-13** show the current sense as function of the load current in the power DMOS. Usually, a pull-down resistor $R_{IS}$ is connected to the current sense pin IS. A typical value is 1 kΩ. The dotted curve represents the typical sense current, assuming a typical $dk_{ILIS}$ factor value. The range between the two solid curves shows the sense accuracy range that the device is able to provide, at a defined current.

$$I_{IS} = \frac{I_L}{dk_{ILIS}} + I_{IS0} \text{ with } (I_{IS} \geq 0) \tag{5.3}$$

where the definition of $dk_{ILIS}$ is:

$$dk_{ILIS} = \frac{I_{L3} - I_{L1}}{I_{IS3} - I_{IS1}} \tag{5.4}$$

the definition of $I_{IS0}$ is:

$$I_{IS0} = I_{IS1} - \frac{I_{L1}}{dk_{ILIS}} \tag{5.5}$$

and the definition of $I_{L0}$ is:

$$I_{IL0} = I_{IL1} - I_{S1} \times dk_{ILIS} \tag{5.6}$$

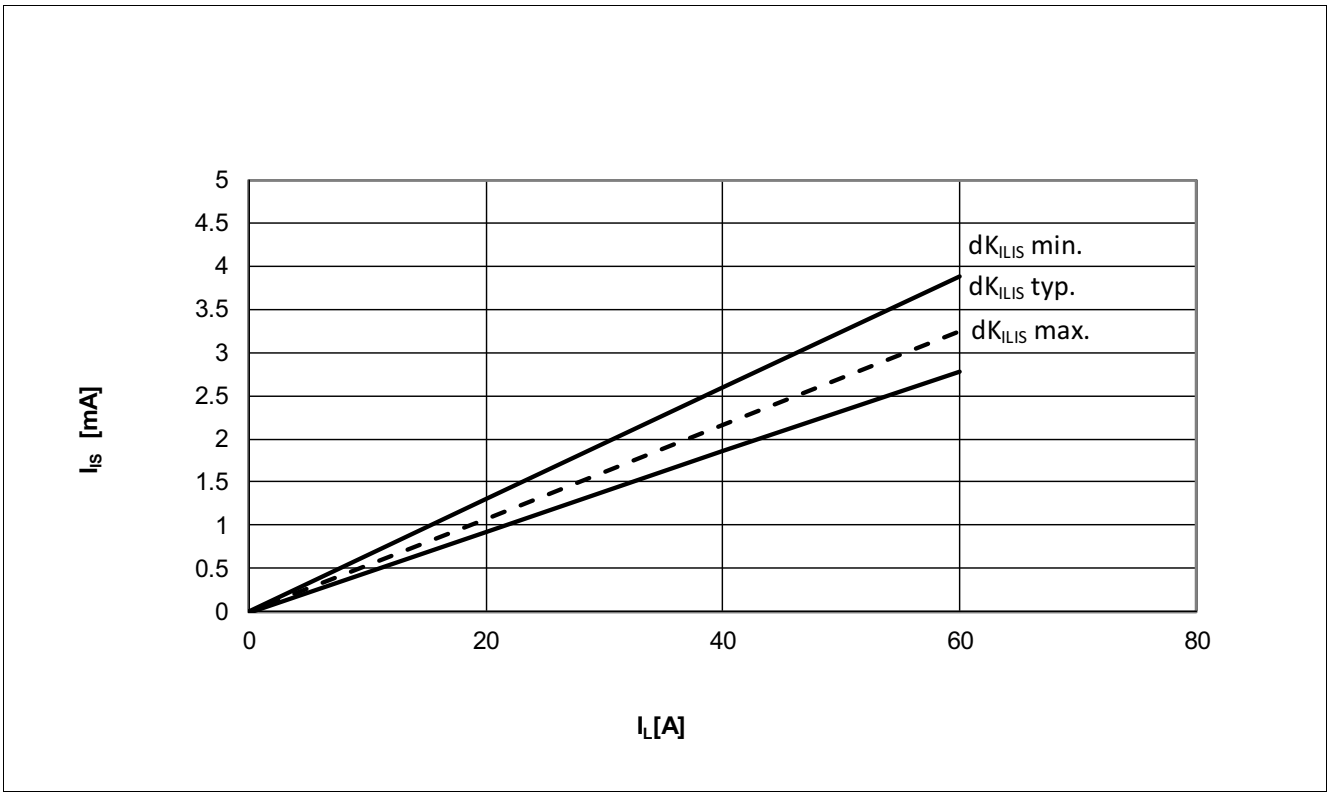



**Figure 5-11 Current Sense for Nominal and Overload Condition**

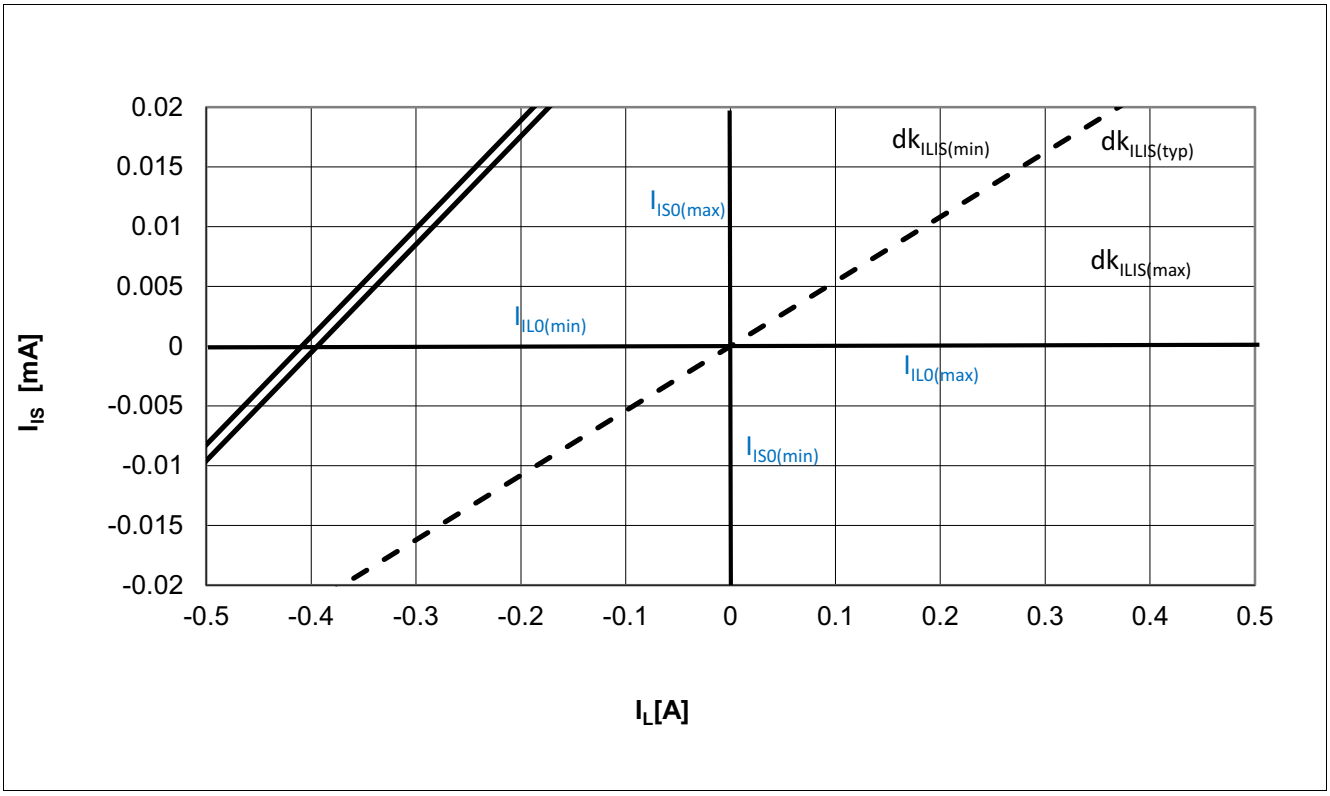



**Figure 5-12 $I_{IL0}$ and $I_{ISO}$ definition**

### 5.4.3.1 SENSE Signal Variation and Calibration

In some applications, an enhanced accuracy is required around the device nominal current range $I_{L(NOM)}$. To achieve this accuracy requirement, a calibration on the application is possible. After two point calibration, the BTS50025-1TEA will have a limited $I_{IS}$ value spread at different load currents and temperature conditions. The $I_{IS}$ variation can be described with the parameters $\Delta(dk_{ILIS(cal)})$ and the $\Delta I_{IS0(cal)}$. The blue solid line in **Figure 5-13** is the current sense ratio after the two point calibration at a given temperature. The slope of this line is defined as follows:

$$\frac{1}{dk_{ILIS(cal)}} = \frac{I_{IS(cal)2} - I_{IS(cal)1}}{I_{L(cal)2} - I_{L(cal)1}} \tag{5.7}$$

The offset is defined as follows:

$$I_{IS0(cal)} = I_{IS(cal)1} - \frac{I_{L(cal)1}}{dk_{ILIS(cal)}} = I_{IS(cal)2} - \frac{I_{L(cal)2}}{dk_{ILIS(cal)}} \tag{5.8}$$

The bluish area in **Figure 5-13** is the range where the current sense ratio can vary across temperature and load current after performing the calibration. The accuracy of the load current sensing is improved and, given a sense current value $I_{IS}$ (measured in the application), the load current can be calculated as follow, using the absolute value for $\Delta(dk_{ILIS(cal)})$ instead of % values:

$$I_L = dk_{ILIS(cal)} \times \left(1 + \Delta(dk_{ILIS(cal)})\right) \times \left(I_{IS} - I_{IS0(cal)} - \Delta I_{IS0(cal)}\right) \tag{5.9}$$

where $dk_{ILIS(cal)}$ is the current sense ratio measured after two-points calibration (defined in **Equation (5.7)**), $I_{IS0(cal)}$ is the current sense offset (calculated after two points calibration, see **Equation (5.8)**), and $\Delta I_{IS0(cal)}$ is the additional variation of the individual offset over life time and temperature. For a calibration at 25°C $\Delta I_{IS0(cal)}$ varies over temperature and life time for all positive $\Delta I_{IS0(cal)}$ within the differences of the temperature dependent Max. limits. All negative $\Delta I_{IS0(cal)}$ vary within the differences of the temperature dependent Min. limits.

For positive $I_{IS0(cal)}$ values ($I_{IS0(cal)} > 0$):

$$\text{Max } I_{IS0}\ (@T_J = 150°C) - \text{Max } I_{IS0}\ (@T_J = 25°C) \le \Delta I_{IS0(cal)} \le \text{Max } I_{IS0}\ (@T_J = -40°C) - \text{Max } I_{IS0}\ (@T_J = 25°C) \quad (5.10)$$

For negative $I_{IS0(cal)}$ values ($I_{IS0(cal)} < 0$):

$$\text{Min } I_{IS0}\ (@T_J = 150°C) - \text{Min } I_{IS0}\ (@T_J = 25°C) \ge \Delta I_{IS0(cal)} \ge \text{Min } I_{IS0}\ (@T_J = -40°C) - \text{Min } I_{IS0}\ (@T_J = 25°C) \quad (5.11)$$

**Equation (5.9)** actually provides four solutions for load current, considering that $\Delta(dk_{ILIS(cal)})$ and $\Delta I_{IS0(cal)}$ can be both positive and negative. The load current $I_L$ for any sense current $I_{IS}$ will spread between a minimum $I_L$ value resulting from the combination of lowest $\Delta(dk_{ILIS(cal)})$ value and highest $\Delta I_{IS0(cal)}$ and a maximum $I_L$ value resulting from the combination of highest $\Delta(dk_{ILIS(cal)})$ value and lowest $\Delta I_{IS0(cal)}$.

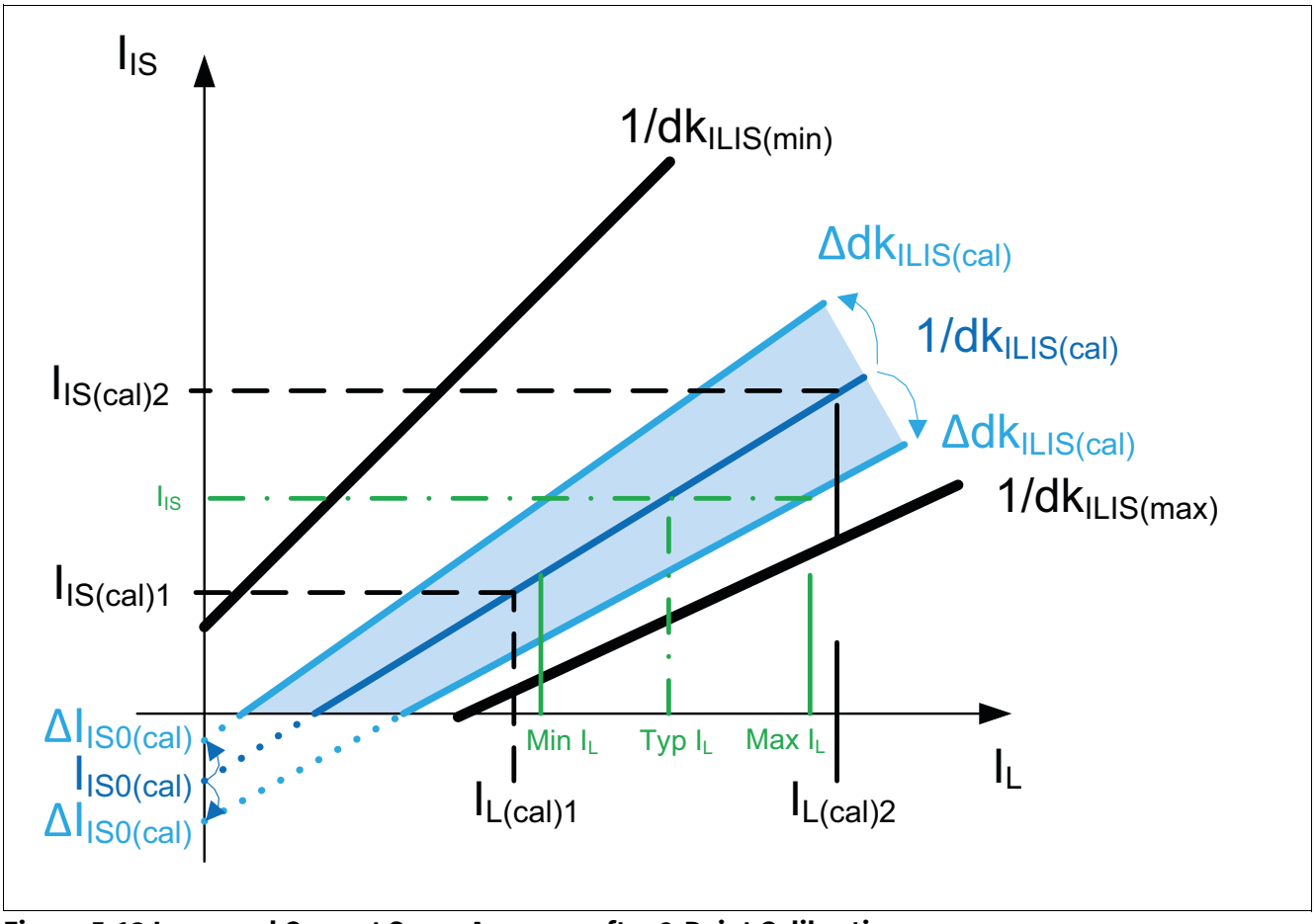



**Figure 5-13 Improved Current Sense Accuracy after 2-Point Calibration**

### 5.4.3.2 SENSE Signal Timing

**Figure 5-14** shows the timing during settling and disabling of the sense.

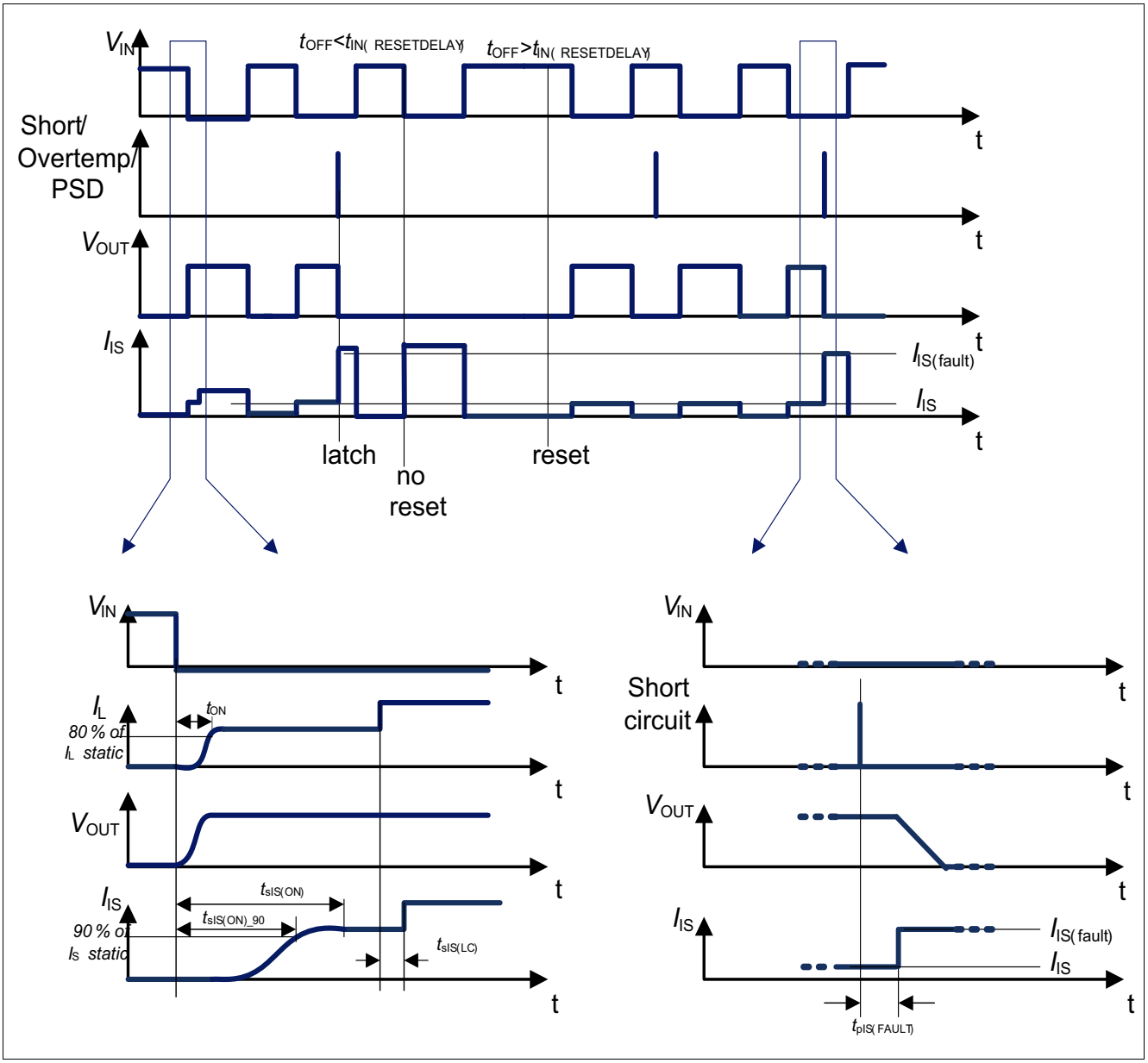



**Figure 5-14 Fault Acknowledgement**

### 5.4.3.3 SENSE Signal in Case of Short Circuit to $V_S$

In case of a short circuit between OUT and VS, a major part of the load current will flow through the short circuit. As a result, a lower current compared to the nominal operation will flow through the DMOS of the BTS50025-1TEA, which can be recognized at the current sense signal.

### 5.4.3.4 SENSE Signal in Case of Over Load

An over load condition is defined by a current flowing out of the DMOS reaching the current over load $I_{CL}$ or the junction temperature reaches the thermal shutdown temperature $T_{J(TRIP)}$. Please refer to **Chapter 5.3.1** for details. In that case, the SENSE signal will be $I_{IS(FAULT)}$ when the IN pin stays LOW.

This is a device with latch functionality. The state of the device will remain and the sense signal will remain on $I_{IS(FAULT)}$ until a reset signal comes from the IN pin. For example, when a thermal shutdown occurs, even when the over temperature condition has disappeared, the DMOS can only be reactivated when a reset signal is sent to the IN pin.

# 6 Electrical Characteristics BTS50025-1TEA

## 6.1 Electrical Characteristics Table

**Table 6-1 Electrical Characteristics: BTS50025-1TEA**

$V_S$ =5.8 V to 18 V, $T_j$ = -40°C to +150°C (unless otherwise specified)
For a given temperature or voltage range, typical values are specified at $V_S$ = 13.5 V, $T_J$ = 25°C

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| **Operating and Standby Currents** | | | | | | | |
| Standby Current for Whole Device with Load | $I_{VS(OFF)}$ | – | 1 | 4 | µA | 1) $V_S$ = 18 V<br>$V_{OUT}$ = 0 V<br>$V_{in}$ = $V_s$<br>$T_J$ ≤ 85°C<br>See **Page 35** | P_6.1.1 |
| Maximum Standby Current for Whole Device with Load | $I_{VS(OFF)}$ | – | 10 | 100 | µA | $V_S$ = 18 V<br>$V_{OUT}$ = 0 V<br>$V_{in}$ = $V_s$<br>$T_J$ ≤ 150°C<br>See Παγε 35 | P_6.1.2 |
| **Power Stage** | | | | | | | |
| ON-State Resistance in Forward Condition | $R_{DS(ON)}$ | – | 4.4 | 5 | mΩ | $I_L$ = 20 A<br>$V_s$ - $V_{in}$ ≥ 5.8 V<br>$T_J$ = 150°C<br>See Παγε 35 | P_6.1.3 |
| ON-State Resistance in Forward Condition | $R_{DS(ON)}$ | – | 2.7 | – | mΩ | 1) $I_L$ = 20 A<br>$V_s$ - $V_{in}$ ≥ 5.8 V<br>$T_J$ = 25°C | P_6.1.4 |
| ON-State Resistance in Forward Condition, Low Battery Voltage | $R_{DS(ON)}$ | – | 6 | 20 | mΩ | $I_L$ = 12 A<br>$V_s$ - $V_{in}$ ≥ 3.1 V<br>$T_J$ = 150°C | P_6.1.5 |
| ON-State Resistance in Forward Condition, Low Battery Voltage | $R_{DS(ON)}$ | – | 3.5 | – | mΩ | 1) $I_L$ = 12 A<br>$V_s$ - $V_{in}$ ≥ 3.1 V<br>$T_J$ = 25°C | P_6.1.6 |
| Nominal Load Current | $I_{L(NOM)}$ | 24 | 26 | – | A | 2) $T_A$ = 85°C<br>$T_J$ ≤ 150°C | P_6.1.7 |
| Drain to Source Smart Clamp Voltage $V_{DS(CL)}$ = $V_S$ - $V_{OUT}$ | $V_{DS(CL)}$ | 30 | 35 | 45 | V | $I_{DS}$ = 10 mA<br>$T_J$ = 25°C<br>See **Page 37** | P_6.1.8 |
| Drain to Source Smart Clamp Voltage $V_{DS(CL)}$ = $V_S$ - $V_{OUT}$ | $V_{DS(CL)}$ | 35 | 39 | 50 | V | $I_{DS}$ = 10 mA<br>$T_J$ = 150°C<br>See **Page 37** | P_6.1.9 |
| Fast turn off detection voltage | $V_{DS(FAST)}$ | – | 28 | – | V | 1) See **Page 16** | P_6.1.10 |

**Table 6-1 Electrical Characteristics: BTS50025-1TEA** (cont'd)

$V_S$ =5.8 V to 18 V, $T_j$ = -40°C to +150°C (unless otherwise specified)
For a given temperature or voltage range, typical values are specified at $V_S$ = 13.5 V, $T_J$ = 25°C

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| Body diode Forward voltage | $V_F$ | – | 0.6 | 0.8 | V | $I_{OUT}$ = -20A<br>$T_J$ = 150°C | P_6.1.11 |
| Output Leakage Current | $I_{L(OFF)}$ | – | 1 | 4 | µA | 1) $V_S$ = 18 V<br>$V_{OUT}$ = 0 V<br>$V_{in}$ = $V_s$<br>$T_J \leq$ 85°C<br>( 10ms after<br>$V_S$ = $V_{IN}$ ) | P_6.1.12 |
| Output Leakage Current | $I_{L(OFF)}$ | – | 10 | 100 | µA | $V_S$ = 18 V<br>$V_{OUT}$ = 0 V<br>$V_{in}$ = $V_s$<br>$T_J \leq$ 150°C<br>( 10ms after<br>$V_S$ = $V_{IN}$ ) | P_6.1.13 |
| Turn ON Slew Rate<br>$V_{OUT}$ = 25% to 50% $V_S$ | $dV_{ON}/dt$ | 0.05 | 0.25 | 1 | V/µs | $R_L$ = 0.68 Ω<br>$V_S$ = 13.5 V<br>See **Figure 5-1**<br>See **Page 36** | P_6.1.14 |
| Turn OFF Slew Rate<br>$V_{OUT}$ = 50% to 25% $V_S$ | $-dV_{OFF}/dt$ | 0.05 | 0.25 | 1 | V/µs | | P_6.1.15 |
| Rising time during turn on<br>$V_{OUT}$ from 20% to 80% of $V_S$ | $t_r$ | 10 | 50 | 150 | µs | | P_6.1.16 |
| Falling time during turn off<br>$V_{OUT}$ from 80% to 20% of $V_S$ | $t_f$ | 10 | 50 | 150 | µs | | P_6.1.17 |
| Turn ON Time to<br>$V_{OUT}$ = 20% of $V_S$ | $t_{ON(DELAY)}$ | 10 | 50 | 250 | µs | | P_6.1.18 |
| Turn OFF Time to<br>$V_{OUT}$ = 80% of $V_S$ | $t_{OFF(DELAY)}$ | 50 | 150 | 450 | µs | | P_6.1.19 |
| Switch ON Energy | $E_{ON}$ | – | 5.5 | – | mJ | 1) $R_L$ = 0.68 Ω<br>$V_S$ = 13.5 V<br>See **Page 37** | P_6.1.20 |
| Switch OFF Energy | $E_{OFF}$ | – | 4 | – | mJ | 1) $R_L$ = 0.68 Ω<br>$V_S$ = 13.5 V<br>See **Page 37** | P_6.1.21 |

**Table 6-1 Electrical Characteristics: BTS50025-1TEA** (cont'd)

$V_S$ =5.8 V to 18 V, $T_j$ = -40°C to +150°C (unless otherwise specified)
For a given temperature or voltage range, typical values are specified at $V_S$ = 13.5 V, $T_J$ = 25°C

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| **Input Pin** | | | | | | | |
| LOW Level Input Voltage | $V_{VS-VIN(L)}$ | 2.3 | 2.7 | 3.1 | V | | P_6.1.22 |
| HIGH Level Input Voltage | $V_{VS-VIN(H)}$ | 4 | 4.8 | 5.8 | V | | P_6.1.23 |
| Input Voltage Hysteresis | $V_{VS-VIN(HYS)}$ | 1.7 | 2.1 | 2.5 | V | | P_6.1.24 |
| On stage Input Current | $I_{IN(ON)}$ | 1 | 2 | 4 | mA | $V_S$ - $V_{IN}$ = 18 V, $V_S$ = 18V | P_6.1.25 |
| LOW Level Input Current | $I_{IN(L)}$ | 100 | – | – | µA | $V_{IN}$ = $V_{in(L)}$ | P_6.1.26 |
| Input resistor | $R_{in}$ | 115 | 200 | 300 | Ω | Built-in | P_6.1.27 |
| **Protection: Reverse Polarity** | | | | | | | |
| ON-State Resistance in Reverse Polarity | $R_{DS(REV)}$ | – | 5 | 10 | mΩ | $V_S$ = 0 V<br>$V_S$ - $V_{IN}$ = -16 V<br>$I_L$ = -20 A<br>$T_J$ = 150°C | P_6.1.28 |
| ON-State Resistance in Reverse Polarity | $R_{DS(REV)}$ | – | 4 | – | mΩ | [1] $V_S$ = 0 V<br>$V_S$ - $V_{IN}$ = -16 V<br>$I_L$ = -20 A<br>$T_J$ = 25°C<br>See **Page 37** | P_6.1.29 |
| **Protection: Overload** | | | | | | | |
| Current Trip Detection Level | $I_{CL(0)}$ | 65 | 82 | 100 | A | 5.8V < $V_S$ - $V_{IN}$< 27V<br>See **Figure 5-9** | P_6.1.30 |
| Current Trip Detection Level at low voltage | $I_{CL(0_UV)}$ | 12 | 82 | 120 | A | $V_S$ = 3.1V | P_6.1.32 |
| Current Trip Maximum Level | $I_{CL(1)}$ | 65 | 92 | 140 | A | $dI_L/dt$ = 1 A/µs<br>See **Figure 5-9** | P_6.1.33 |
| Overload Shutdown Delay Time | $t_{OFF(TRIP)}$ | – | 7 | – | µs | [1] See **Figure 5-9** | P_6.1.34 |
| Thermal Shutdown Temperature | $T_{J(TRIP)}$ | 150 | 175[1] | 200[1] | °C | See **Figure 5-9**<br>3.1V < $V_S$ - $V_{IN}$< 27V | P_6.1.35 |
| Over Power Shutdown Detection Level | $V_{DS(PSD)}$ | 650 | 900 | 1100 | mV | [1] See **Figure 5-7** | P_6.1.36 |
| Over Power Shutdown Activation Level | $V_{VS-VIN(PSD)}$ | 3.8 | 4.3 | 5 | V | [1] See **Figure 5-7** | P_6.1.37 |
| Over Power Shutdown Time | $t_{PSD(UV)}$ | 10 | 50 | 300 | µs | See **Figure 5-7** | P_6.1.38 |
| | | | | | | | |
| | | | | | | | |

**Table 6-1 Electrical Characteristics: BTS50025-1TEA** (cont'd)

$V_S$ =5.8 V to 18 V, $T_j$ = -40°C to +150°C (unless otherwise specified)
For a given temperature or voltage range, typical values are specified at $V_S$ = 13.5 V, $T_J$ = 25°C

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| **Diagnostic Function: Sense Pin** | | | | | | | |
| Sense Signal Current in Fault Condition | $I_{IS(FAULT)}$ | 5 | 12 | 18 | mA | $V_S$ - $V_{IS}$ ≥ 3.5 V Typ. and Max. value: $V_S$ - $V_{IS}$ ≥ 8 V | P_6.1.39 |
| Sense Signal Saturation Current | $I_{IS(LIM)}$ | 4.4 | 6.5 | – | mA | [1] $V_S$ - $V_{IS}$ ≥ 3.5 V | P_6.1.40 |

**Table 6-1 Electrical Characteristics: BTS50025-1TEA** (cont'd)

$V_S$ =5.8 V to 18 V, $T_j$ = -40°C to +150°C (unless otherwise specified)
For a given temperature or voltage range, typical values are specified at $V_S$ = 13.5 V, $T_J$ = 25°C

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| **Diagnostic Function: Current Sense Ratio Signal in the Nominal Area, Stable Current Load Condition** | | | | | | | |
| Current Sense Differential Ratio | $dk_{ILIS}$ | 15500 | 18000 | 20500 | – | $I_{L3}$ = 60 A<br>$I_{L1}$ = 0.2 A<br>$V_S$ - $V_{IS}$ ≥ 3.5 V<br>See **Equation (5.4)** | P_6.1.41 |
| Calculated Sense Offset load Current<br>$I_S$ = 0 A, Tj=-40°C | $I_{L0}$ | -0.15 | 0 | 0.15 | A | [3] $V_S$ - $V_{IS}$ ≥ 3.5 V<br>See **Figure 5-11** | P_6.1.42 |
| Calculated Sense Offset load Current<br>$I_S$ = 0 A, Tj=25°C | $I_{L0}$ | -0.13 | 0 | 0.13 | A | [3] $V_S$ - $V_{IS}$ ≥ 3.5 V<br>See **Figure 5-11** | P_6.1.60 |
| Calculated Sense Offset load Current<br>$I_S$ = 0 A, Tj=150°C | $I_{L0}$ | -0.105 | 0 | 0.105 | A | [3] $V_S$ - $V_{IS}$ ≥ 3.5 V<br>See **Figure 5-11** | P_6.1.61 |
| Calculated Sense Offset Current<br>$I_L$ = $I_{L0}$ = 0 A, Tj=-40°C | $I_{IS0}$ | -7 | 0 | 9.7 | µA | [3] $V_S$ - $V_{IS}$ ≥ 3.5 V<br>Tj=-40°C<br>See **Figure 5-11** | P_6.1.43 |
| Calculated Sense Offset Current<br>$I_L$ = $I_{L0}$ = 0 A, Tj=25°C | $I_{IS0}$ | -5.95 | 0 | 8.25 | µA | [3] $V_S$ - $V_{IS}$ ≥ 3.5 V<br>Tj=25°C<br>See **Figure 5-11** | P_6.1.58 |
| Calculated Sense Offset Current<br>$I_L$ = $I_{L0}$ = 0 A, Tj=150°C | $I_{IS0}$ | -4.9 | 0 | 6.8 | µA | [3] $V_S$ - $V_{IS}$ ≥ 3.5 V<br>Tj=150°C<br>See **Figure 5-11** | P_6.1.59 |
| Sense Current<br>$I_L$ = $I_{L1}$ = 0.2 A | $I_{IS1}$ | 2.3 | 10.8 | 22.6 | µA | $V_S$ - $V_{IS}$ ≥ 3.5 V<br>See **Figure 5-11** | P_6.1.44 |
| Sense Current<br>$I_L$ = $I_{L2}$ = 20 A | $I_{IS2}$ | 0.92 | 1.08 | 1.3 | mA | $V_S$ - $V_{IS}$ ≥ 3.5 V<br>See **Figure 5-11** | P_6.1.45 |
| Sense Current<br>$I_L$ = $I_{L3}$ = 60 A | $I_{IS3}$ | 2.78 | 3.24 | 3.88 | mA | $V_S$ - $V_{IS}$ ≥ 3.5 V<br>See **Figure 5-11** | P_6.1.46 |
| Current Sense Ratio Spread between -40°C and 25°C for Repetitive Operation | $\Delta(dk_{ILIS(cal)(-40°C)})$ | -1.5 | 0 | +1.5 | % | [1] $(dk_{ILIS(cal)(-40°C)}$ - $dk_{ILIS(cal)(25°C)})/$ $dk_{ILIS(cal)(25°C)}$<br>See **Figure 5-13** | P_6.1.47 |
| Current Sense Ratio Spread between 150°C and 25°C for Repetitive Operation | $\Delta(dk_{ILIS(cal)(150°C)})$ | -3.5 | -0.8 | +2 | % | [1] $(dk_{ILIS(cal)(150°C)}$ - $dk_{ILIS(cal)(25°C)})/$ $dk_{ILIS(cal)(25°C)}$<br>See **Figure 5-13** | P_6.1.48 |
| | | | | | | | |
| | | | | | | | |

**Table 6-1 Electrical Characteristics: BTS50025-1TEA** (cont'd)

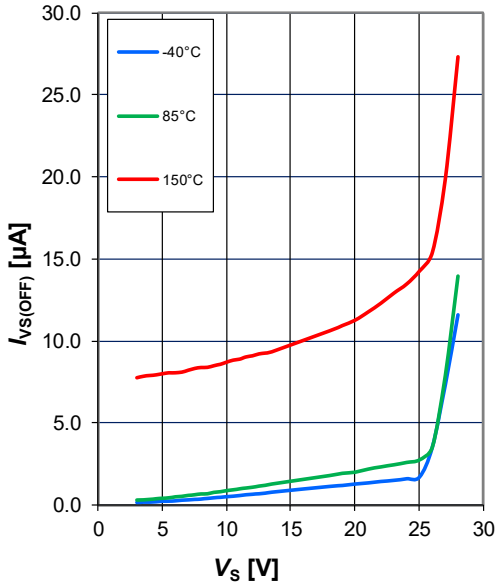
$V_S$ =5.8 V to 18 V, $T_j$ = -40°C to +150°C (unless otherwise specified)
For a given temperature or voltage range, typical values are specified at $V_S$ = 13.5 V, $T_J$ = 25°C

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| **Diagnostic Function: Diagnostic Timing in Normal Condition** | | | | | | | |
| Current Sense Settling Time until 90% and 110% of $I_{IS}$ Stable after turn on | $t_{sIS(ON)_90}$ | – | – | 700 | µs | $V_S$ = 13.5 V<br>$R_L$ = 0.68 Ω<br>See **Figure 5-14** | P_6.1.49 |
| Current Sense Settling Time to $I_{IS}$ Stable after turn on | $t_{sIS(ON)}$ | – | – | 1500 | µs | $V_S$ = 13.5 V<br>$R_L$ = 0.68 Ω<br>See **Figure 5-14** | P_6.1.50 |
| $I_{IS}$ Leakage Current when IN Disabled | $I_{IS(OFF)}$ | – | – | 1 | µA | $V_{IN}$ = $V_S$<br>$R_{IS}$ = 1k Ω<br>$T_J$ ≤ 150°C | P_6.1.51 |
| Current Sense Settling Time after Load Change | $t_{sIS(LC)}$ | – | 5 | – | µs | [1] $I_L$ ≥ 0.2 A | P_6.1.52 |
| **Diagnostic Function: Diagnostic Timing in Overload Condition** | | | | | | | |
| Fault Propagation Time for Short Circuit Detection | $t_{pIS(FAULT)}$ | – | 3 | 20 | µs | See **Figure 5-14** | P_6.1.53 |
| Fault Propagation Time for Over temperature Detection | $t_{FAULT(OT)}$ | – | 100 | – | µs | [1] | P_6.1.55 |
| Delay Time to Reset Fault Pin after Turning OFF $V_{IN}$ | $t_{IN(RESETDELAY)}$ | 6 | – | 5000 | µs | See **Figure 5-14** | P_6.1.54 |

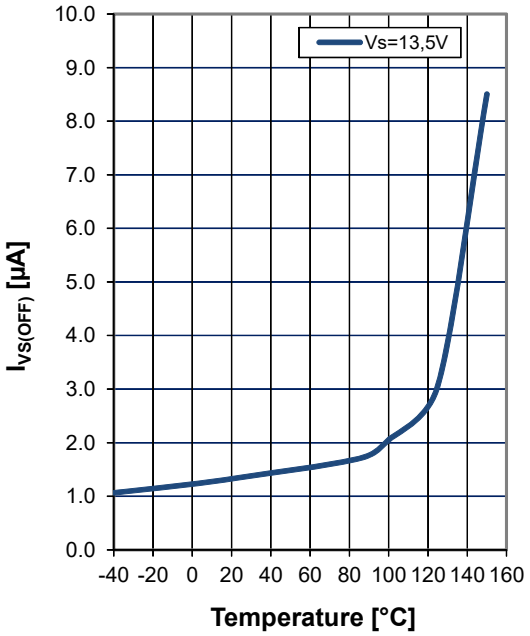
1) Not subject to production test, specified by design.
2) Value is calculated from the parameters typ. $R_{thJA(2s2p)}$, with 65 K temperature increase, typ. and max. $R_{DS(ON)}$.
3) Value is calculated from the parameters d$k_{ILIS}$ and $I_{IS1}$.

## 6.2 Typical Performance Characteristics

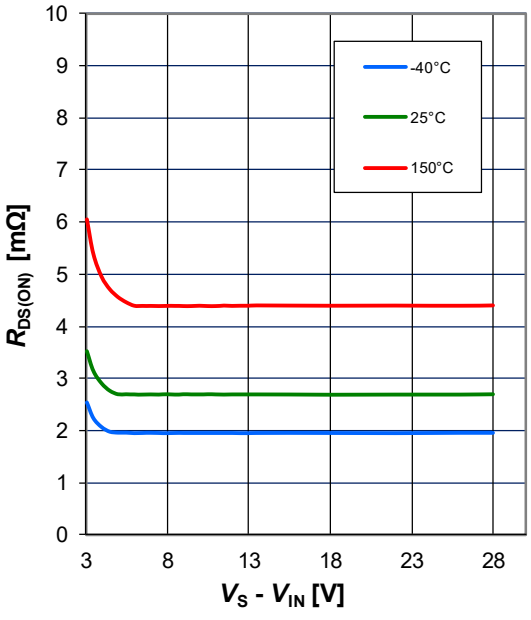
**Standby Current for Whole Device with Load, $I_{VS(OFF)} = f(V_S, T_J)$, -40°C, 85°C, 150°C**



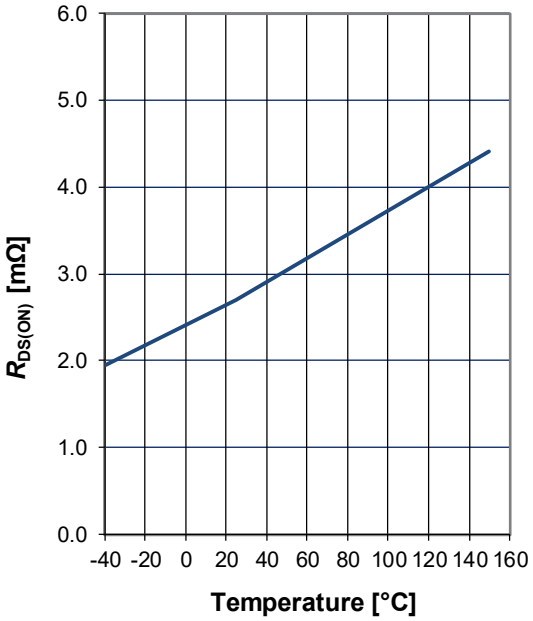

**Standby Current for Whole Device with Load, $I_{VS(OFF)} = f(T_J)$ at $V_S$ = 13.5 V**



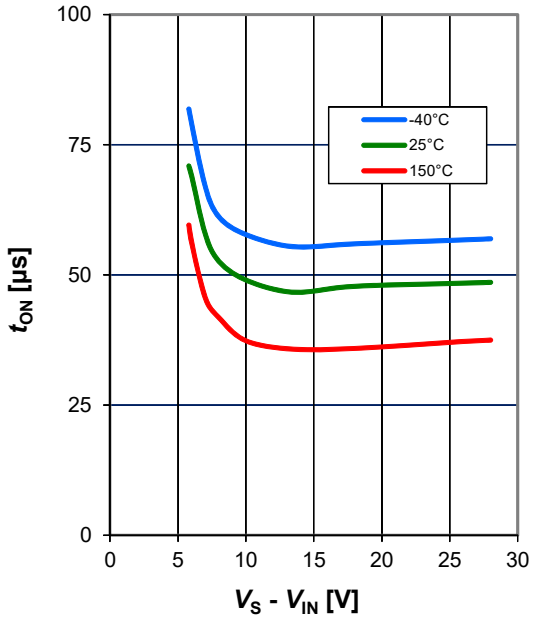

**ON State Resistance**
**$R_{DS(ON)} = f(V_S - V_{IN}, T_J)$, $I_L$ = 10 A ... $I_{CL}(0)$ min; -40°C, 25°C, 150°C**



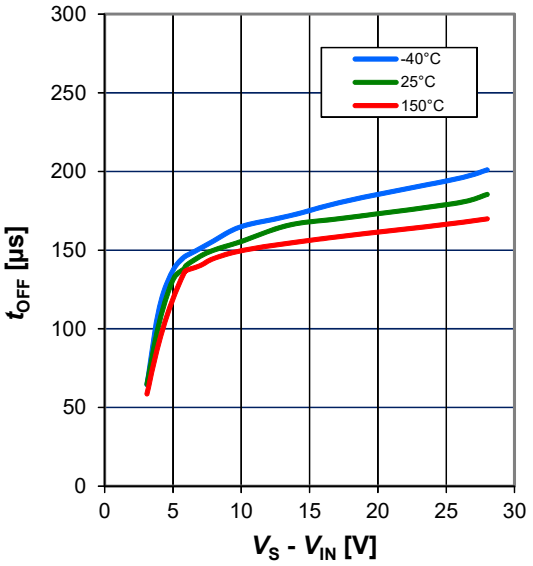

**ON State Resistance**
**$R_{DS(ON)} = f(T_J), V_S - V_{IN}$= 13.5 V, $I_L$ = 10 A ... $I_{CL}(0)$ min**



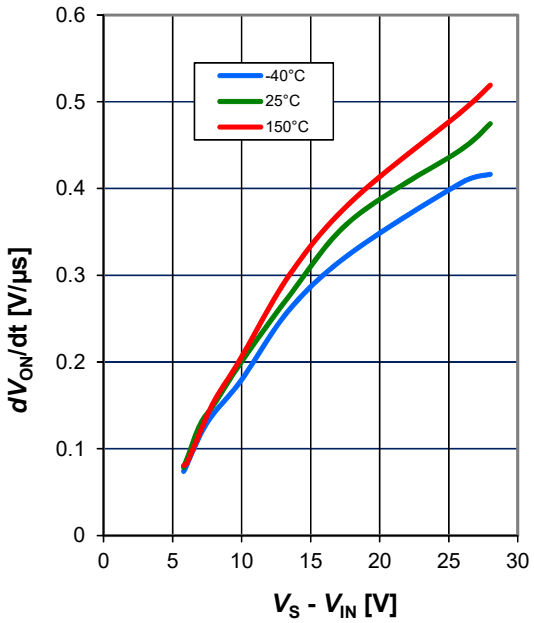
### Turn ON Time
$t_{ON} = f(V_S, T_J), R_L = 0.68\ \Omega$



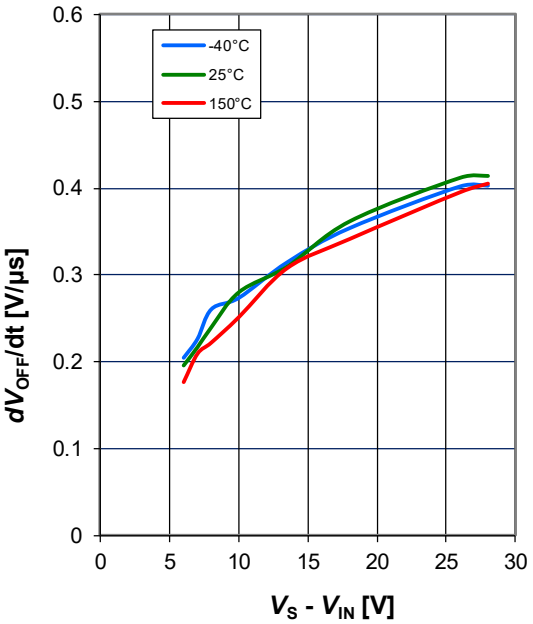

### Turn OFF Time
$t_{OFF} = f(V_S, T_J), R_L = 0.68\ \Omega$



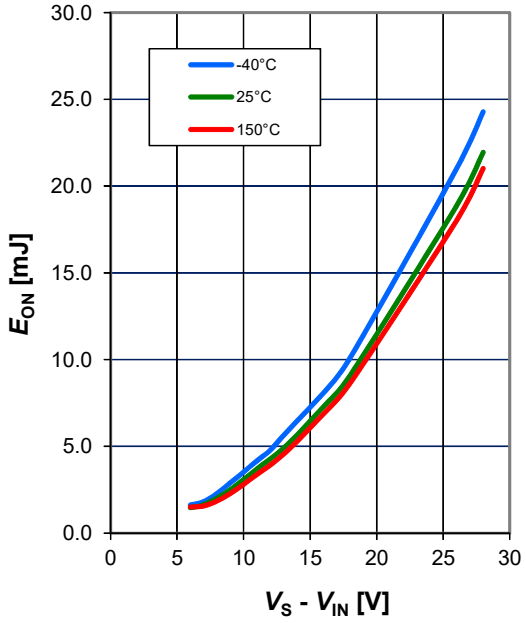

### Slew Rate at Turn ON
$dV_{ON} / dt = f(V_S, T_J), R_L = 0.68\ \Omega$



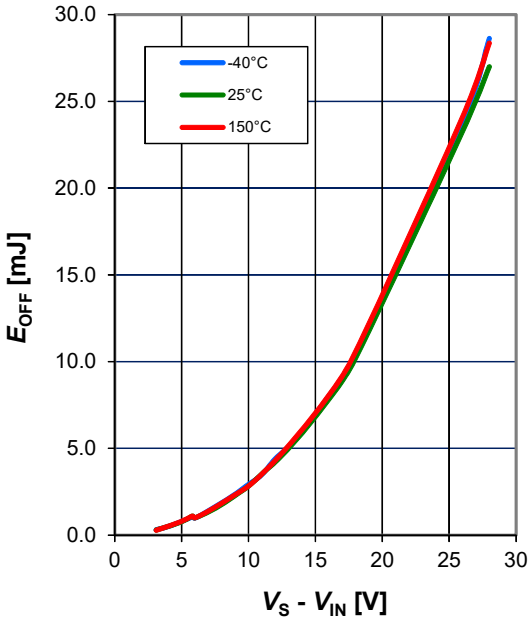

### Slew Rate at Turn OFF
$dV_{OFF} / dt = f(V_S, T_J), R_L = 0.68\ \Omega$



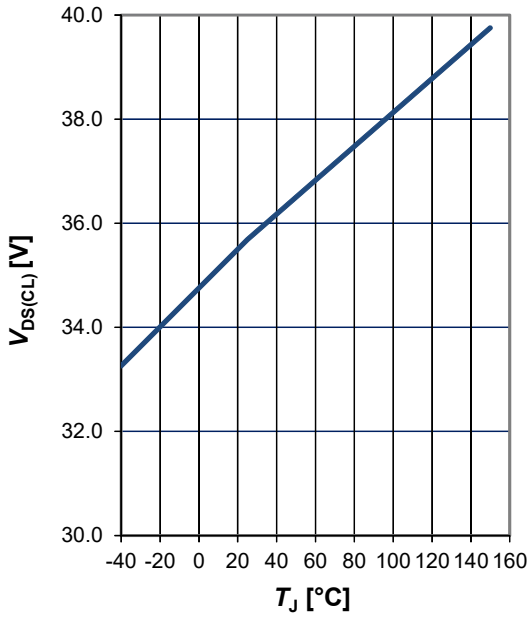
### Switch ON Energy
$E_{ON} = f(V_S, T_J), R_L = 0.68\ \Omega$



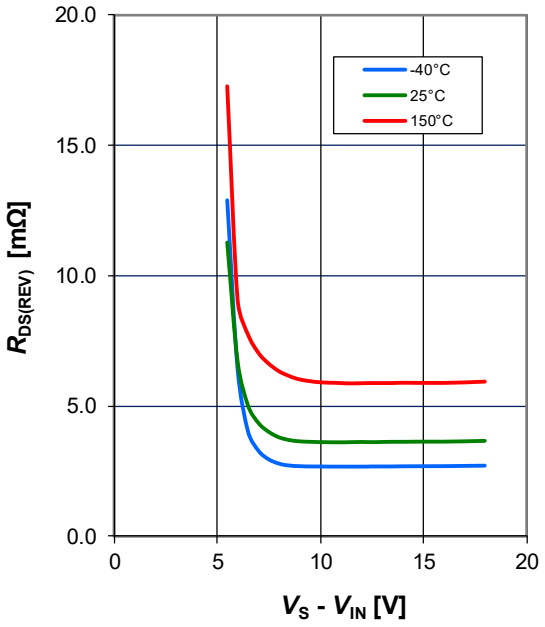

### Switch OFF Energy
$E_{OFF} = f(V_S, T_J), R_L = 0.68\ \Omega$



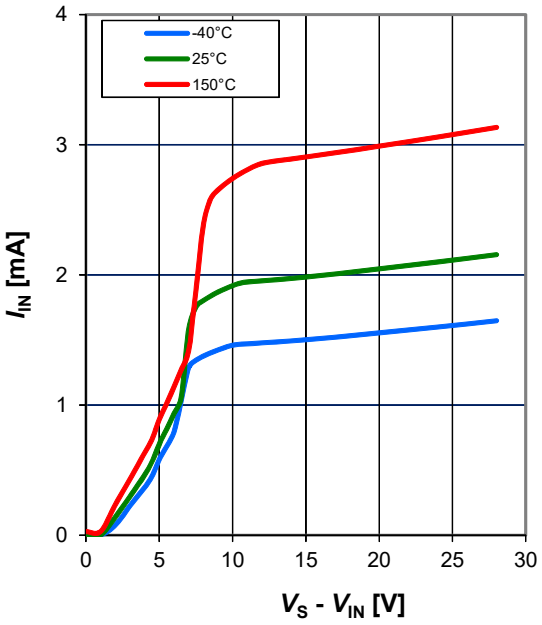

### Drain to Source Clamp Voltage
$V_{DS(CL)} = f(T_J), I_L = 10\ mA$



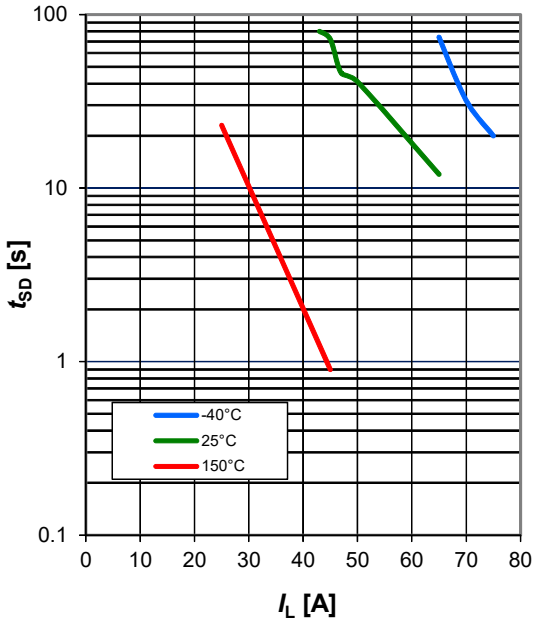

### Resistance in ReverSave™
$R_{DS(REV)} = f(V_S, T_J), I_L = -20\ A$



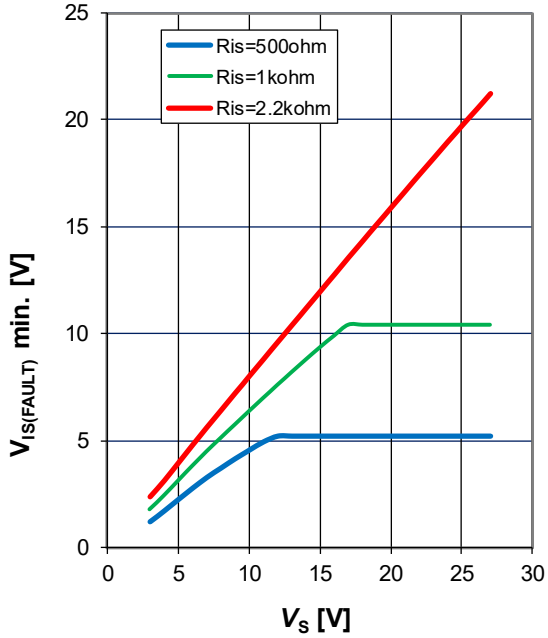
### Input Current
$I_{IN} = f(V_S, T_J)$



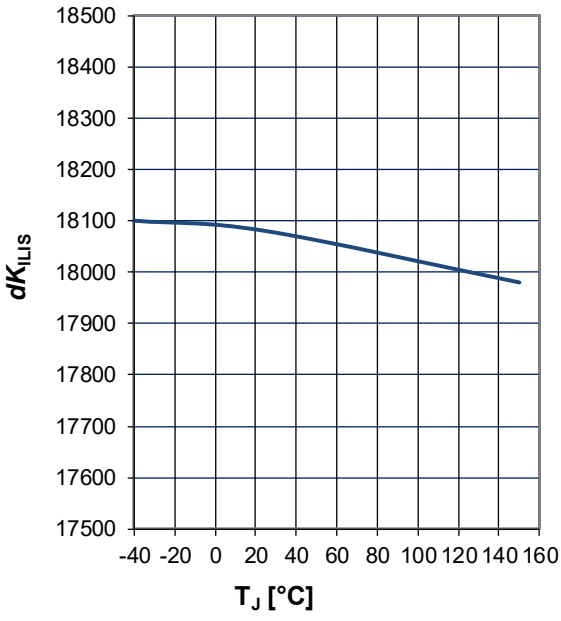

### Time to Shutdown
$t_{SHUTDOWN}$ Vs $I_L$ , $R_{thJA(2s2p)}$




### $V_{IS(FAULT)}$ min. Vs $V_S$; $R_{IS}$ = 500Ω, 1 kΩ, 2.2 kΩ

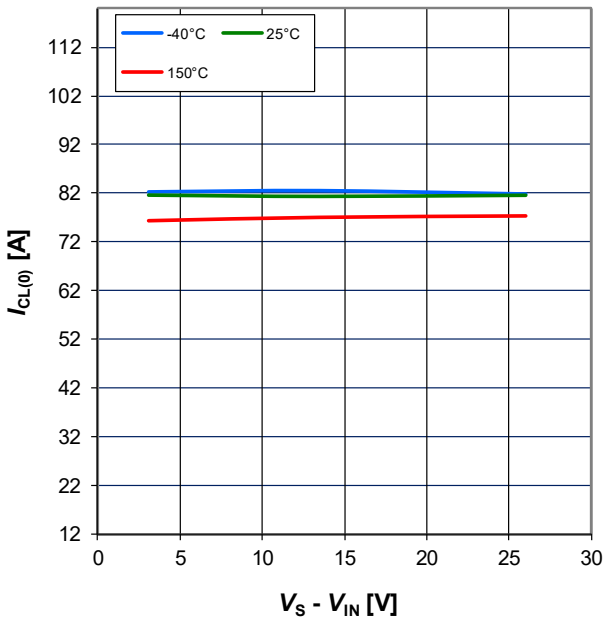



### $dK_{ILIS}$ Vs $T_J$



## Electrical Characteristics BTS50025-1TEA

$I_{CL(0)} = f(V_S, T_J)$



# 7 Application Information

*Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.This is a very simplified example of an application circuit. The function must be verified in the real application.*

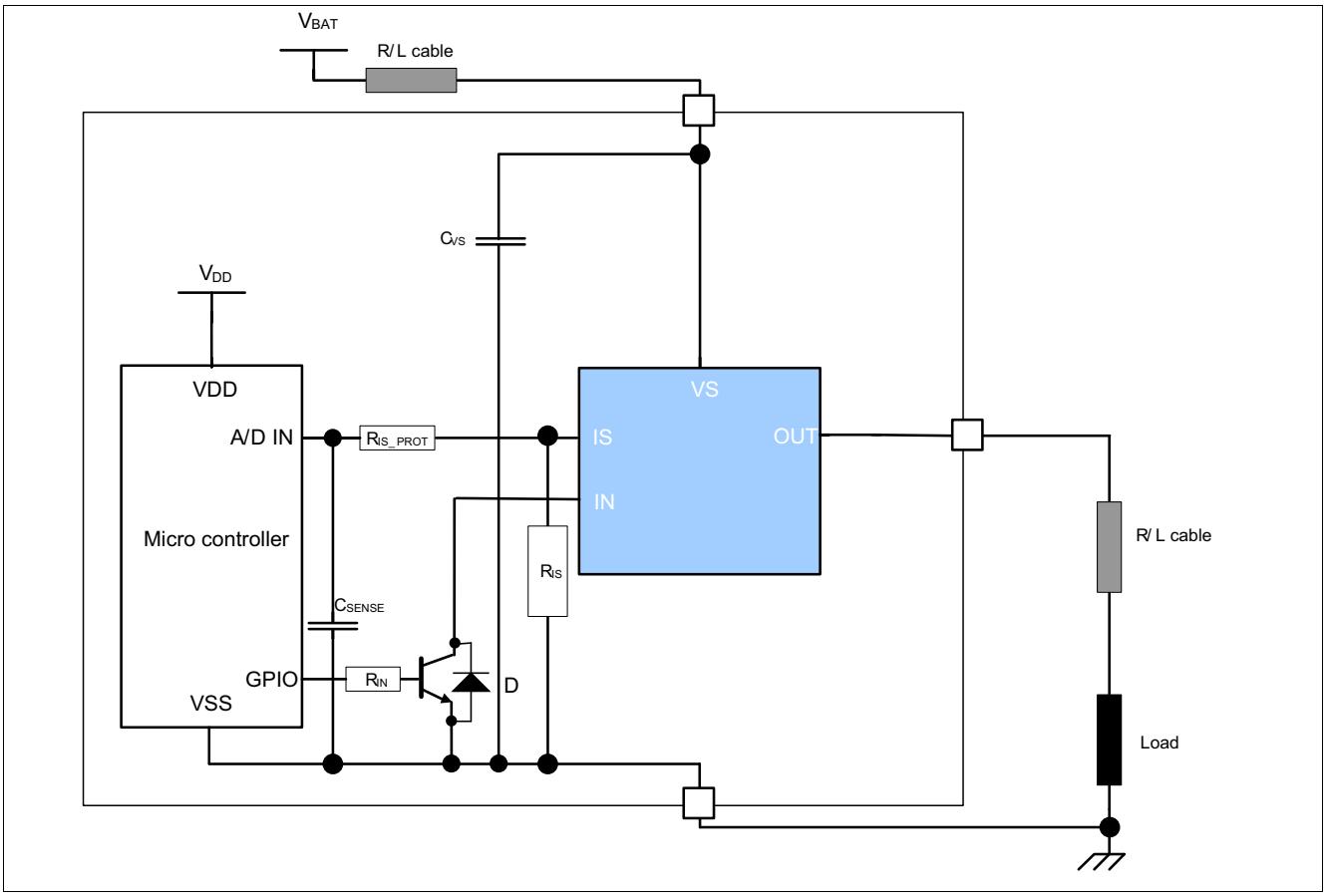



**Figure 7-1 Application Diagram with BTS50025-1TEA**

**Table 7-1 Bill of material**

| Reference | Value | Purpose |
|---|---|---|
| $R_{IN}$ | 4.7 kΩ | Protection of the microcontroller during reverse polarity and during loss of ground |
| $R_{IS}$ | 1 kΩ | Sense resistor |
| $R_{IS_PROT}$ | 10 kΩ | Protection of the microcontroller during fault condition<br>Protection of the BTS50025-1TEA and the microcontroller during reverse polarity |
| $C_{SENSE}$ | 10 nF | Sense signal filtering |
| $C_{VS}$ | 100 nF | Improved EMC behavior (in layout, pls. place close to the pins) |
| $D$ | | To turn on the Power Mosfet during reverse polarity |

## 7.1 Further Application Information

- Please contact us for information regarding the pin FMEA
- For further information you may contact **http://www.infineon.com/**

# 8 Package Information

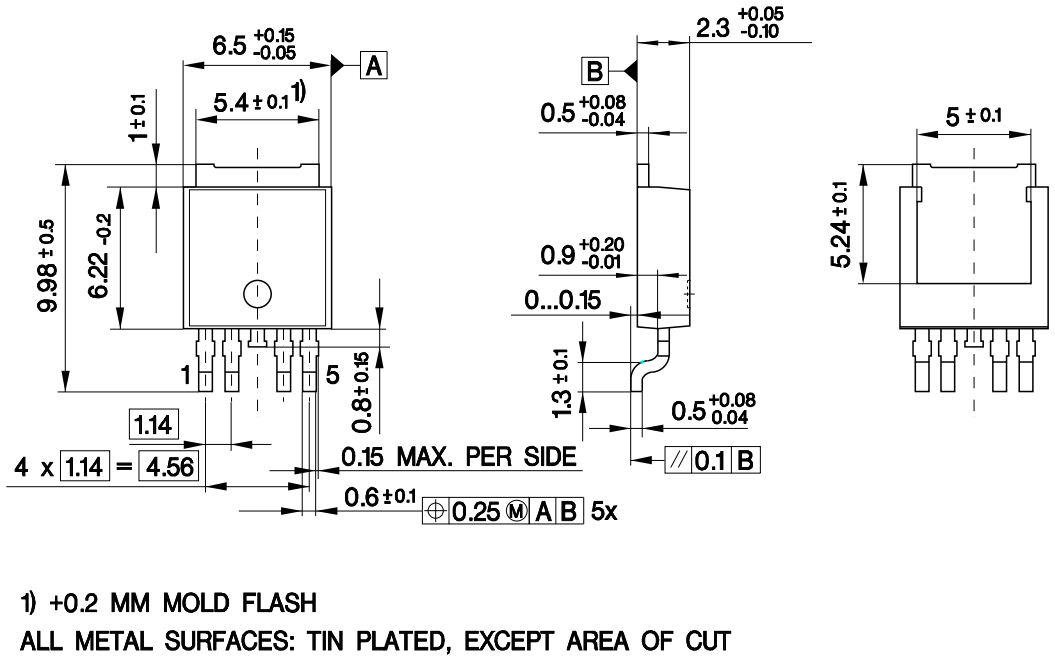



**Figure 8-1 PG-TO-252-5-11** (RoHS-Compliant)[1)]

### Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e. Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

1) Dimensions in mm

# 9 Revision History

| Revision | Date | Changes |
|---|---|---|
| 1.1 | 2019-09-30 | Chapter “Electrical Characteristics”<br>• Change P_6.1.30 and P_6.1.33 minimum limit from 60A to 65A<br>• Change P_6.1.30 and P_6.1.32 typical value from 80A to 82A<br>• Change P_6.1.33 typical value from 87A to 92A |
| 1.0 | 2018-08-16 | Datasheet created |

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