

Bilkent University
Computer Engineering Department
CS224- Computer Organization
Preliminary Design Report
Section 1
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b) Machine code to assembly instruction

Location	Machine Code	MIPS instruction
0x00000000	0x20020005	addi \$v0, \$zero, 5
0x00000004	0x2003000c	addi \$v1, \$zero, 12
0x00000008	0x2067fff7	addi \$a3, \$v1, -9
0x0000000C	0x00e22025	or \$a0, \$a3, \$v0
0x00000010	0x00642824	and \$a1, \$v1, \$a0
0x00000014	0x00a42820	add \$a1, \$a1, \$a0
0x00000018	0x10a7000a	beq \$a1, \$a3, 10
0x0000001C	0x0064202a	slt \$a0, \$v1, \$a0
0x00000020	0x10800001	beq \$a0, \$zero, 1
0x00000024	0x20050000	addi \$a1, \$zero, 0
0x00000028	0x00e2202a	slt \$a0, \$a3, \$v0
0x0000002C	0x00853820	add \$a3, \$a0, \$a1
0x00000030	0x00e23822	sub \$a3, \$a3, \$v0
0x00000034	0xac670044	sw \$a3, 68(\$v1)
0x00000038	0x8c020050	lw \$v0, 80(\$zero)
0x0000003C	0x08000011	j 0x00000011
0x00000040	0x20020001	addi \$v0, \$zero, 1
0x00000044	0xac020054	sw \$v0, 84(\$zero)
0x00000048	0x08000012	j 0x00000012

c) RTL expressions for new instructions

lui rt, imm:

$R[rt] = \{imm, 16'b0\}$

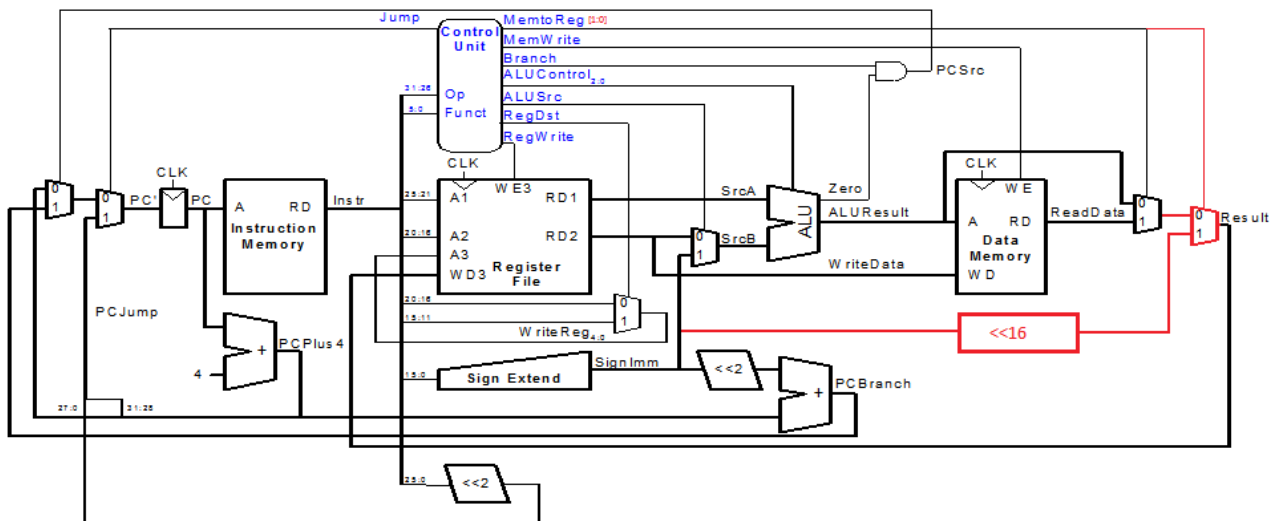
$PC \leftarrow PC + 4$

jalm rt, imm(rs):

$R[rt] = R[pc] + 4$

$R[pc] = M[R[rs] + imm]$

d) Additions to datapath



e) Table

Instruc- tion	Op_{5:0}	Reg Write	Reg Dst	Alu Src	Branch	Mem Write	Mem toReg	ALU Op_{1:0}	Jump
R-type	000000	1	1	0	0	0	0	1x	0
lw	100011	1	0	1	0	0	1	00	0
sw	101011	0	X	1	0	1	X	00	0
beq	000100	0	X	0	1	0	X	01	0
j	000010	0	X	X	X	0	X	XX	1
addi	001000	1	0	1	0	0	0	00	0
lui	001111	1	0	0	0	0	01	XX	0
jalm	010111	0	1	1	X	0	00	00	1

f) Test code

L1:

// Set values to zero

addi \$s0, \$zero, 0

addi \$s1, \$zero, 0

addi \$s2, \$zero, 0

addi \$s3, \$zero, 0

addi \$s0, \$s0, 5

add \$s0, \$s0, \$s0

sub \$s0, \$s0, 5

addi \$s1, \$s1, 3

and \$s2, \$s0, \$s1

or \$s2, \$s0, \$s1

slt \$s2, \$s0, \$s1

slt \$s2, \$s1, \$s0

sw \$s0, 4(\$s1)

lw \$s3, 4(\$s1)

beq \$s3, 999, L2

beq \$s0, 5, L2

nop

L2:

lui \$s4, 0x1234

addi \$s4, \$zero, 0

jalm \$t0, 84(\$s4)

nop

nop

j L1