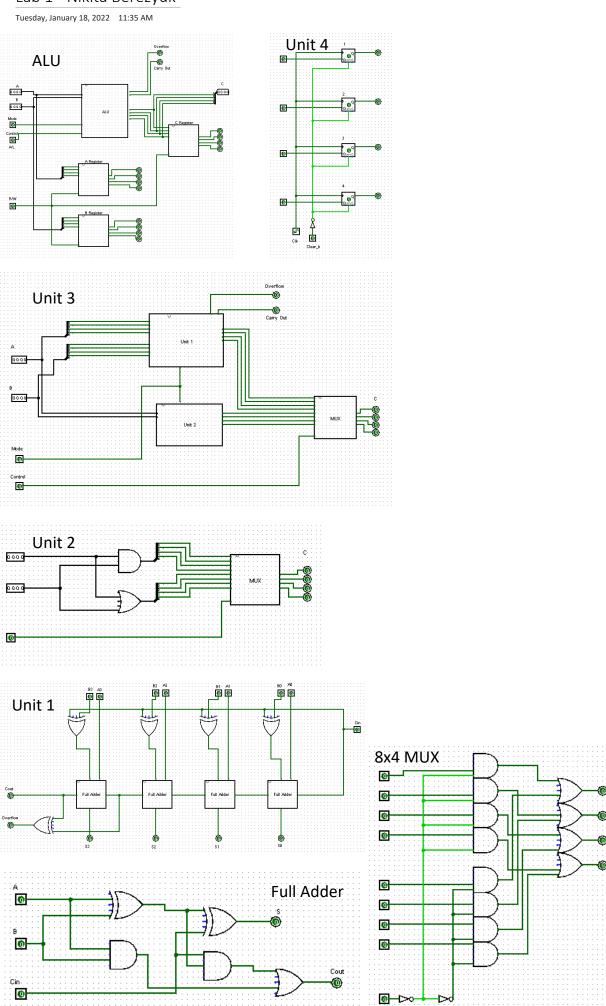
Lab 1 - Nikita Berezyuk



Read

Write

1	1	1	1	0	1	1	1	0	1	1	1	0
1	1	1	1	0	1	1	1	0	1	1	1	0
1	1	1	1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1	1	1	1

Explanation:

When clear_b is 0, the registers read the input every clock iteration and update the next state. But then it is 1, the registers write the present state. This means that the input was saved and will not change the next state.

8X4 Mux:

Control	А	В	Output	
0	XXXX	xxxx	Α	
1	xxxx	xxxx	В	

Unit 1:

If Control is 0, addition.

If Control I 1, subtraction.

(Uses Full Adder)

Control	А	В	Output	
0	XXXX	xxxx	A + B	
1	xxxx	XXXX	A + (-B)	

Unit 2 And/Or:

А	В	Output
0	0	0
0	1	0
1	0	0
1	1	1
0	0	0
0	1	1
1	0	1
1	1	1
	0 1 1 0 0	0 0 1 1 1 0 1 0 0 0 0 1 1 1 0 0 0 1 1 1 0

Unit 3:

Control	Mode	Output		
0	0	Unit 1: Add		
0	1	Unit 1: Subtract		
1	0	Unit 2: And		
1	1	Unit 2: Or		

Full Adder:

Cin	А	В	S	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1