DENEY PROTOKOL KAĞIDI

Deney No	Deney Tarihi	Deney Adı
6	24.11.2023	Logic Gates and Basic Memory Circuits.

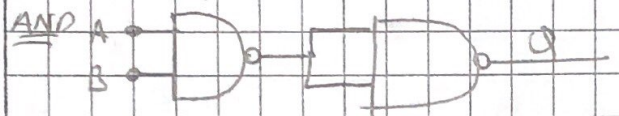
Grup No	Öğrenci No	Adı Soyadı
D-3	040190108	Berfin DUMAN
D-3	040190087	İsmail İlke Güngör
D-3	040190556	Utku Öney
D-3	040190090	Onur Kokel

Araş Gör Ve imzası	Hüsnü Anıl

6.1

NAND kapısı ile OR- AND- NOT gerçeklemesi

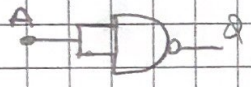
AND



2-input AND GATE

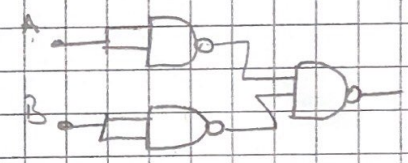
A	B	Q
0	0	0
0	1	0
1	0	0
1	1	1

NOT



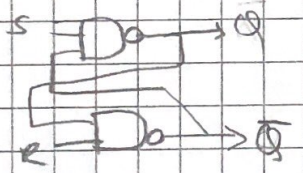
A	Q=Ā
0	1
1	0

OR GATE



A	B	Q
0	0	0
0	1	1
1	0	1
1	1	1

6.2 SR Latch

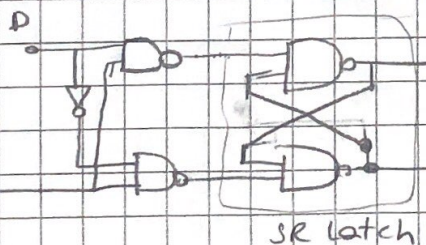


S	R	Q	Q̄
0	0	1	1
0	1	1	0
1	0	0	1
1	1	NC	NC

NC → No Change

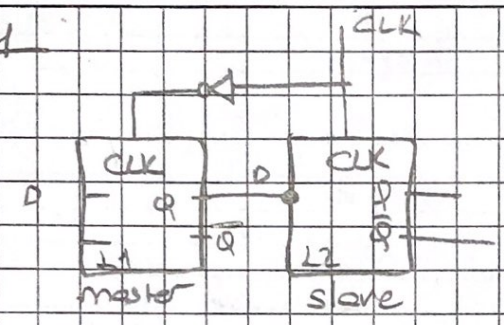
remain present state Hafıza

6.3



Clk	D	Q(t+1)	
0	x	Q(t)	Memory gibi çalışır
1	0	0	
1	1	1	

6.4



clk	D	Q	Q'	
1	1	1	0	
1	0	0	1	
0	1	Q	Q'	Durumunu korudu
0	0	Q	Q'	

D-latch ile aynı clk truth table

D flip flopun D-latch'ten farklı saatın yükseleş

kenarda tetiklenmesidir