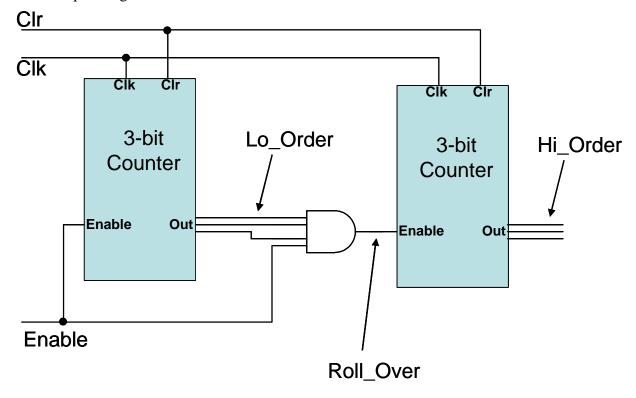
ECEn/CS 224

Cascaded Counter Homework Solutions

1. Create a 6-bit binary counter from two 3-bit counter modules. Assume that the 3-bit counter has the following inputs and outputs: **enable** (when enable=1 the counter increments, when enable = 0, the counter keeps its original value), **clr** (when clr = 1, the counter will reset to "000" on the next clock edge), **clk** (a positive edge triggered clock), and **out[2:0]** (the 3-bit output of the counter). Note that you will have to create your own "rollover" signal for the first 3-bit counter module. For this problem, draw a schematic of your counter and create a timing diagram of your counter that demonstrates the counter sequencing from the value "000000" to "001011".



► clk	0	
► clr	0	
► enable	1	
± lo_order	1	\(\O\)\(1\)\(2\)\(3\)\(4\)\(5\)\(6\)\(7\)\(0\)\(1\)\(2\)\(3\)\(4\)\(5\)
 hi_order	6	(X0X1
± • q	31	00 X01 X02 X03 X04 X05 X06 X07 X08 X09 X0A X0B X0C X0C
roll_over	0	

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