ECEn/CS 224
Chapter 13 Homework Solutions

13.1 If one desires to count to *M*, what is the minimum number of bits required in the resulting counter?

The maximum number, *M*, that can be represented by *K* bits is 2^K-1. In other words, a minimum of *K* bits are required, where *K* is the smallest integer such that 2^K-1 is greater than or equal to *M*. Solving for *K* gives us

$$K = \log_2(M+1)$$

However, this answer allows for fractions of bits. We must therefore limit our answer to the next highest integer (i.e., we take the ceiling). Thus we have,

$$K = \lceil \log_2(M+1) \rceil$$

13.2 Design a 3-bit counter that counts in multiples of 3. That is, the count sequence is: 000 – 011 – 110 – 000 – ⋯. Use D flip flops.

Q_2	Q_1	Q_0	N_2	N_1	N_0
0	0	0	0	1	1
0	0	1	X	X	X
0	1	0	X	X	X
0	1	1	1	1	0
1	0	0	X	X	X
1	0	1	X	X	X
1	1	0	0	0	0
1	1	1	X	X	X

N_2	Q_2 = 0	Q_2 = 1
Q_1Q_0 = 00	0	X
Q_1Q_0 = 01	X	X
Q_1Q_0 = 11	1	X
Q_1Q_0 = 10	X	0

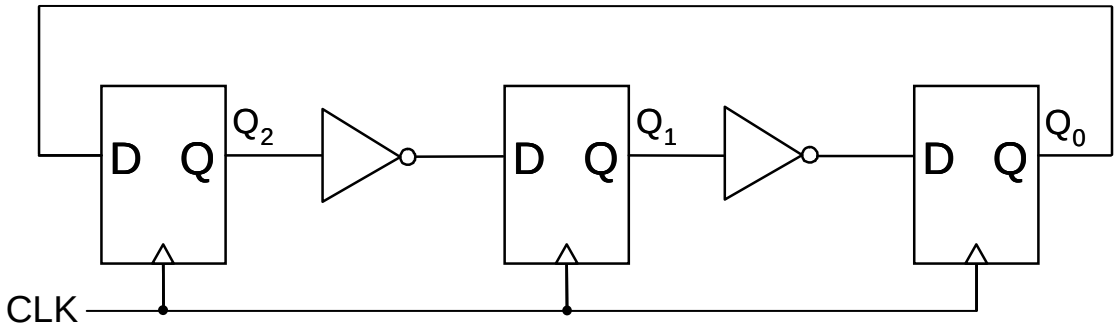
$N_2 = Q_0$

N_1	Q_2 = 0	Q_2 = 1
Q_1Q_0 = 00	1	X
Q_1Q_0 = 01	X	X
Q_1Q_0 = 11	1	X
Q_1Q_0 = 10	X	0

$N_1 = Q_2'$

N_0	Q_2 = 0	Q_2 = 1
Q_1Q_0 = 00	1	X
Q_1Q_0 = 01	X	X
Q_1Q_0 = 11	0	X
Q_1Q_0 = 10	X	0

$N_0 = Q_1'$


D
Q
Q_2
D
Q
Q_1
D
Q
Q_0
CLK

13.3. Repeat Problem 13.1 but use T flip flops.

Q_2	Q_1	Q_0	N_2	N_1	N_0	T_2	T_1	T_0
0	0	0	0	1	1	0	1	1
0	0	1	X	X	X	X	X	X
0	1	0	X	X	X	X	X	X
0	1	1	1	1	0	1	0	1
1	0	0	X	X	X	X	X	X
1	0	1	X	X	X	X	X	X
1	1	0	0	0	0	1	1	0
1	1	1	X	X	X	X	X	X

T_2	Q_2 = 0	Q_2 = 1
Q_1Q_0 = 00	0	X
Q_1Q_0 = 01	X	X
Q_1Q_0 = 11	1	X
Q_1Q_0 = 10	X	1

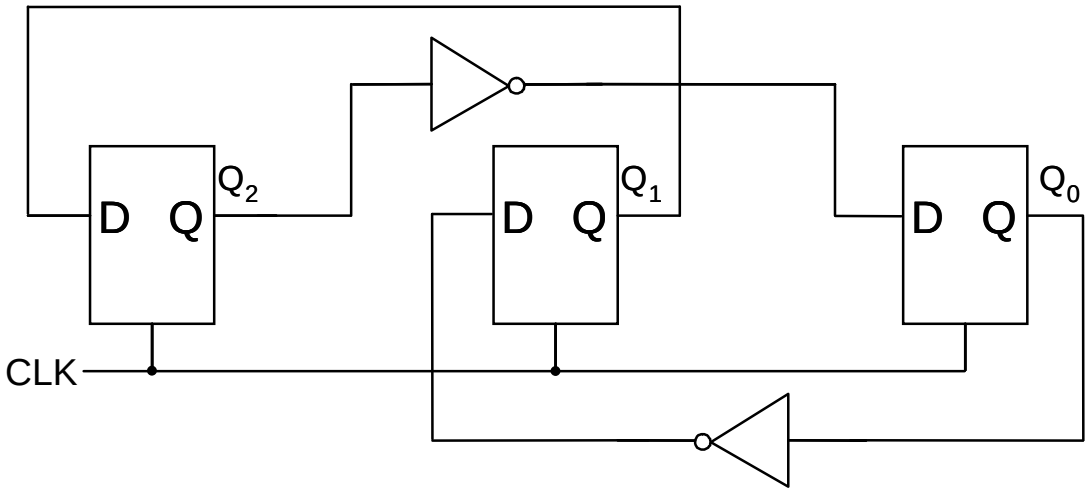
$N_2 = Q_1$

T_1	Q_2 = 0	Q_2 = 1
Q_1Q_0 = 00	1	X
Q_1Q_0 = 01	X	X
Q_1Q_0 = 11	0	X
Q_1Q_0 = 10	X	1

$N_1 = Q_0'$

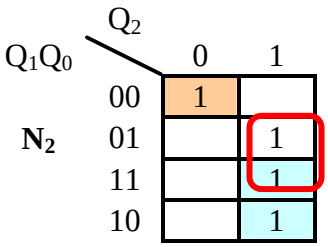
T_0	Q_2 = 0	Q_2 = 1
Q_1Q_0 = 00	1	X
Q_1Q_0 = 01	X	X
Q_1Q_0 = 11	1	X
Q_1Q_0 = 10	X	0

$N_0 = Q_2'$

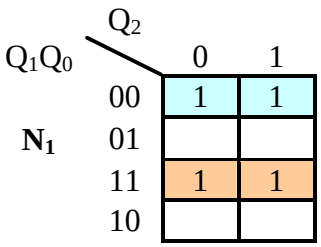


13.5. Design a 3-bit binary counter which counts down rather than up. Use D flip flops.

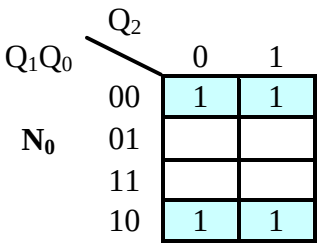
Q_2	Q_1	Q_0	N_2	N_1	N_0
0	0	0	1	1	1
0	0	1	0	0	0
0	1	0	0	0	1
0	1	1	0	1	0
1	0	0	0	1	1
1	0	1	1	0	0
1	1	0	1	0	1
1	1	1	1	1	0



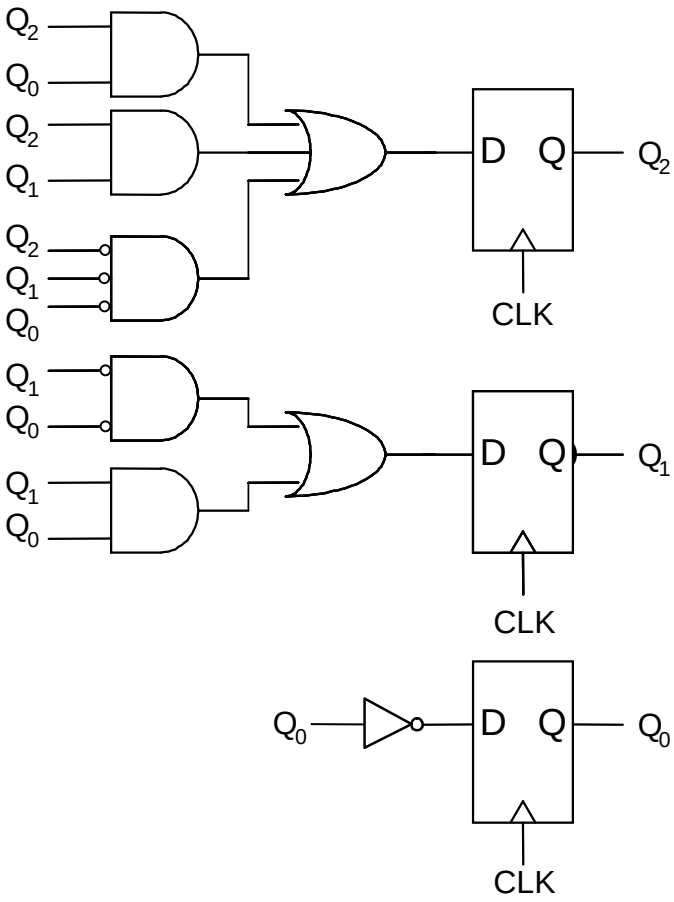
$N_2 = Q_2Q_0+Q_2Q_1+Q_2'Q_1'Q_0'$



$N_1 = Q_1'Q_0'+Q_1Q_0$



$N_0 = Q_0'$



13.7 Determine the minimum clock period for the counter of Figure 13.11. Use the following delays: t_{NOT} = 1 ns, t_{AND} = 2 ns, t_{OR} = 3 ns, $t_{CLK \rightarrow Q}$ = 2 ns, t_{setup} = 3 ns, t_{hold} = 1 ns. Note that the flip flops are shown without a *Q'* output. Thus, you *must* use inverters as a part of the input forming logic as necessary.

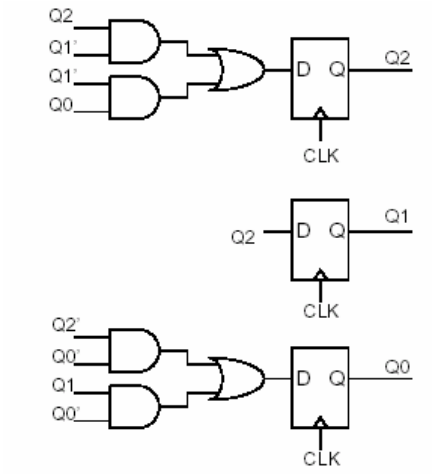


Figure 13.11

In general, the minimum clock period is the sum of the Clock-to-Q time, the time for the longest path of the input forming logic, and the setup time of the flip flop. In this case, there are several equally long paths. The longest paths consist of an inverter, an AND gate, and an OR gate.

Longest path =	Inverter	1 ns
	AND	2 ns
	OR	3 ns
	Setup	3 ns
	Clk→Q	2 ns
		------
		11 ns

Minimum Period = 11 ns, or 11 x 10^{-9} s

Maximum Frequency = 1/Period = 1/(11 x 10^{9} s) = 90.9 MHz, or 90.9 x 10^{6} s