ECEn/CS 224
Register File Homework Solutions

1. Write the logic equation which describes the data out after the next clock cycle. It should be in the form

   $Dout^+$ = (logic equation here)

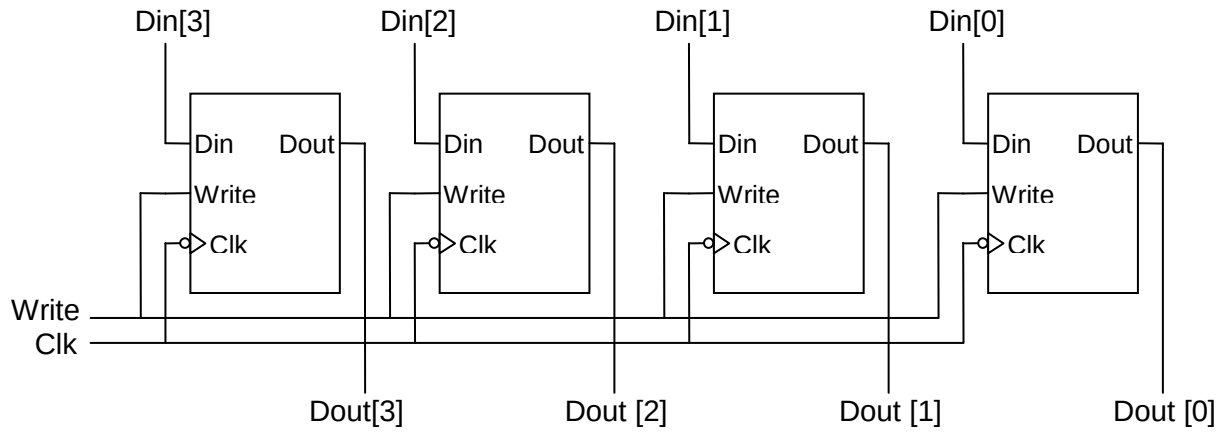
   and should use Dout, DataIn, and Write as literals in the equation.

Write	Din	Dout	$Dout^+$
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

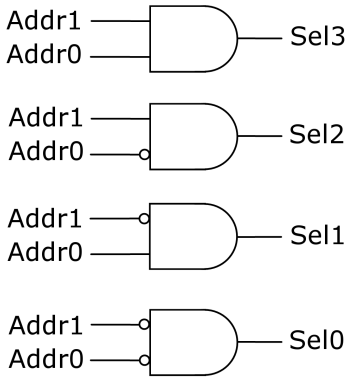
Write \ Din, Dout	00	01	11	10
0	0	1	1	0
1	0	0	1	1

$Dout^+$ = (DataIn • Write) + (Dout • Write')

2. Using the symbol for the 1-bit register, design a 4-bit register. Note that within a register word, all bits are clocked and written by the same Clk and Write signals.

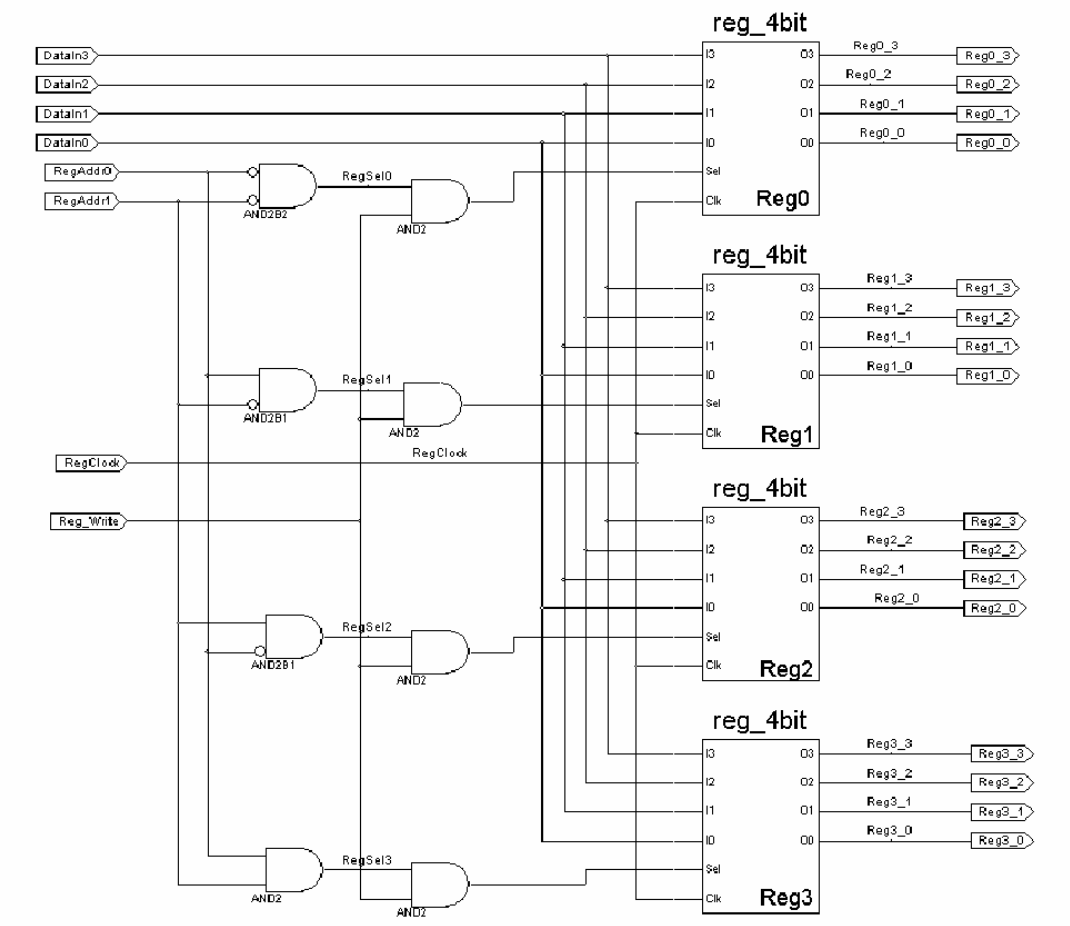


3. Design a 2:4 decoder using logic gates.

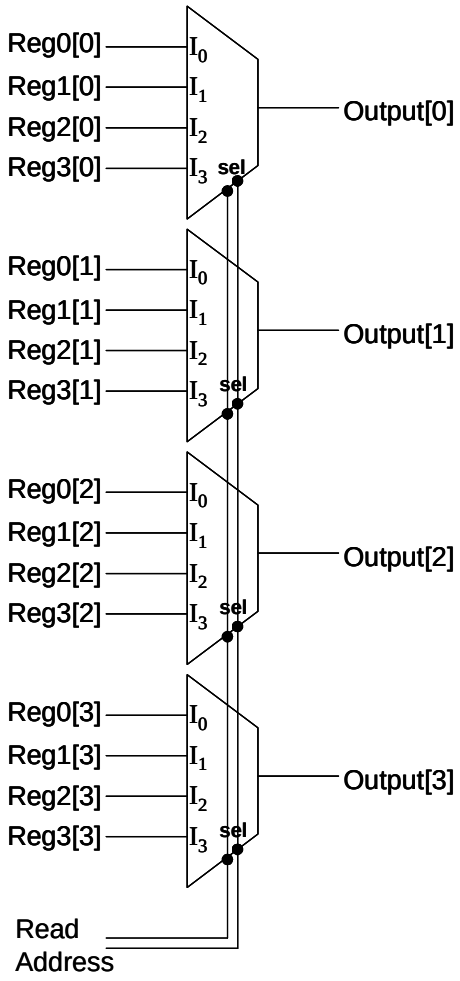


4. Design a 4-bit word by 4-word register file (4 registers of 4 bits each). You will use the 4-bit register symbols and the 2:4 decoder for register selection. The address inputs to the decoder will be the write address bits for your register file.

The schematic is shown below. Notice that the inside of the decoder (the 4 AND gates on the left) are shown rather than a 2:4 decoder block. Also, this example deviates somewhat from the naming conventions used in the previous examples.



5. Now design the circuit that will accomplish the read. It needs to use the read address bits (register select address bits) to choose which group of 4 bits from the register file output should be selected as the DataOut signals. In essence what you need to design is a 4-bit, 4:1 multiplexer which selects among 4 groups of 4-bit data inputs. Pay close attention to the address bits and which data bits they are selecting. As you might guess, you should build this out of a collection of 4:1 multiplexers.



6. Draw a block diagram to show how all the pieces fit together to make a complete, dual-ported 4x4 register file.