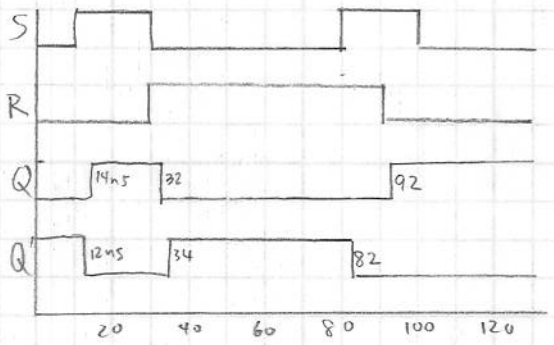
ECEn 220 HW7

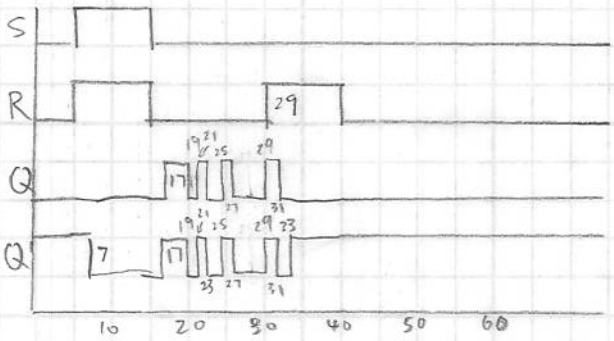
11 #2,3,5,7,12,14,15
12 #1,2,3,4

Benjamin Bergeson

11.2



11.3

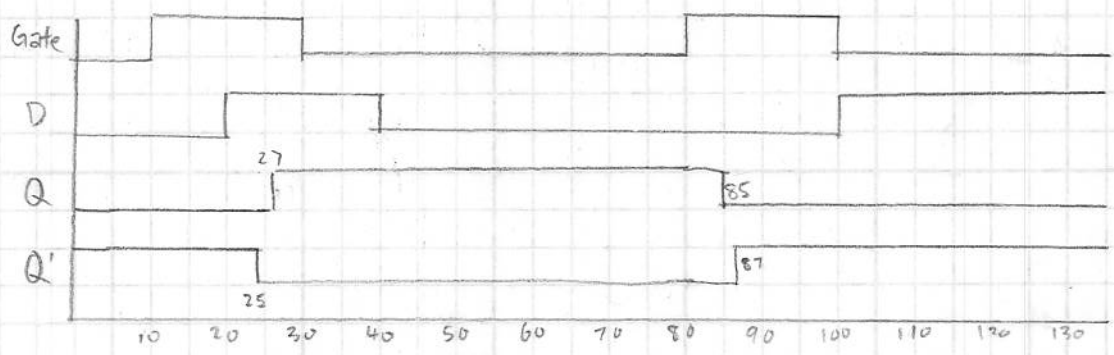


11.5

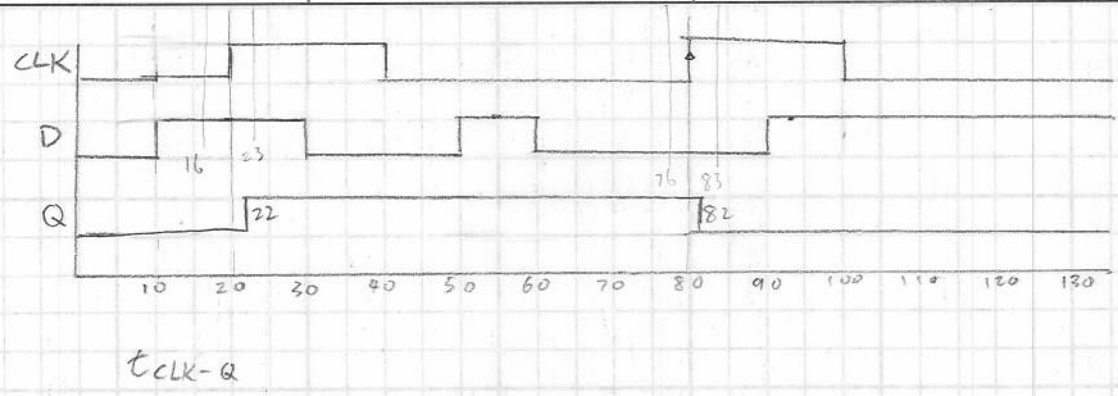
S	R	Q	Q'	Q+	Q'+	
0	0	0	0	1	1	useless
0	0	0	1	1	1	
0	0	1	0	1	1	
0	0	1	1	1	1	
0	1	0	0	1	1	
0	1	0	1	1	1	
0	1	1	0	1	0	stable
0	1	1	1	1	0	set
1	0	0	0	1	1	
1	0	0	1	0	1	stable
1	0	1	0	1	1	
1	0	1	1	0	1	reset
1	1	0	0	1	1	
1	1	0	1	0	1	stable
1	1	1	0	1	0	stable
1	1	1	1	0	0	

when S goes low, the latch is set.
when R goes low, the latch is reset.

11.7

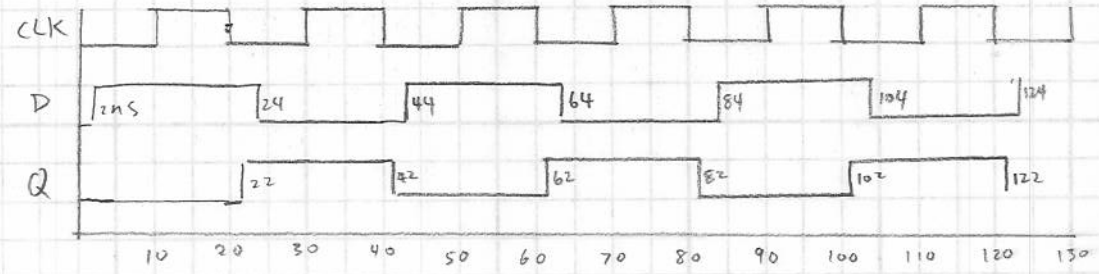


11.12



t_{CLK-Q}

11.14



11.15 (a) When there are false outputs on the logic generating the asynchronous control signals, the control signals will be loaded without waiting for the clock signal to load the latches.

(b) There would be an additional setup time for the asynchronous signal. If it were to change too soon before the clock edge, the latch would have to wait additional time before it can process more information.