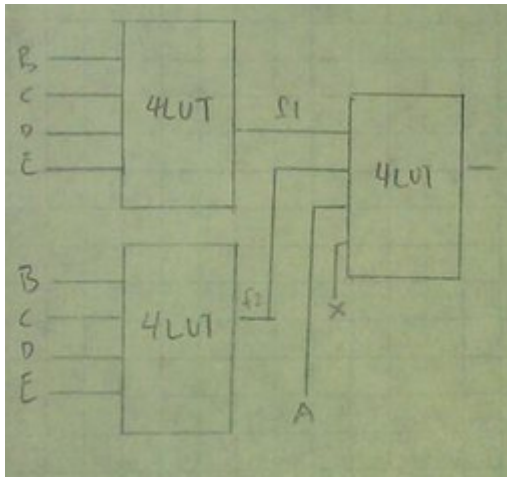
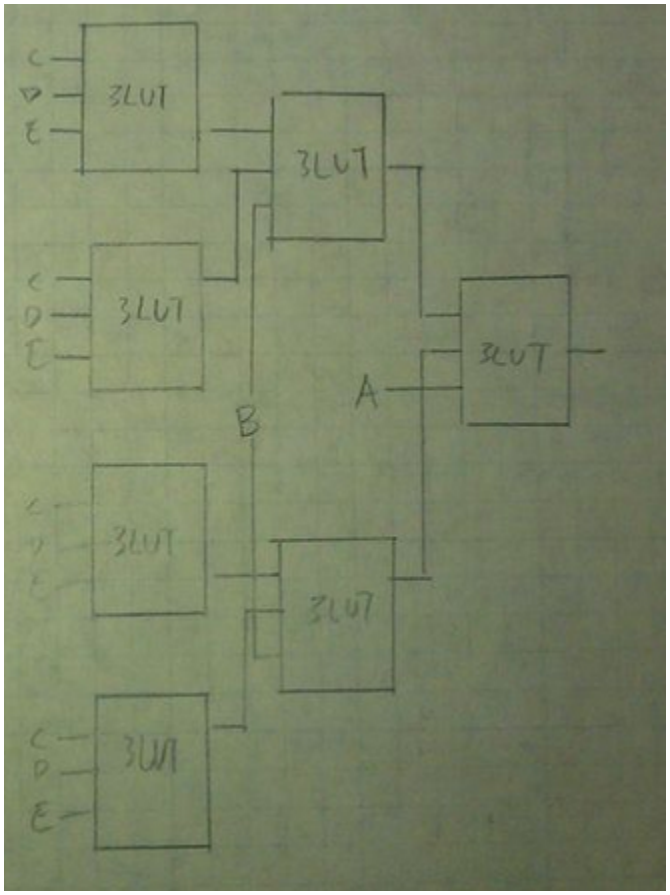
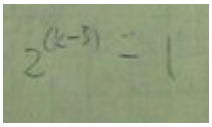
Benjamin Bergeson
ECEn 220 HW 13

19.1





19.2

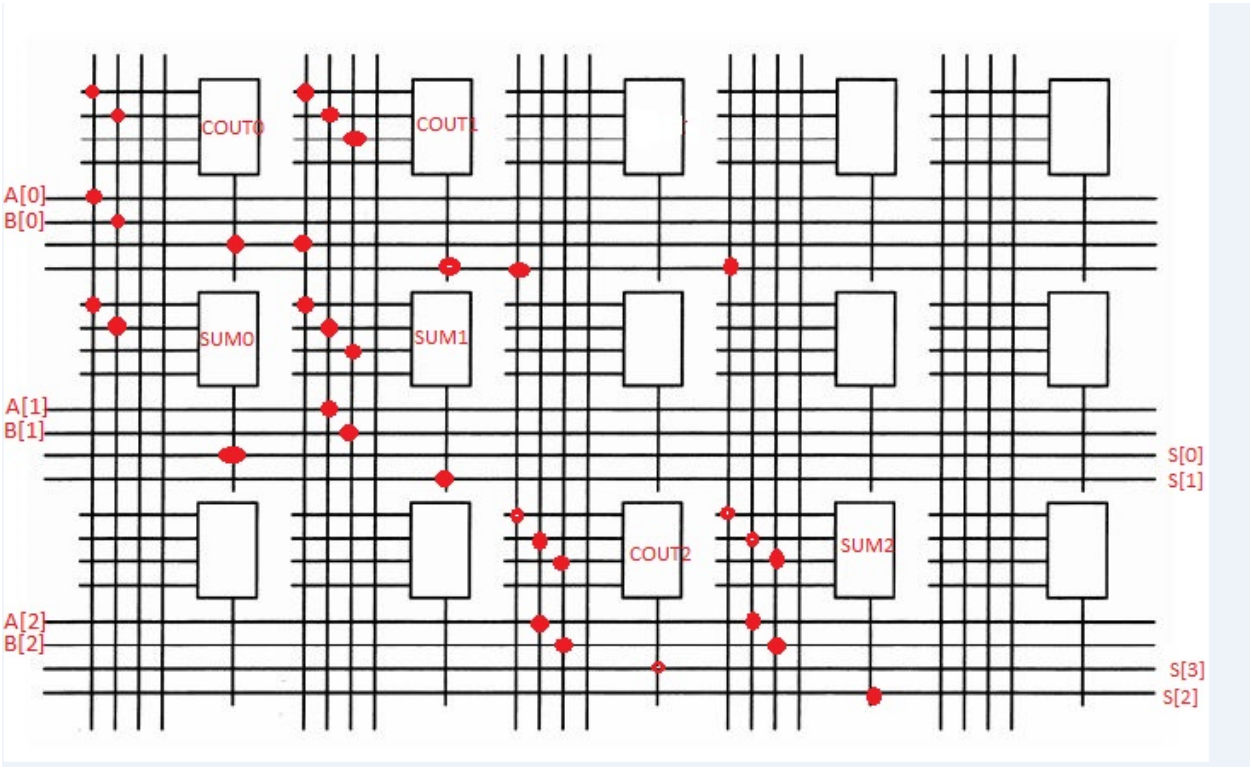


19.3

63 4LUTs needed

The first 32 would store functions. The outputs of those functions would go into 16 4LUTs acting as MUXs. The output of these 16 LUTs would then go into 8 LUTs acting as MUX. This pattern goes on. With each level only having half the LUTs of the previous level.

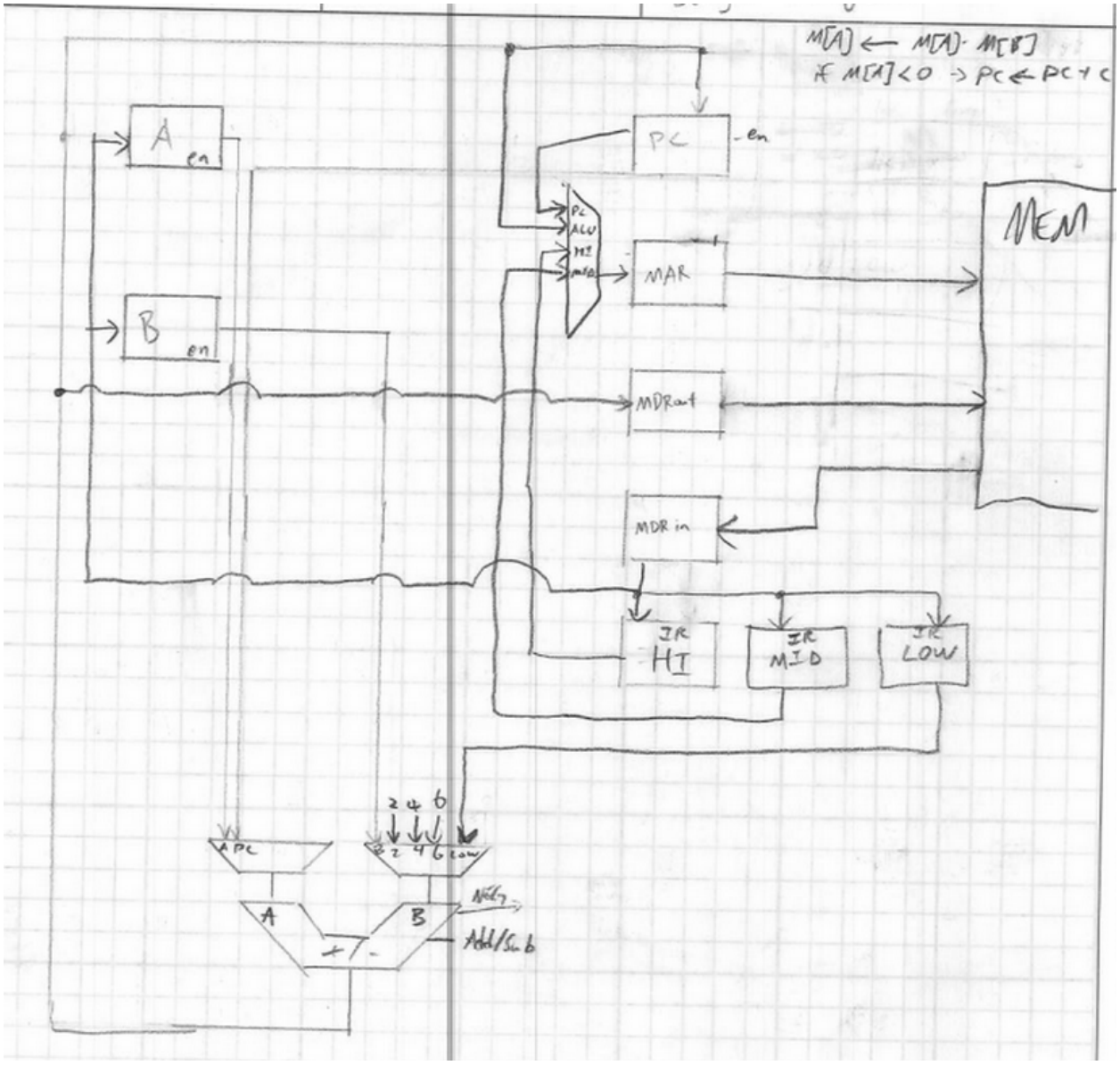
19.5



M1

Instruction Set Architecture = Instructions + Registers + How memory is accessed

M2


M[A] ← M[A] - M[B]
if M[A] < 0 -> PC ← PC + C
A
en
B
en
PC
en
PC
ALU
MI
MDR
MAR
MEM
MDRout
MDR in
IR HI
IR MID
IR LOW
2 4 6
PC
A
B
+
-
Add/Sub

ECEn 220 HW13 Pt.3

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