# ECEn/CS 224
# Chapter 11 Homework Solutions

11.1 Below is a timing diagram for the SR latch of Figure 11.1. Fill in the output waveform. Reflect approximate timing. See section 11.7 to remind you what is meant by *approximate timing*.

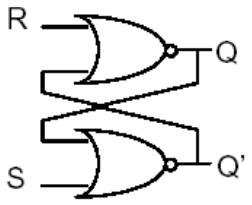
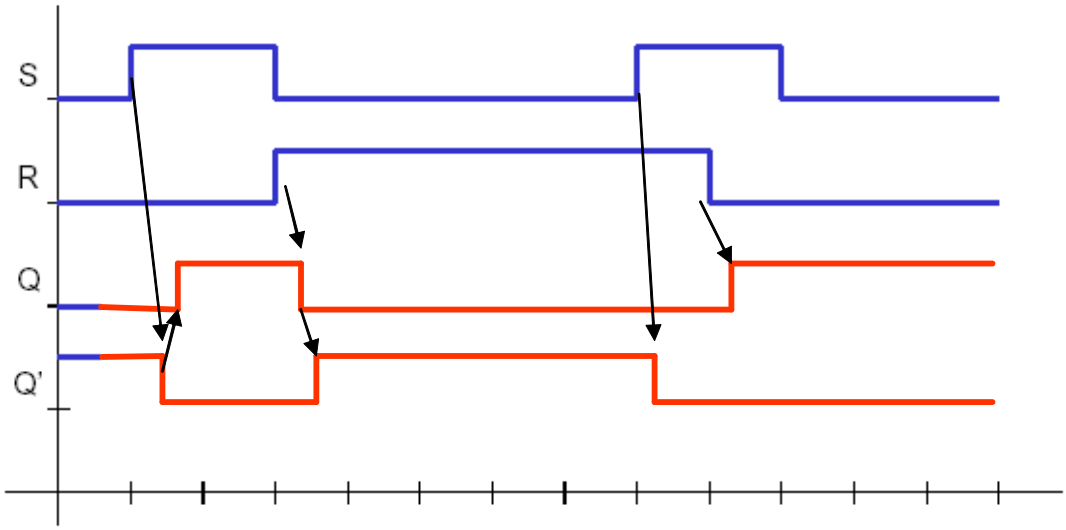
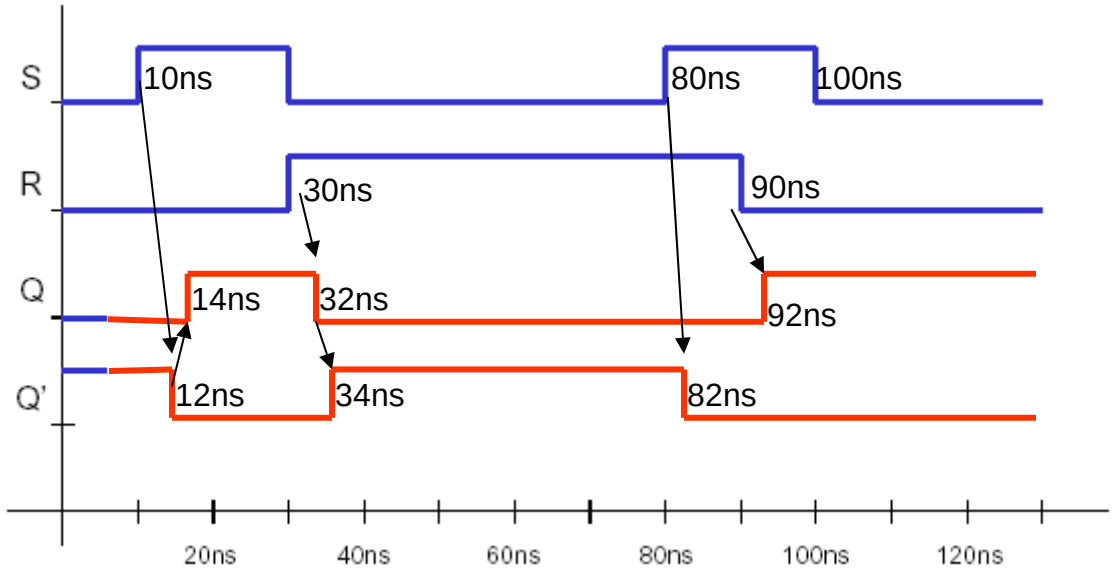


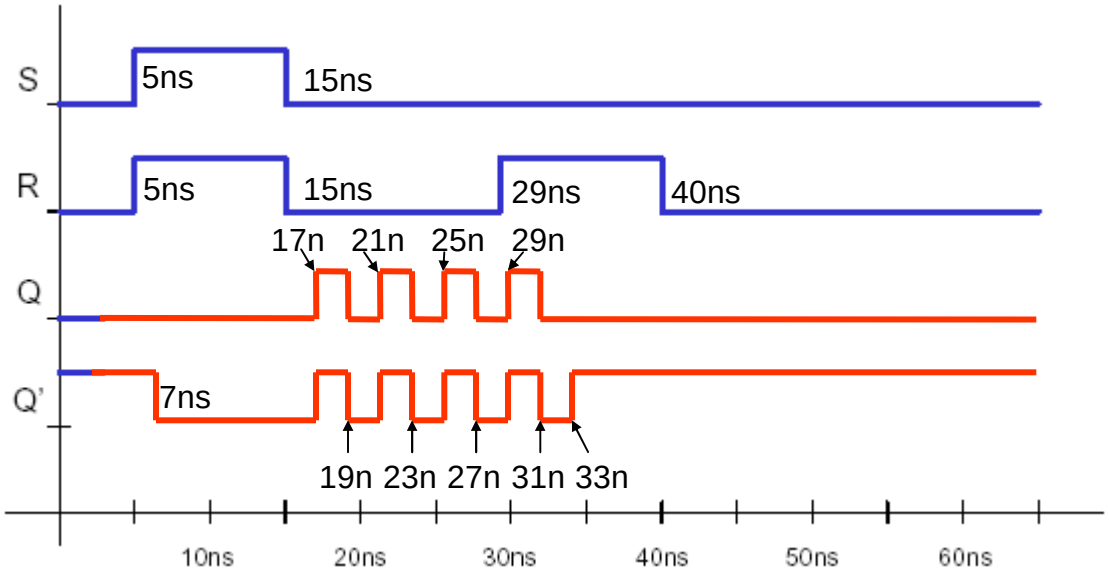

**Figure 11.1: SR Latch**



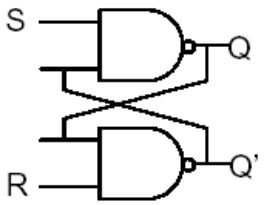
11.2 Repeat Problem 11.1 but with detailed timing. You may simply label each output signal transition in the timing diagram with the time it occurs. Delays of the various gates include: $t_{NOT} = 1ns$, $t_{AND} = 3ns$, $t_{NOR} = 2ns$.




11.3 Complete the timing diagram below for an SR latch. In this case, the circuit oscillates. Use $t_{NOR} = 2ns$ and accurately reflect the *Q* and *Q'* waveforms in the drawing (complete with timing).



11.5 Shown in the figure below is a storage circuit made from NAND gates instead of NOR gates. Experiment with values on the *S* and *R* inputs to determine how it works. Hint: start with *S*=*R*='1'. Write a transition table to summarize what you find.




| S | R | Q | Q+ |
|---|---|---|---|
| 0 | 0 | 0 | NA (1) |
| 0 | 0 | 1 | NA (1) |
| 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 |

Notice the similarity to the NOR latch.

11.6 Below is a timing diagram for the circuit of Figure 11.7. Fill in the output waveform. Reflect approximate timing.

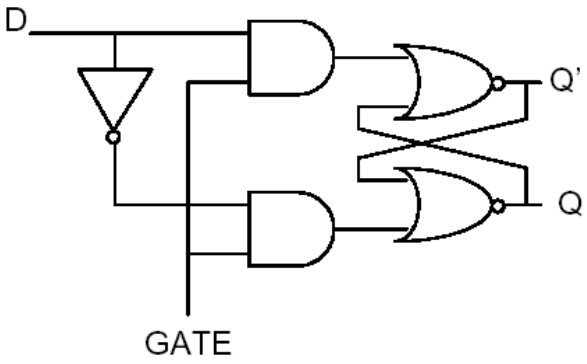
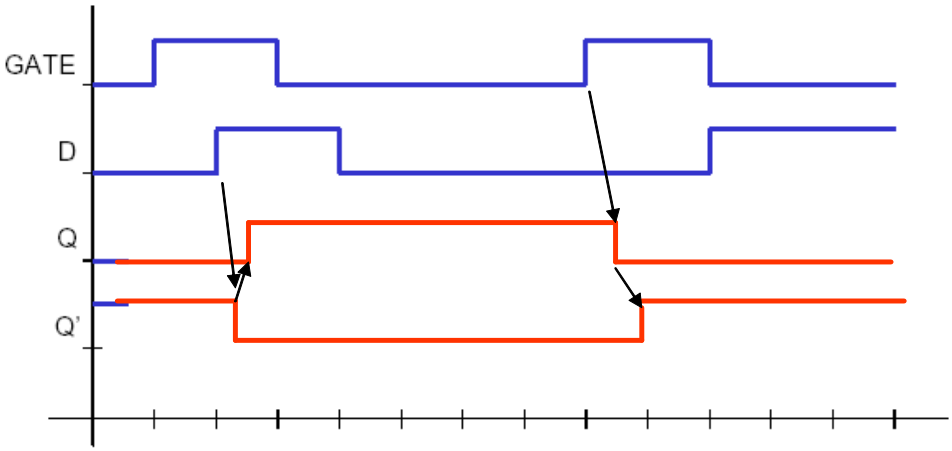
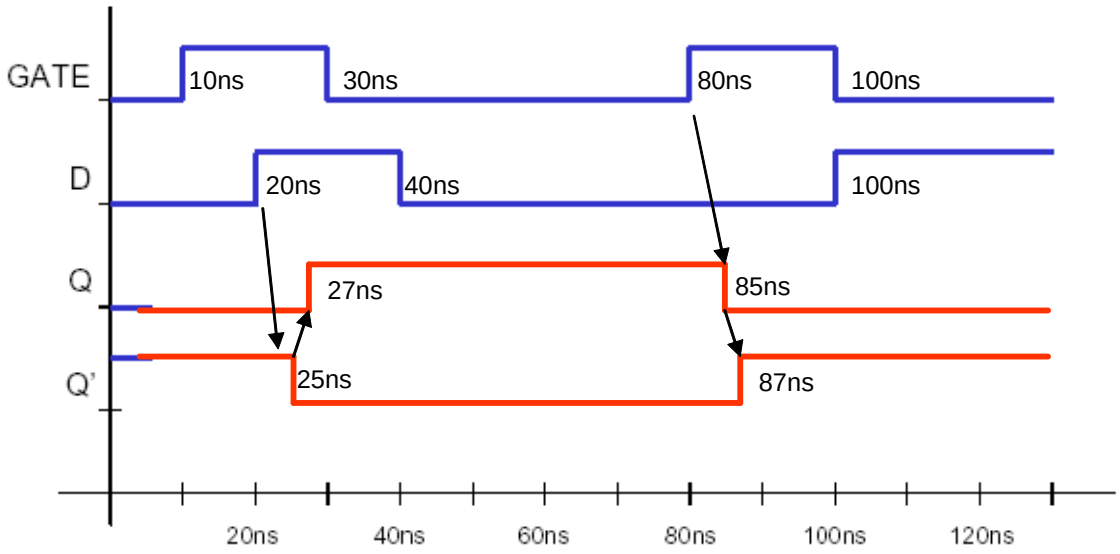



**Figure 11.7: Gated D Latch**



11.7 Repeat Problem 11.6 but with detailed timing. Use the following delays: $t_{NOT} = 1ns$, $t_{AND} = 3ns$, $t_{NOR} = 2ns$.




11.11 Below is a timing diagram for the circuit of Figure 11.18. Fill in the output waveform. Reflect approximate timing.

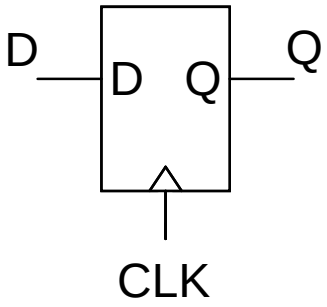
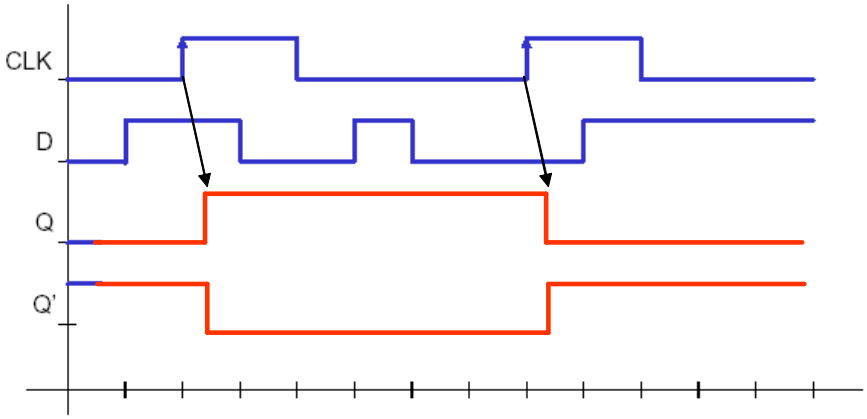


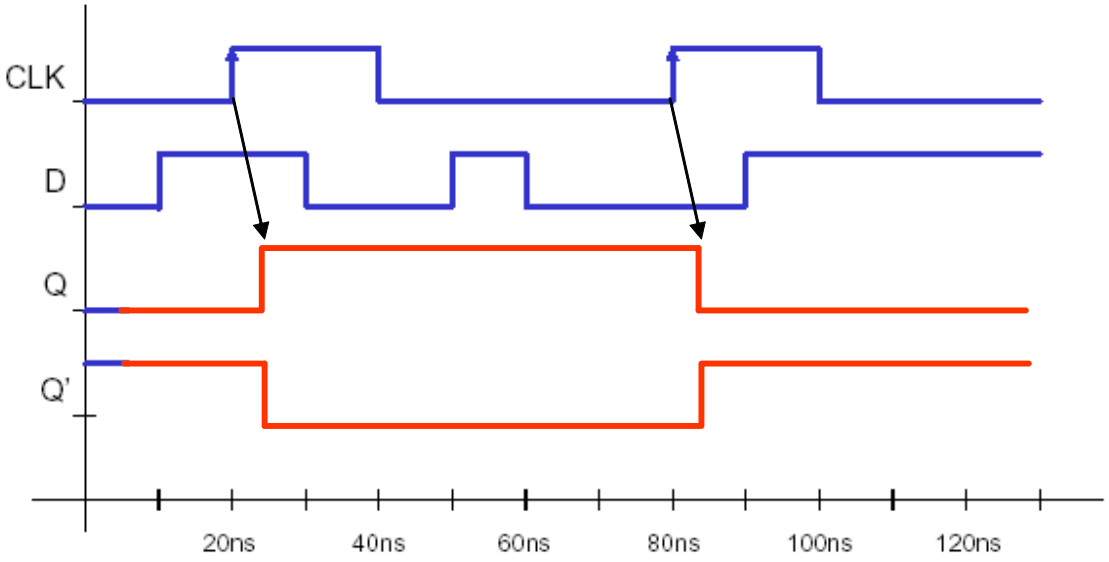

**Figure 11.18 Rising Edge Triggered Master/Slave D Flip Flop**



22ns 82ns

22ns 82ns

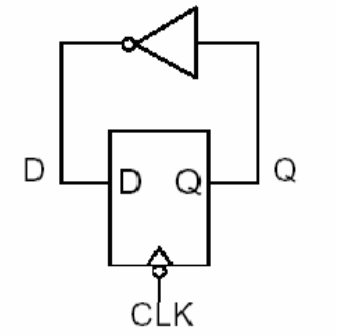
11.12 Repeat Problem 11.11 but with detailed timing. For your delays use the following: $t_{CLK\text{-}Q} = 2ns$, $t_{setup} = 4ns$, $t_{hold} = 3ns$. Which of these delays is actually needed in order to complete the timing diagram?

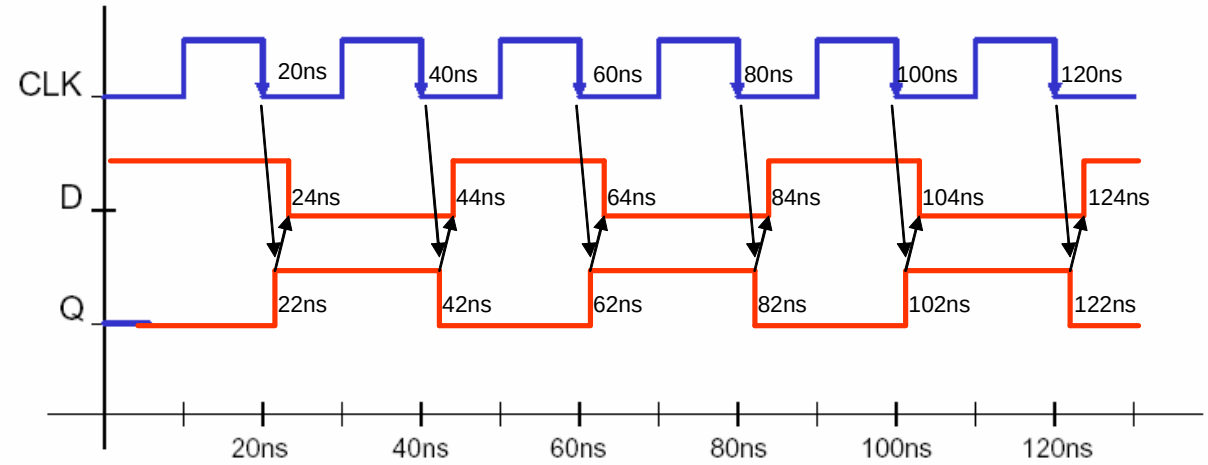



When only $t_{CLK\text{-}Q}$ is given, it should be treated as a worst case delay from the clock edge to either Q or Q'. Therefore, in the timing diagram, there isn't a difference between when Q changes and Q' changes.

For this example, only $t_{CLK\text{-}Q}$ is required to complete the timing diagram.

11.14 Below is a toggle circuit along with a timing diagram. Complete the associated timing diagram complete with detailed timing. Use the delays from Problem 11.12. Also, use $t_{NOT} = 2ns$.



11.15 Discuss the problems associated with using flip flops with asynchronous clear or preset signals. In particular, address the following: (a) false outputs on the logic generating the asynchronous control signals and (b) timing issues associated with the asynchronous control signals.

a) Because asynchronous signals are constantly monitored by the flip-flop, any false output or glitch may cause the flip flop to be cleared or set. Because of this, the logic generating these asynchronous signals must be hazard free.

b) First, there will be a minimum pulse width on the asynchronous signals similar to $t_{setup}$. This minimum is required to ensure that the flip flop is completely set or cleared by the input. Otherwise, correct clear/preset behavior may not be guaranteed.

Second, an asynchronous input to a flip flop must not be released too close to the asserting clock edge (i.e., it should not be released during the $t_{setup}$ period). Otherwise some of the flip flops may take on their cleared/preset values and others may take on the value on their inputs. These asynchronous signals should only be released after the clock edge and before the next $t_{setup}$ period to ensure that all of the flip flops in the circuit come out of reset correctly in the same clock cycle.