**Cs303 Lab-6 Term Project**

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**Introduction**

In this laboratory assignment, we were expected to modify the given template codes to work as a down counter with binary-to-seven segment display. To achieve this working state, we were asked to implement a controller to determine the states and next state transitions.

**Verilog codes**

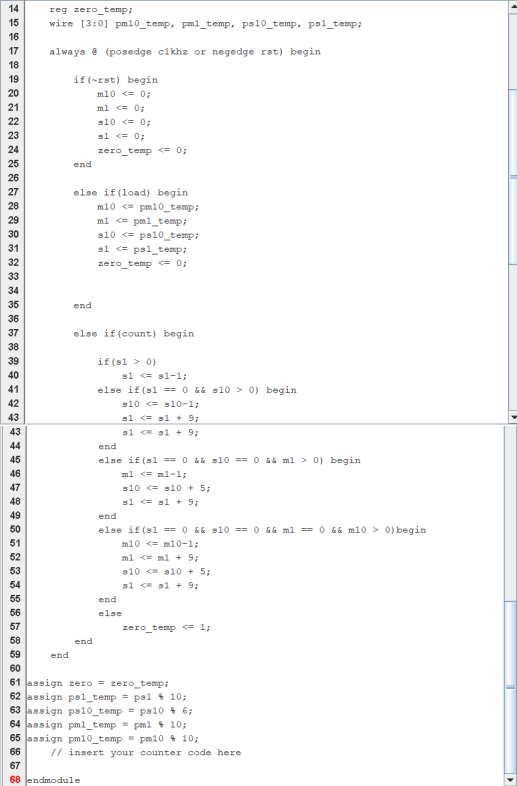
The Verilog code of our controller is as below :

**Graphical user interface, text, application

Description automatically generated**

**Graphical user interface, application, table

Description automatically generated**

After I have written the controller, I shifted my attention to editing the down counter to make it count my clock down by 1 seconds for every clock (measured by the counter code given to me, making every tick 1 seconds) tick.****

**Results**

Results can be seen at the .dig file that I have submitted at the zip file, everything is working as they should.