

LECTURE 21

APRIL 7

→ ROUTER CYCLE is NP-complete
(HAMILTON)

→ CIRCUIT SAT is NP-complete
(Mother of all NP-completeness results)

Every problem
in NP \leq_p Circuit Sat

→ CIRCUIT SAT \leq_p 3SAT

RUDRATA CYCLE (directed)

INPUT: A directed graph $G = (V, E)$

SOLUTION: A cycle passing through all nodes exactly once

RUDRATA CYCLE $\in NP$

GOAL: RUDRATA CYCLE is NP-complete

: Thm: $3SAT \leq_P RUDRATA CYCLE$

3SAT \leq_P RUDRATA CYCLE

3SAT instance: Φ

$(x \vee y \vee z) \wedge$
 $(\bar{y} \vee z \vee w) \wedge$
 $(\bar{x} \vee y \vee \bar{w}) : -$

Reduction

Algorithm

RUDRATA CYCLE G

Input: Directed Graph $G=(V, E)$

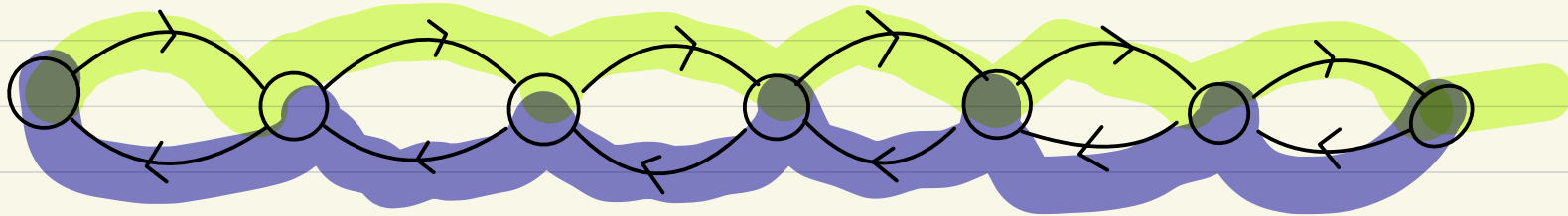
\exists a satisfying assignment to $\Phi \implies \exists$ a Rudrata Cycle in G

\exists a Rudrata cycle in $G \implies \exists$ a satisfying assignment in Φ

3SAT \rightarrow RUDRATA CYCLE

$$x \in \{0, 1\}$$

$x = 0 \Leftrightarrow$ Right to left
 $x = 1 \Leftrightarrow$ left to right



x

(Traverse the graph without skipping / repeating any vertex)

3SAT \rightarrow RUDRATA CYCLE

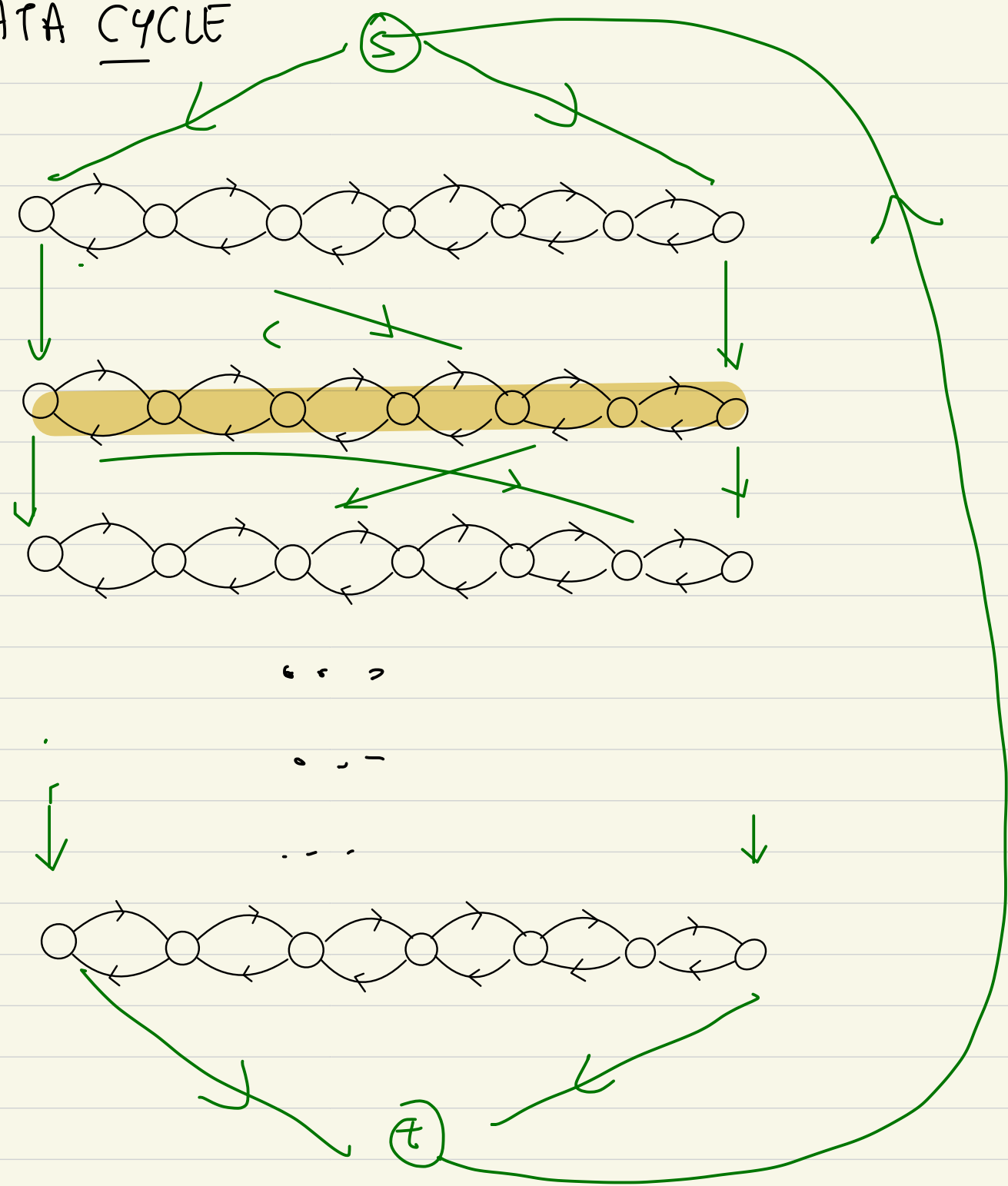
x_1

x_2

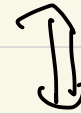
x_n

Every boolean
assignment

\Updownarrow
Rudrata Cycle



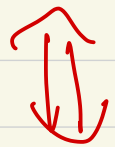
$$C = (x \vee \bar{y} \vee z)$$



$x \leftarrow L \text{ to } R$
OR

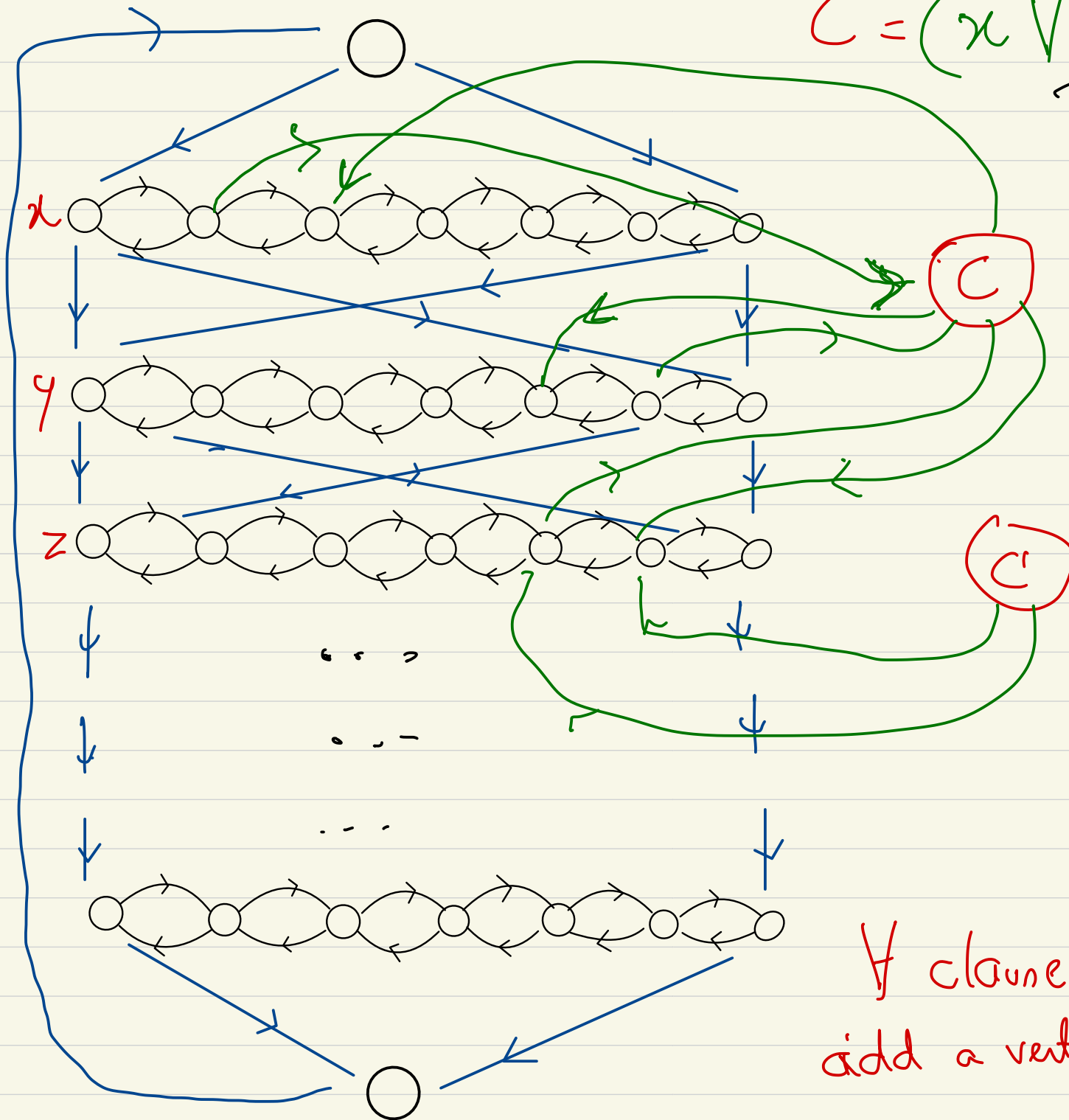
$y \leftarrow R \text{ to } L$
or

$z \leftarrow L \text{ to } R$



Cycle covers
 C

If clause in 3SAT
add a vertex, and connect
it as shown
above

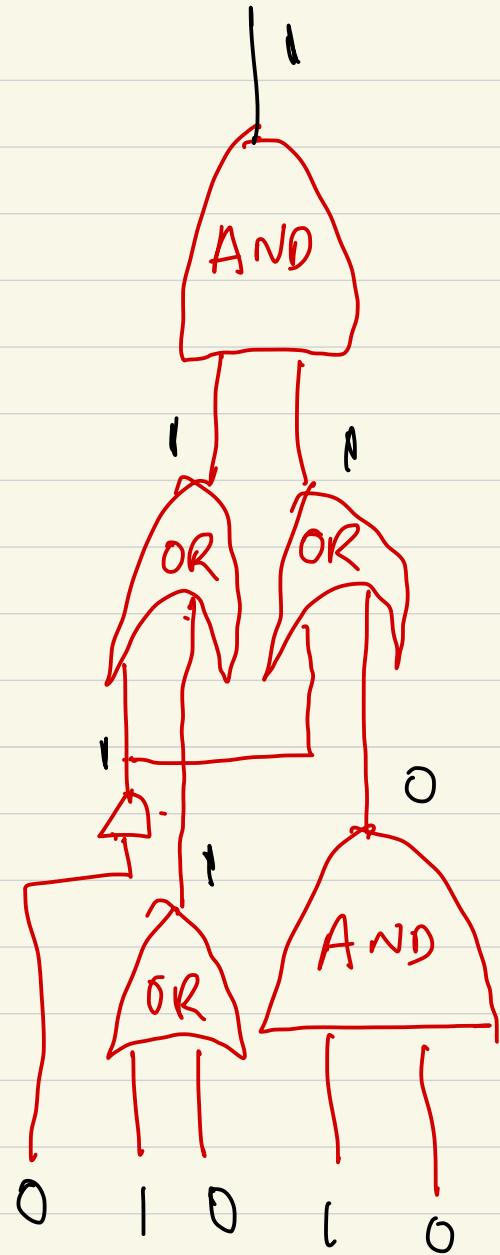


CIRCUIT SAT

INPUT: 1) Circuit with AND/OR/NOT gates
2) n inputs

SOLUTION: An boolean assignment
so that output = 1.

Circuit SAT \in NP



Circuit SAT is NP-complete:

Every problem
in NP

\leq_p

Circuit SAT

Example: Factorization \leq_p

FACTORIZATION

INPUT: An n bit number N

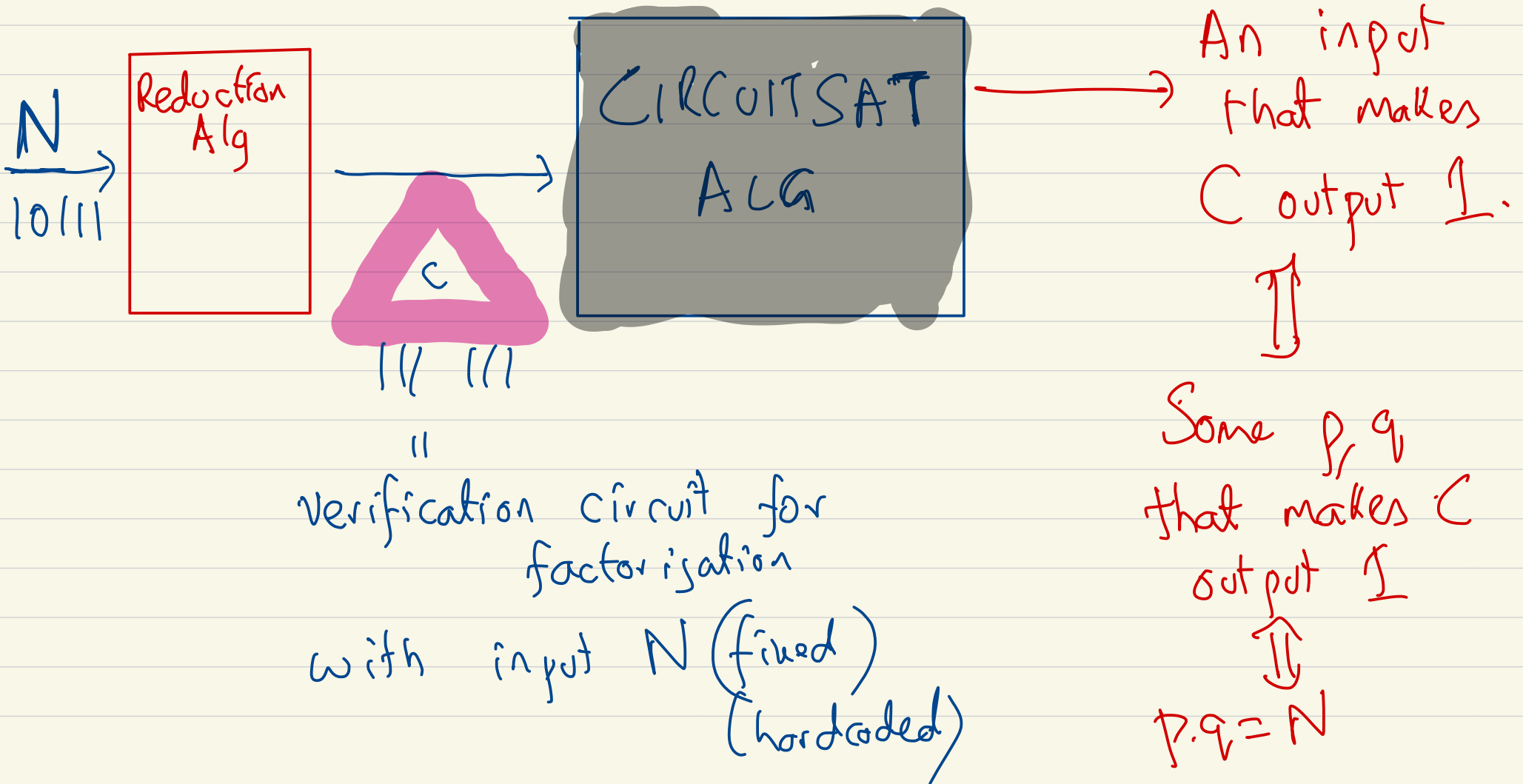
SOL: p, q $p, q > 1$
and $p \cdot q = N$



CIRCUIT SAT

INPUT: Circuit C

SOL: x s.t. $C(x) = 1$

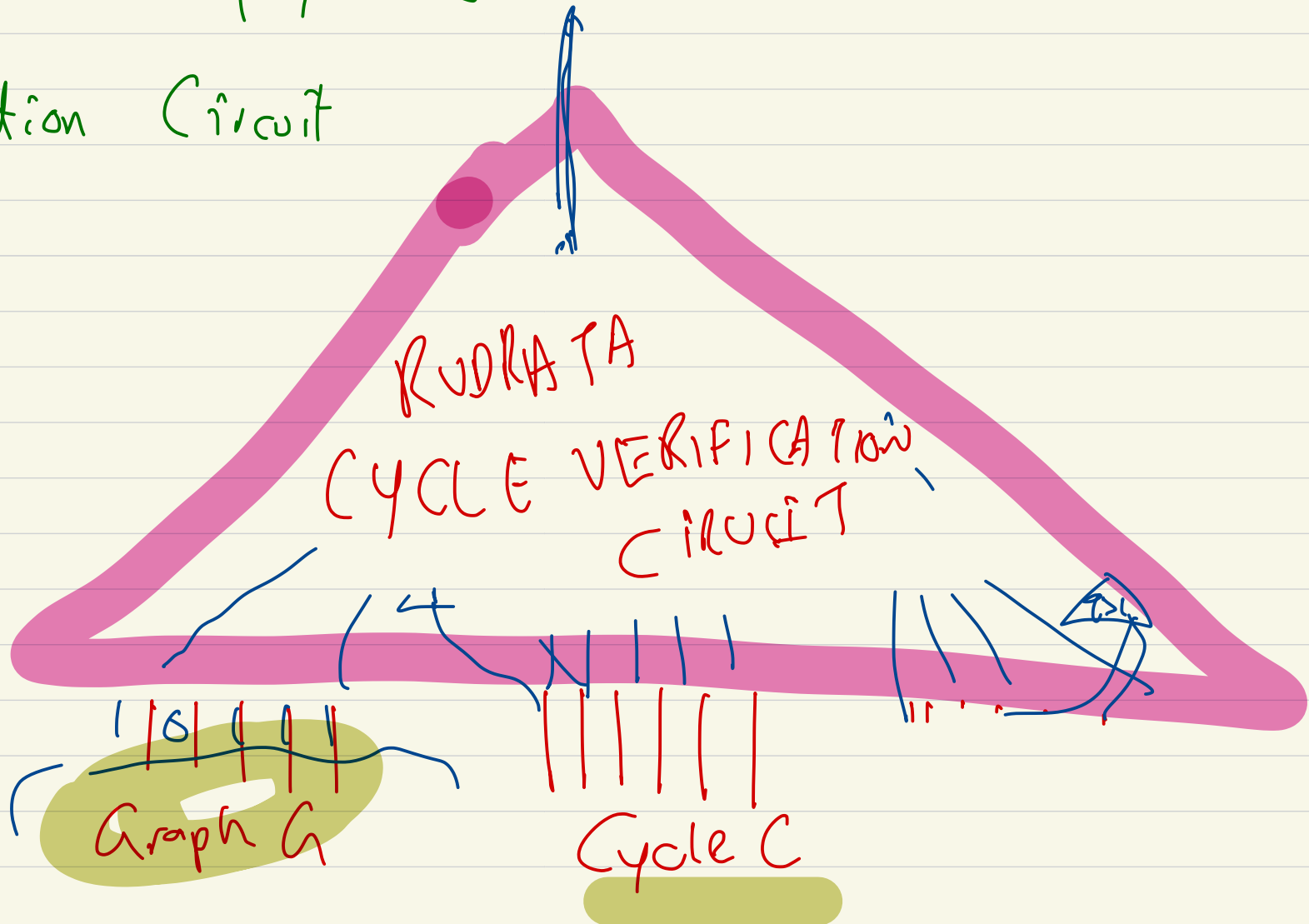


\exists a verification algorithm for Factorization n



polytime Circuit

Verification Circuit



Same proof applies to every problem in NP

\Rightarrow Every problem in NP \leq_p Circuit SAT.

\Rightarrow Circuit SAT is NP-complete.

CIRCUIT SAT

INPUT: A circuit C

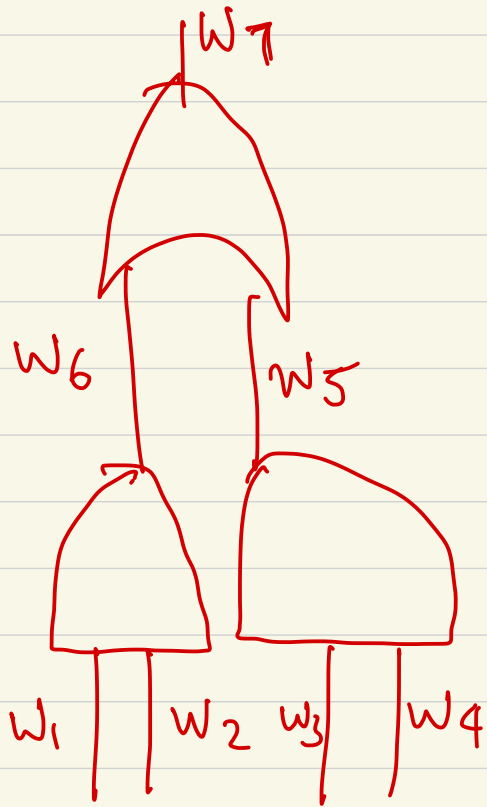
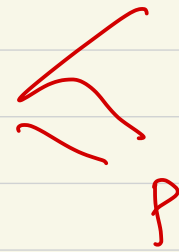
SOL: An assignment x , s.t.
 $C(x) = 1$

3SAT

INPUT: A 3SAT formula

$(x_1 \vee y_1 \vee z_1) \wedge (\neg x_1 \vee \neg y_1 \vee z_2) \dots$

SOL: A satisfying assignment



1) \forall each wire w_i , introduce
a variable in 3SAT

$\{w_1, \dots, w_7\}$

2) \forall each gate introduce clauses

Example: we want

$$w_6 = w_1 \wedge w_2$$



Simulate this using clauses

Obs: Every constraint on 3-variables can be simulated
via clauses of form $(x \vee y \vee z) \dots$

Example: Suppose we want a constraint
 $x = y \wedge z$,

Then $x = y \wedge z$

$$\left\{ \begin{array}{l} (x \vee \bar{y} \vee \bar{z}) \\ (\bar{x} \vee y \vee \bar{z}) \\ (\bar{x} \vee \bar{y} \vee z) \\ (\bar{x} \vee y \vee z) \end{array} \right\}$$

↑
4 clauses simulate $x = y \wedge z$.

To express a constraint using 3SAT clauses

Example: $x = y \wedge z$



Forbidden assignments

0	1	1	→	$(x \vee \bar{y} \vee \bar{z})$
1	0	1	→	$(\bar{x} \vee y \vee \bar{z})$
1	1	0	→	$(\bar{x} \vee \bar{y} \vee z)$
1	0	0	→	$(\bar{x} \vee y \vee z)$