T.C.
PÎRÎ REİS UNIVERSITY
FACULTY OF ENGINEERING
DEPARTMENT OF INFORMATION SYSTEMS ENGINEERING
SPRING SEMESTER OF 2022-20232 ACADEMIC YEAR
ISE223 COMPUTER ARCHITECTURE MIDTERM EXAM

(Following items will be completed in ink) **Date**: 02 May 2022

Student's Name & Surname : .....
PRU student number : .....
Department : .....
Signature : .....

Score	

INSTRUCTIONS:

All your writing must be handed in.
Your answers must be increase ordered (1, 2, …).
Scan your paper to pdf and send only one pdf file.

Time allocated	: **100 minutes**
Instructor	: Assist. Prof. Dr. Mehmet Zeki KONYAR
Instructor's signature	: .....

GOOD LUCK…

QUESTIONS:

See attached sheets for questions.

QUESTIONS:

Q-1. Complete the following sentences:

a-) ……refers to those attributes of a system visible to a programmer or, put another way, those attributes that have a direct impact on the logical execution of a program.

b-) …… refers to the operational units and their interconnections that realize the architectural specifications.

c-) The …….. defines instruction formats, instruction opcodes, registers, instruction and data memory; the effect of executed instructions on the registers and memory; and an algorithm for controlling instruction execution.

Q-2.
a-) What are the four main functions of a computer?
b-) Explain Moore's law.

Q-3. Consider two different computers, with two different instruction sets, both of which have a clock rate of 300 MHz. The following measurements are recorded on the two computers running a given set of benchmark programs.
a-) Determine the effective CPI, MIPS rate, and execution time for each machine.
b-) Comments on the results and compare the computers.

Computer	Instruction Type	Instruction Count (millions)	Cycles per Instruction
Computer A	Arithmetic and logic	8	1
	Load and store	4	3
	Branch	2	4
	Others	4	3
Computer B	Arithmetic and logic	10	1
	Load and store	8	2
	Branch	2	4
	Others	4	3

Q-4. A processor has access to 3 levels of cache memory. Level 1 has an access time of 0.01 μs; Level 2 has an access time of 0.1 μs. And Level 3 has an access time 1 μs. Assume that if a word to be accessed is in level 1, then the processor accesses it directly. If it is in level 2, then the word is first transferred to level 1 and then accessed by the processor. If it is in level 3, then it is transferred to level 2 and level 1 respectively.

Suppose 90% of the memory accesses are found in level 1, %8 of the memory accesses are found in level 2 and rest of are found in level 3. Calculate the average time to access the memory.

Q-5. Explain MBR, MAR, PC, IR, I/OAR, and O/OBR with an example.

Q-6. Draw the memory hierarchy and explain the advantage of the using register and cache for memory.

Q-7. Draw the instruction cycle state diagram and use a sample instruction code example to explain each element.