Tahmini Ders İçeriği
(Tentative Couse Schedule – Syllabus)

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1. Hafta: Sayısal Sinyaller/Sistemler, İkilik Tabanda Sayılar, Taban Aritmetiği, İşaretli/Eksi Sayıların Gösterimi, Sayısal Tasarım Tarihçesi

2. Hafta: İkili Mantık Aritmetiği ve Kapıları, Bool Cebiri Teorisi ve Tanımları, Bool Fonksiyonları, Kapı-Seviyesinde Yalınlaştırma, Karnough Haritası, Önemsenmeyen Durumlar, NAND, NOR, XOR

3-4. Hafta: FPGA, Birleşik (Combinational) Devreler, Aritmetik Modüller, Decoder, Encoder, Mux, Verilog HDL

5. Hafta: Ardışık (Sequential) Devreler, Mandal (Latch), Flip-Flop, Yazmaçlar (Registers)

Lab Sınavı (265/264L)

6. Hafta: Durum Makinaları, Örnek Tasarımlar, Sayaçlar (Counters)

7. Hafta: FSM Örnekleri

8. Hafta: RTL (Register Transfer Level) ASMD (Algorithmic State Machine and Datapath) Tasarımları

9. Hafta: Durağan Zaman Analizi (Static Timing Analysis)

Ara Sınav (265/264)

10. Hafta: Bellekler, FPGA'da RAM, OpenRAM

11-12. Hafta: **(21-25 Kasım, 28 Kasım – 2 Aralık)** Boru hattı, FPGA ve ASIC Tasarım Akışları

Final **(16 Aralık)** – Proje Teslimleri **(31 Aralık)**

SAYISAL TASARIM AKIŞI

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ASIC (Application Specific Integrated Circuits)
FPGA (Field Programmable Gate Array)

S: Ne zaman FPGA, ne zaman ASIC tasarım seçilir? (FPGA vs ASIC)

C: Bazı tasarım kısıtları incelendiğinde hem FPGA hem de ASIC tasarımın mümkün olduğu gözükür. Bu durumda son ürünün FPGA mi yoksa ASIC mi olacağına karar verilir.

- Düşük güç tüketimi
- Düşük alan tüketimi (footprint)
- Yüksek hız gereksinimi
- Mixed-signal tasarım blokları
- Yüksek adetli üretim (> 100_000)

→ ASIC

- Markete hızlı giriş (faster time to market)
- Sonradan programlanabilme
- Prototipleme
- Düşük adetli üretim
- Düşük tasarım ve NRE maliyeti

→ FPGA

anysilicon

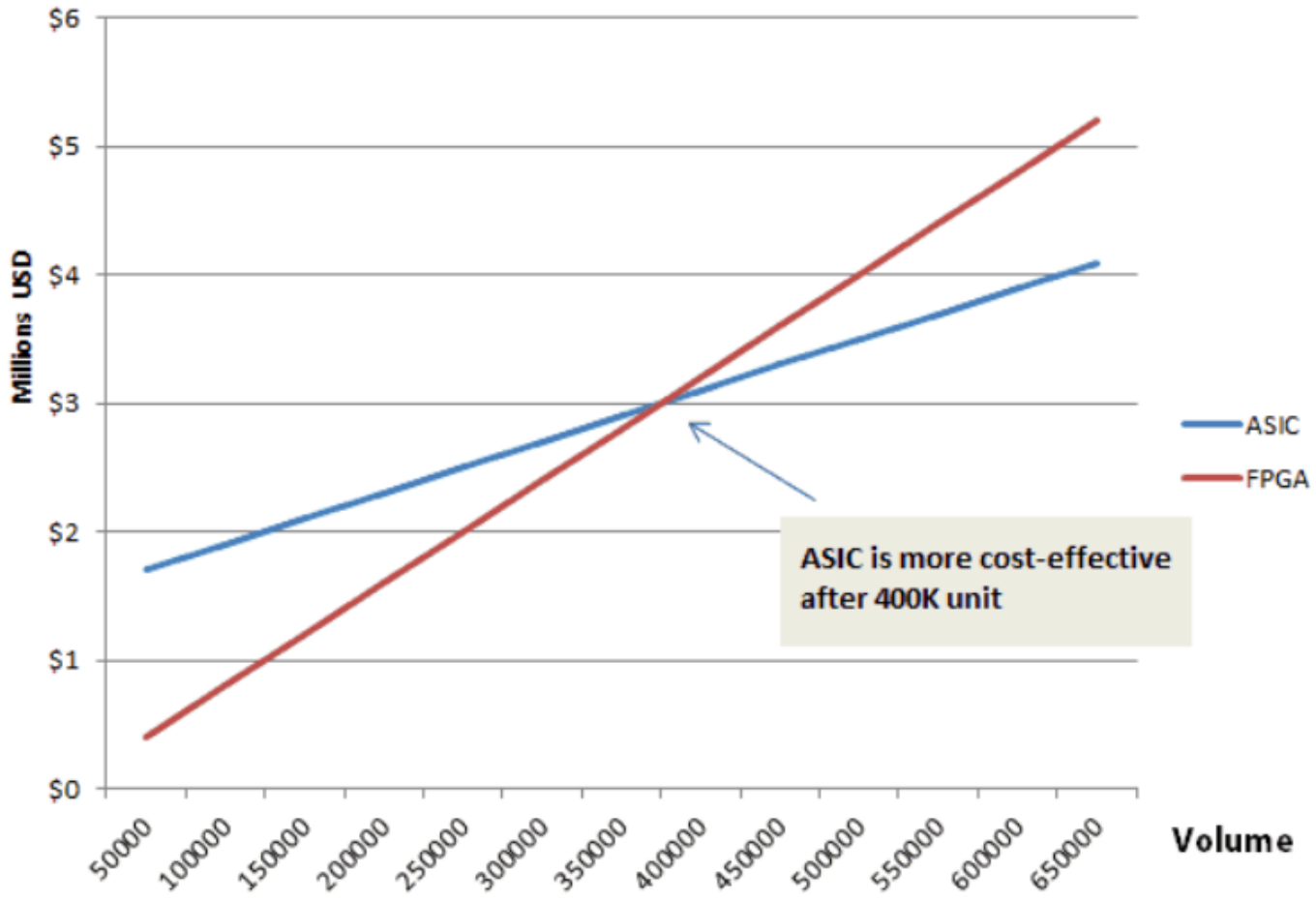
	FPGA	ASIC
Time to Market	Fast	Slow
NRE	Low	High
Design Flow	Simple	Complex
Unit Cost	High	Low
Performance	Medium	High
Power Consumption	High	Low
Unit Size	Medium	Low

ASIC NRE: $1.5M

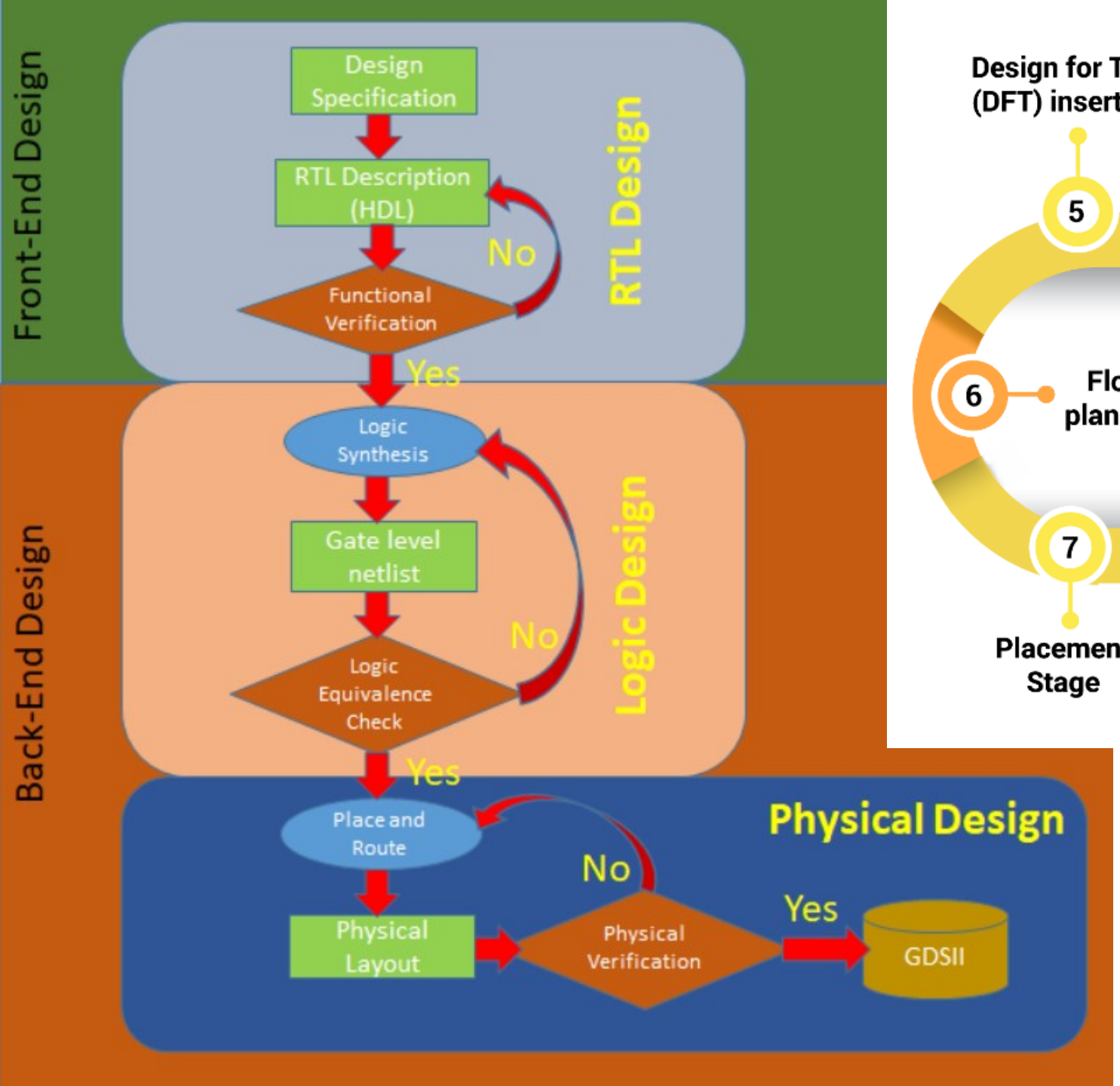
ASIC Unit Cost: $4

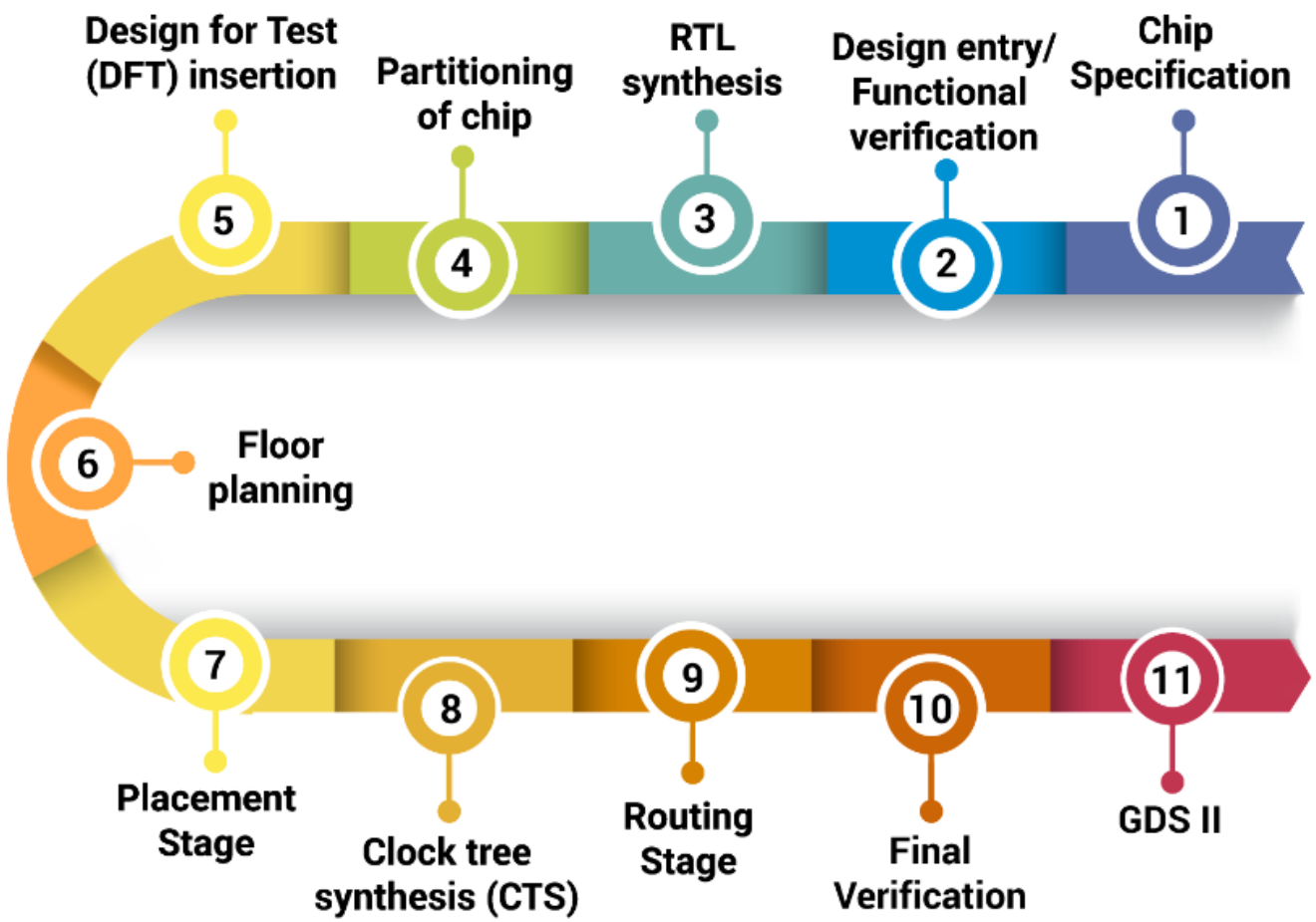
FPGA NRE: $0

FPGA Unit Cost: $8



Total Cost ASIC vs FPGA including NRE in MUSD





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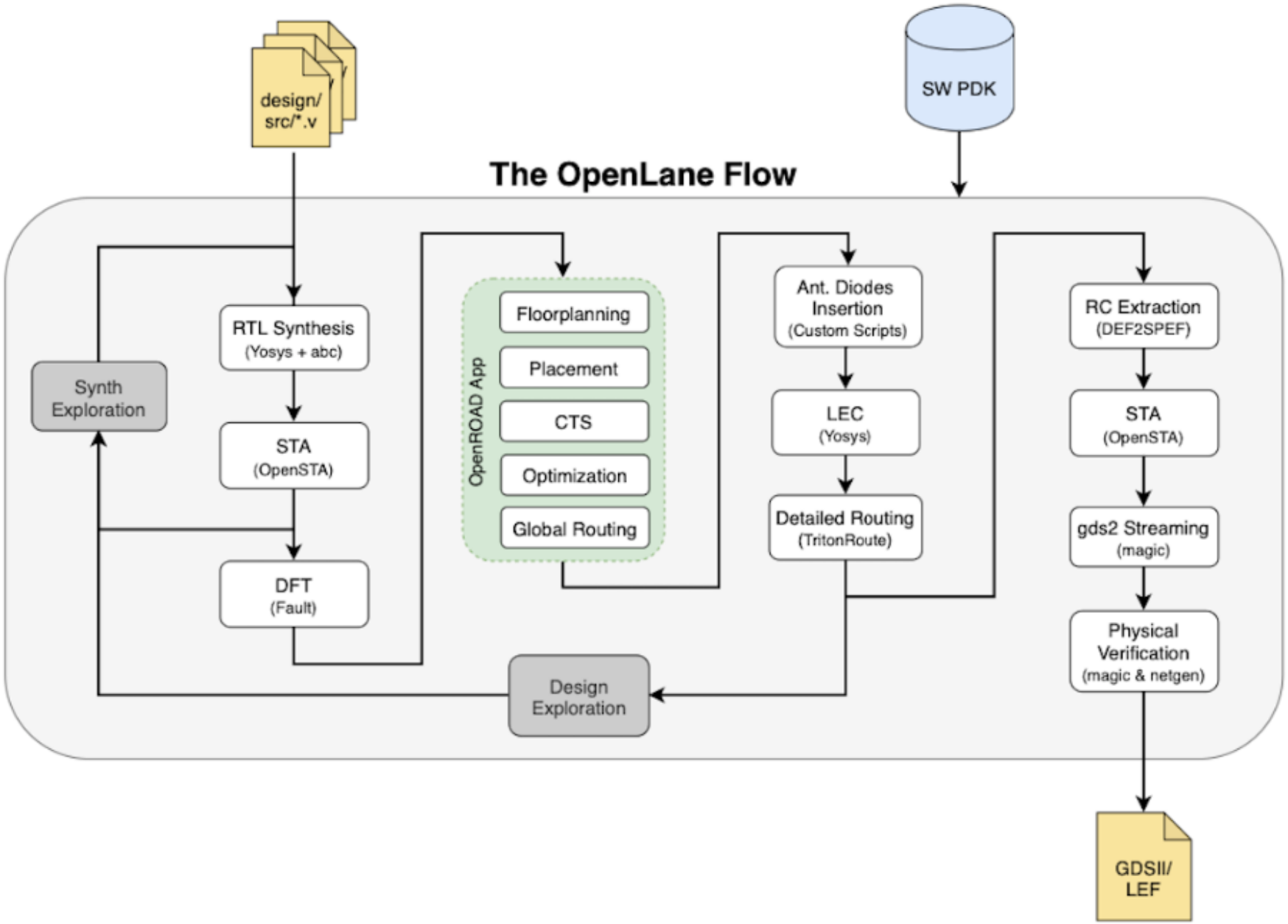
OpenLane Architecture



ASIC TASARIM NASIL YAPABİLİRİM ?

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EDA (Electronic Design Automation) Araçları: Big Three

1. Cadence
2. Synopsys
3. Mentor (Siemens)

Yüzbinlerce, hatta milyonlarca dolar lisans ücreti !!!

AÇIK-KAYNAK ASIC TASARIM ARACI ???

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siliconcompiler / siliconcompiler Public

Watch 18 | Fork 61 | Star 527

Code | Issues 40 | Pull requests 11 | Discussions | Actions | Security | Insights

main | 108 branches | 15 tags | Go to file | Add file | Code

aolofsson Merge pull request #1164 from siliconcompiler/sc_client_message_update ... 5fd04e7 on Oct 25 4,481 commits

.github/workflows	Specify Python locations explicitly	3 months ago
docs	Add :keypath: role to public Sphinx extensions	3 months ago
examples	Merge pull request #1104 from siliconcompiler/caravel_wrapper_fixes	3 months ago
setup	Make Surelog install script consistent w/ OpenROAD	4 months ago
siliconcompiler	Remove debugging message	2 months ago
tests	Merge pull request #1159 from siliconcompiler/dedup_import_inputs	2 months ago
third_party	Update Surelog submodule	2 months ago
.gitattributes	Trying to fix language detection issue	2 years ago
.gitignore	Build simple Cython module through scikit-build	15 months ago
.gitmodules	Remove submodule ettus-uhd	13 months ago
.pylintrc	Switch to Google pylintrc as starting place	13 months ago

About

A modular build system for hardware

- Readme
- Apache-2.0 license
- Security policy
- 527 stars
- 18 watching
- 61 forks

Releases 15

v0.9.6 Latest
on Oct 4

+ 14 releases

Packages

No packages published

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SiliconCompiler

Docs Sou

Compile code into silicon

Free Beta Access

Process scaling is coming to an end and it is a social imperative that we find a new path to extend the Moore's Law exponential. The most viable option is extreme silicon specialization, which will require fast automated translation from program to silicon. Compiling simple programs into silicon should be like using llvm or gcc: fast, automated, and accessible.

```
$ pip install siliconcompiler
$ sc hello.v -target lambda7
```

Supported Technologies

Type	Supported
Languages	C, SV, VHDL, Chisel, Migen/Amaranth, Bluespec
Simulation	Verilator, Icarus, GHDL
Synthesis	Yosys, Vivado, Synopsys, Cadence
ASIC APR	OpenRoad, Synopsys, Cadence
FPGA APR	VPR, nextpnr, Vivado
Layout Viewer	Klayout, Cadence, Synopsys
DRC/LVS	Magic, Mentor, Synopsys
PDKs	sky130, asap7, freepdk45

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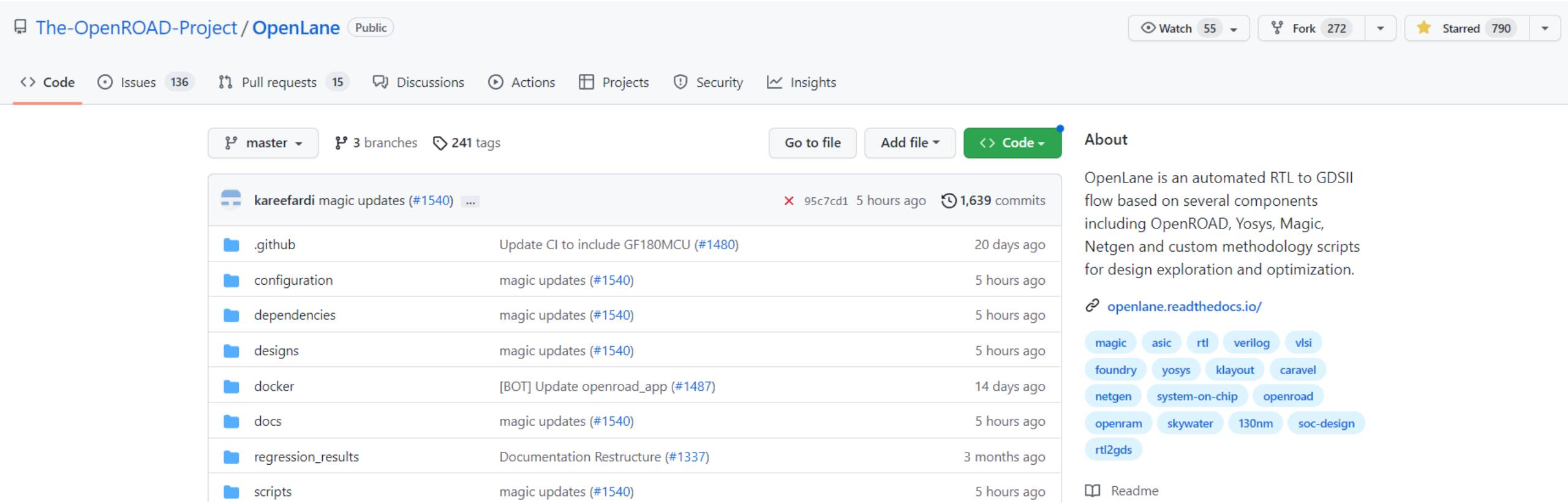

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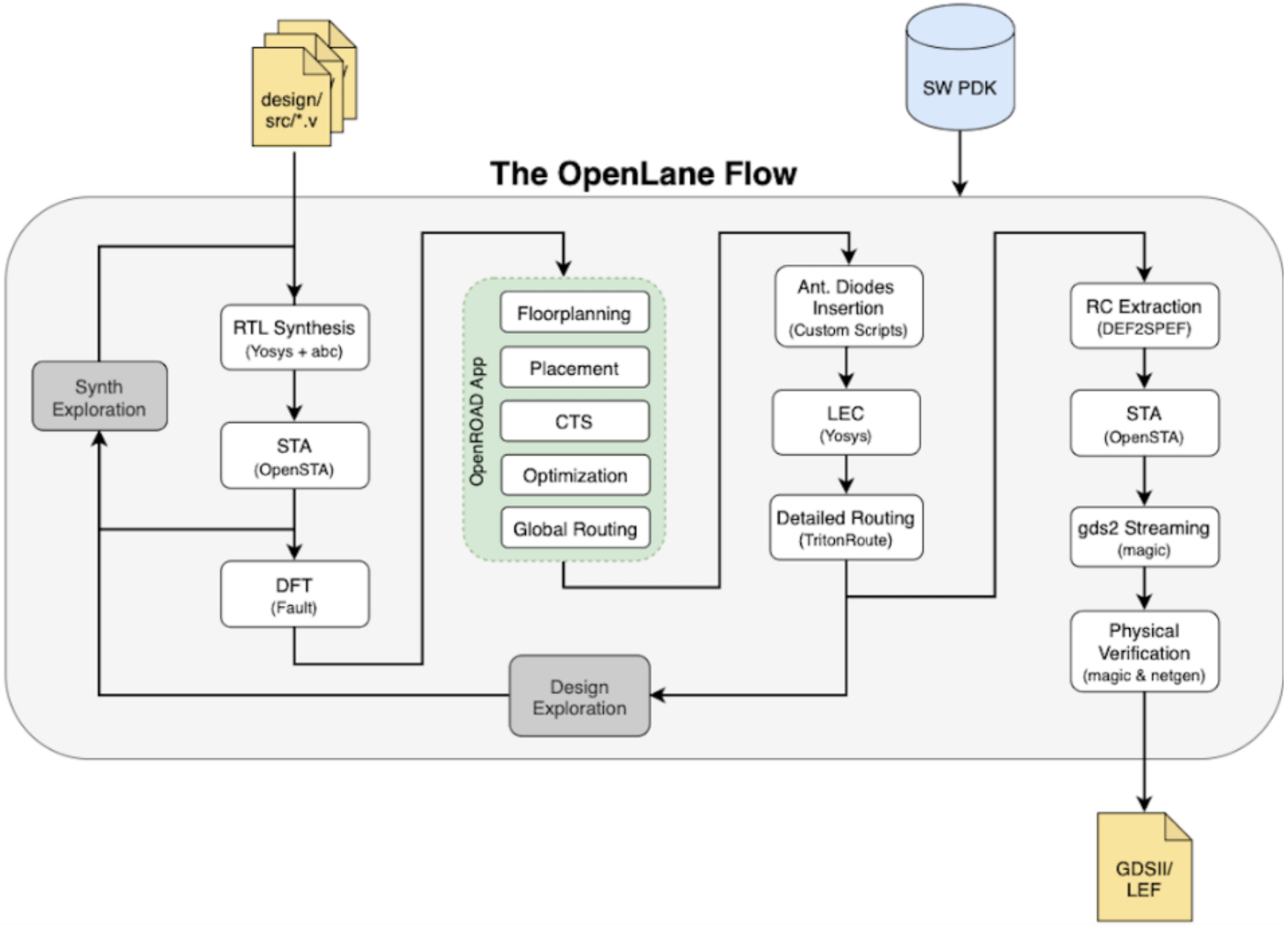

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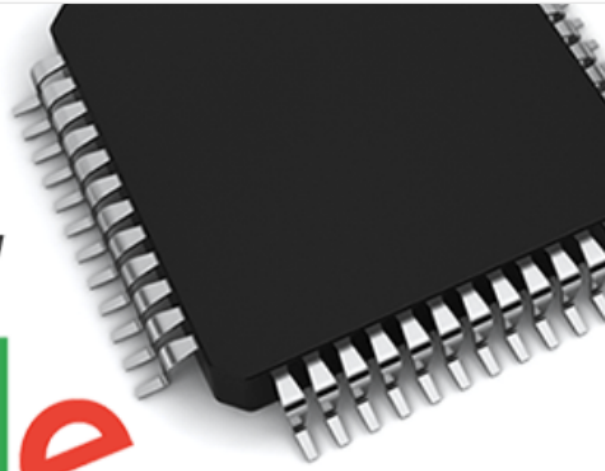

MPW-7 Submission Deadline is September 12

Welcome to the Efabless Open MPW Program

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ÇİP TASARIMI

Mehmet Burak Aykenar

Public

4 videos Last updated on Jul 19, 2022

Play all Shuffle

No description

Sort

ÇİP TASARIMI - Ders 1: Açık-Kaynak Openlane Kurulumu | Örnek Proje Derlenmesi | Google Open MPW

Mehmet Burak Aykenar

ÇİP TASARIMI - Ders 2: SKY130 Skywater Açık-Kaynak Process Design Kit (PDK)

Mehmet Burak Aykenar

YONGA (ÇİP) TASARIMI - Ders 3: Teknofest Çip Tasarım Yarışması için Openlane Kurulumu ve İncelemesi

Mehmet Burak Aykenar

YONGA (ÇİP) TASARIMI - Ders 4: Openlane Tasarım Ekleme - Örnek Uygulama | Floating Point Unit

Mehmet Burak Aykenar

FPGA FİRMALARI

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AMD | XILINX

intel

ALTERA

Microsemi
a MICROCHIP company

LATTICE SEMICONDUCTOR

FPGA EDA ARAÇLARI

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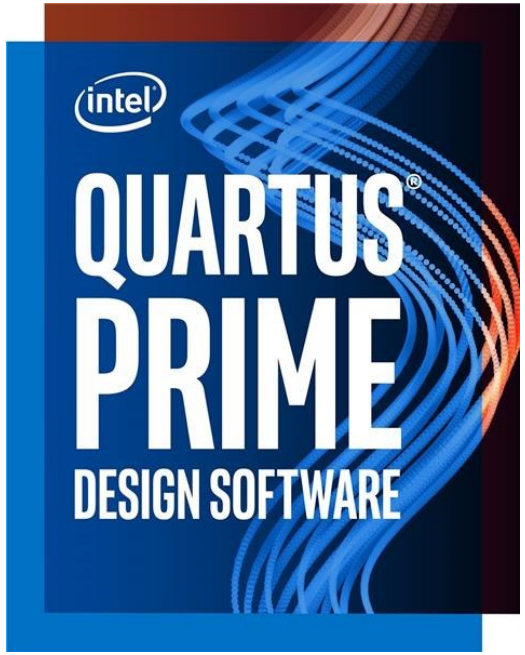
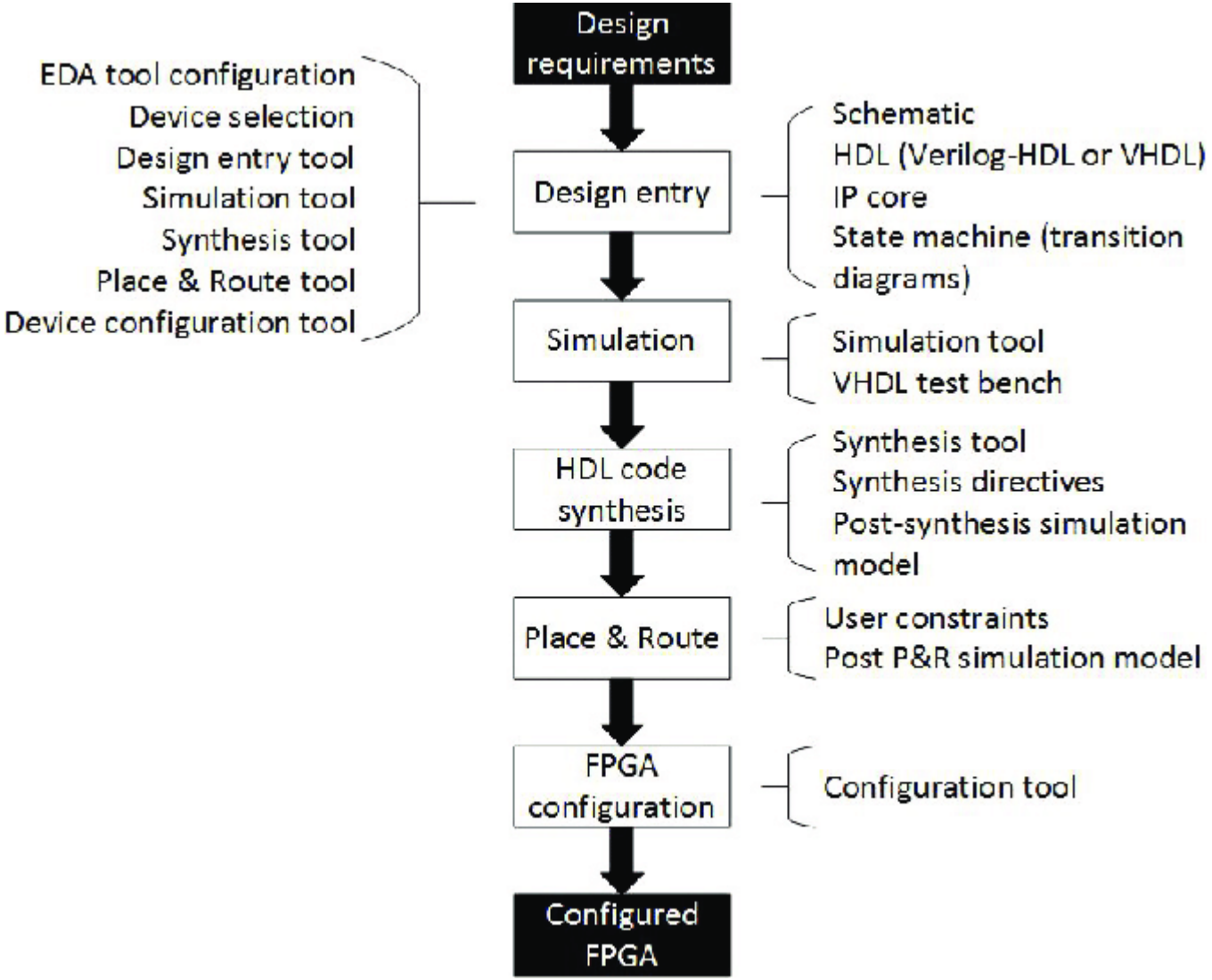
VIVADO™

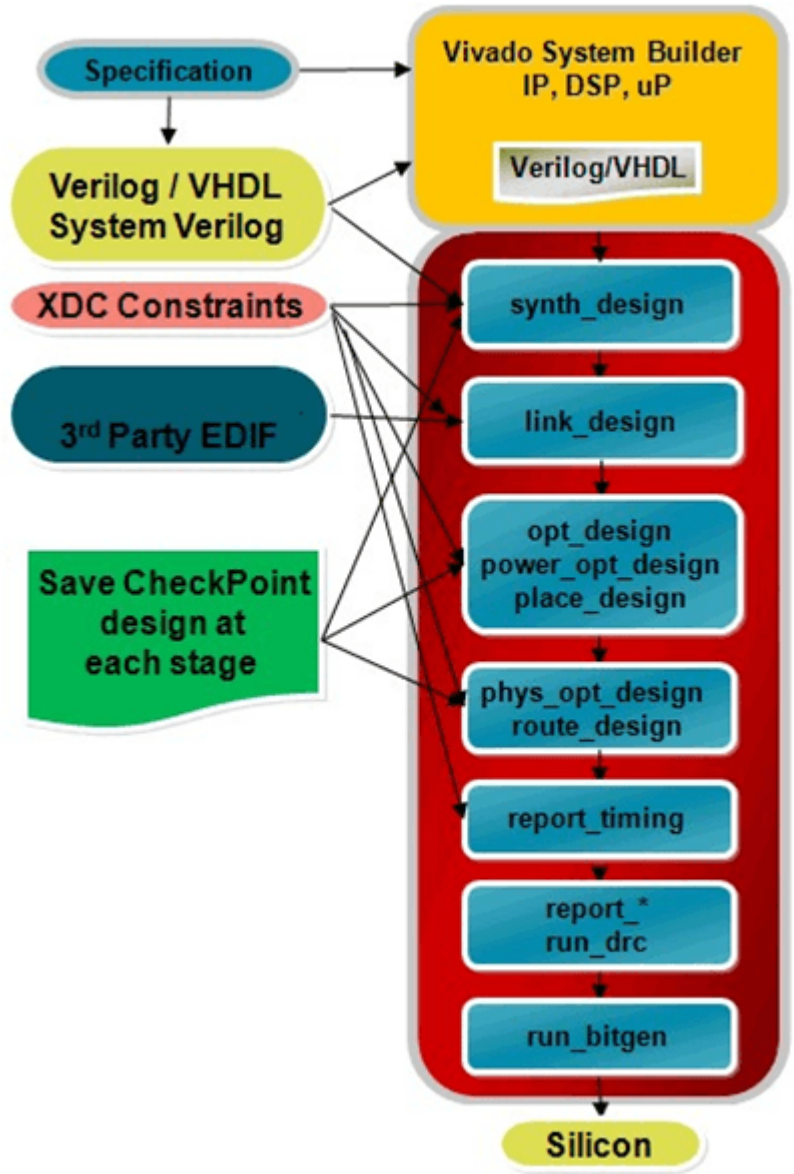


Libero
System-on-Chip

LATTICE
DIAMOND
DESIGN SOFTWARE

FPGA TASARIM AKIŞI






The End