Tahmini Ders İçeriği
(Tentative Couse Schedule – Syllabus)

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1. Hafta: Sayısal Sinyaller/Sistemler, İkilik Tabanda Sayılar, Taban Aritmetiği, İşaretli/Eksi Sayıların Gösterimi, Sayısal Tasarım Tarihçesi

2. Hafta: İkili Mantık Aritmetiği ve Kapıları, Bool Cebiri Teorisi ve Tanımları, Bool Fonksiyonları, Kapı-Seviyesinde Yalınlaştırma, Karnough Haritası, Önemsenmeyen Durumlar, NAND, NOR, XOR

3-4. Hafta: FPGA, Birleşik (Combinational) Devreler, Aritmetik Modüller, Decoder, Encoder, Mux, Verilog HDL

5. Hafta: Ardışık (Sequential) Devreler, Mandal (Latch), Flip-Flop, Yazmaçlar (Registers)

Lab Sınavı (265/264L)

6. Hafta: Durum Makinaları, Örnek Tasarımlar, Sayaçlar (Counters)

7. Hafta: FSM Örnekleri

8. Hafta: RTL (Register Transfer Level) ASMD (Algorithmic State Machine and Datapath) Tasarımları

9. Hafta: **(7-11 Kasım)** Durağan Zaman Analizi (Static Timing Analysis)

Ara Sınav (265/264) **(15 Kasım)**

10. Hafta: **(14-18 Kasım)** Bellekler, FPGA'da Block RAM, OpenRAM

11-12. Hafta: **(21-25 Kasım, 28 Kasım – 2 Aralık)** Boru hattı, FPGA ve ASIC Tasarım Akışları

Final **(Aralık)** – Proje Teslimleri **(18 Aralık)**

DURAĞAN ZAMAN ANALİZİ (STATIC TIMING ANALYSIS - STA)

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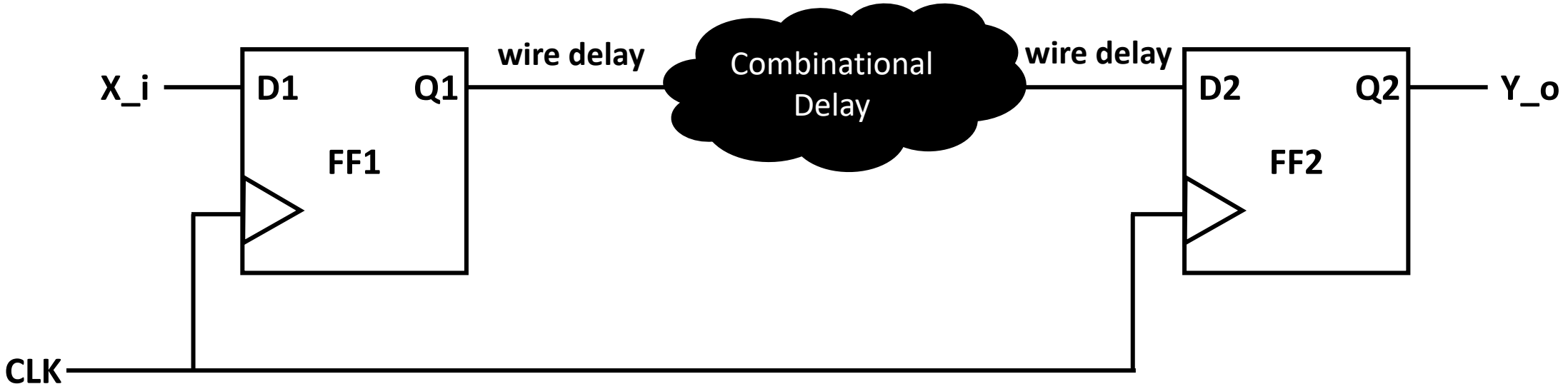
Durağan: Devre sentezlendikten sonra, donanım üzerinde çalışmadan, durağanken, dinamik ya da elektronlar hareketli değilken yapılan bir analizdir

Zaman: Devrenin, istenilen saat frekansında doğru çalışıp çalışamayacağını inceler

Analiz: Bir analiz işlemidir, yani var olan bir netlist (sentez sonucu) içerisinde bulunan mantık hücrelerinin ve aralarındaki bağlantı yollarının gecikmelerini ve yine saat sinyali ile ilgili belirsizlikleri hesaba katan bir bilgisayar yazılımıdır

TANIMLAR



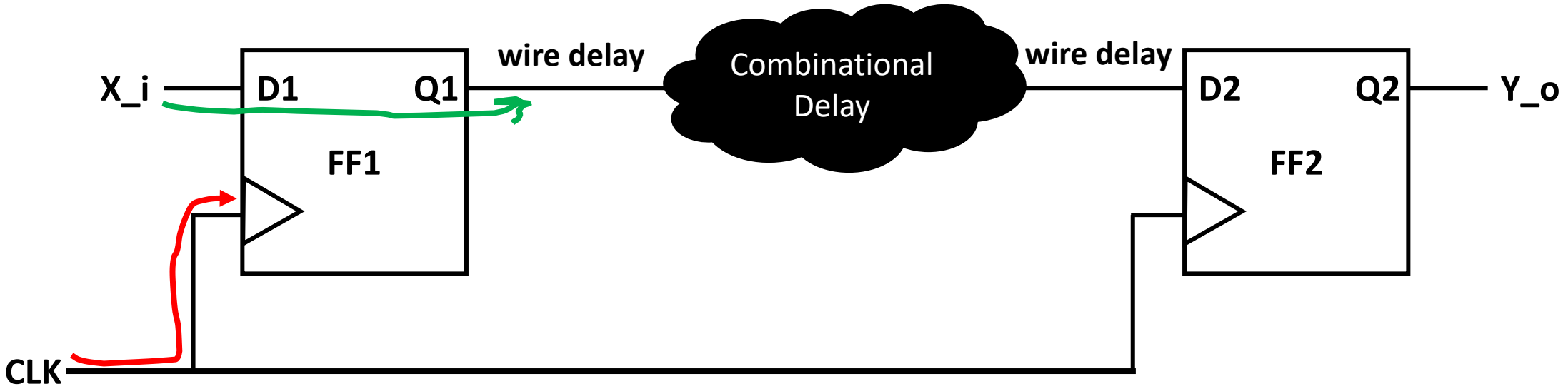
FF1: Kaynak (Source) Flip-Flop

FF2: Hedef (Destination) Flip-Flop

Combinational Delay: Sinyalin birleşik (combinational) devre elemanlarında ilerlerken meydana gelen gecikme

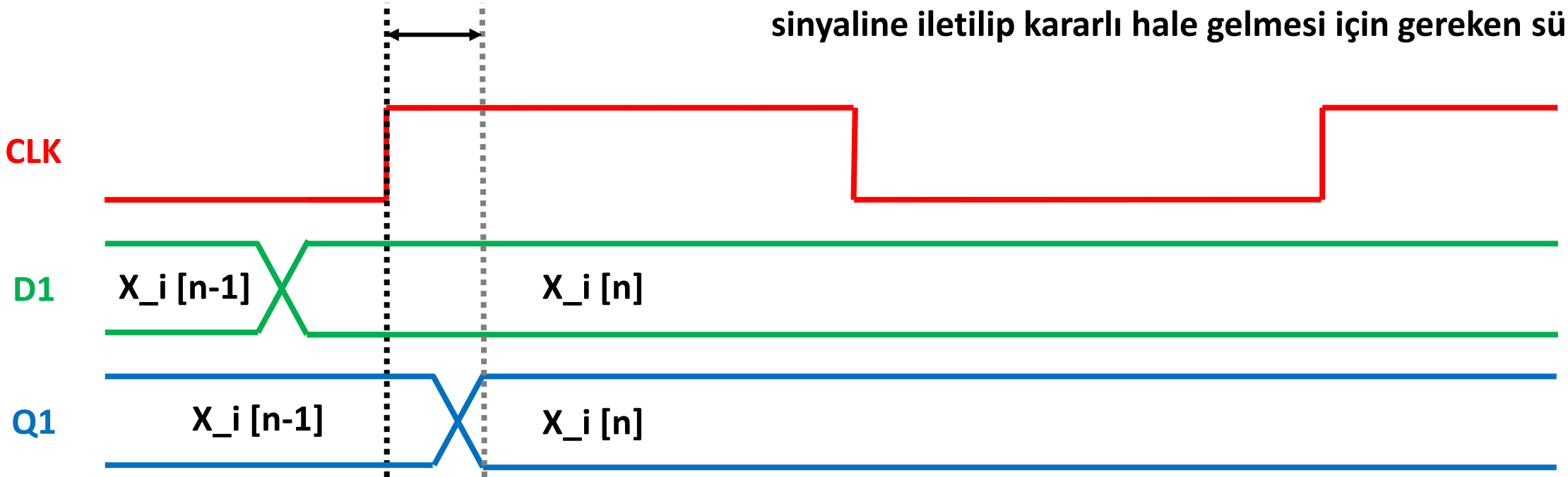
Wire Delay (Routing Delay): Sinyalin bağlantı kablosu, yolu üzerinde ilerlerken meydana gelen gecikme

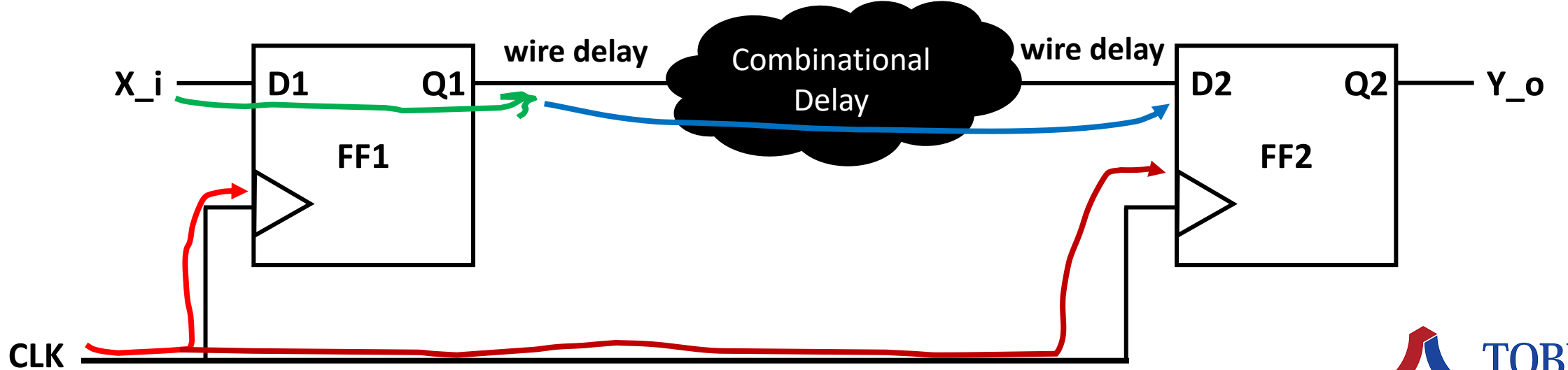
BİR SİNYALİN YOLCULUĞU



Tcq: clock-to-q delay

CLK sinyali yükselen kenarından sonra FF giriş sinyalinin çıkış sinyaline iletilip kararlı hale gelmesi için gereken süre





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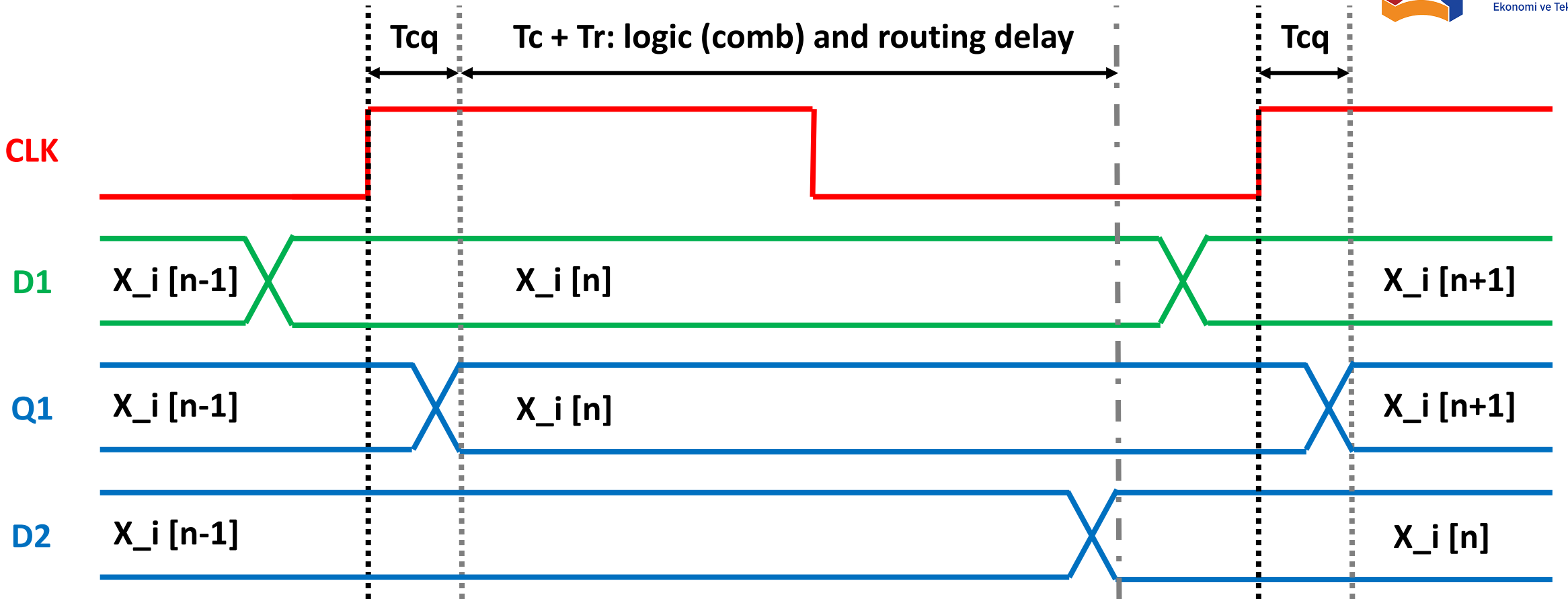
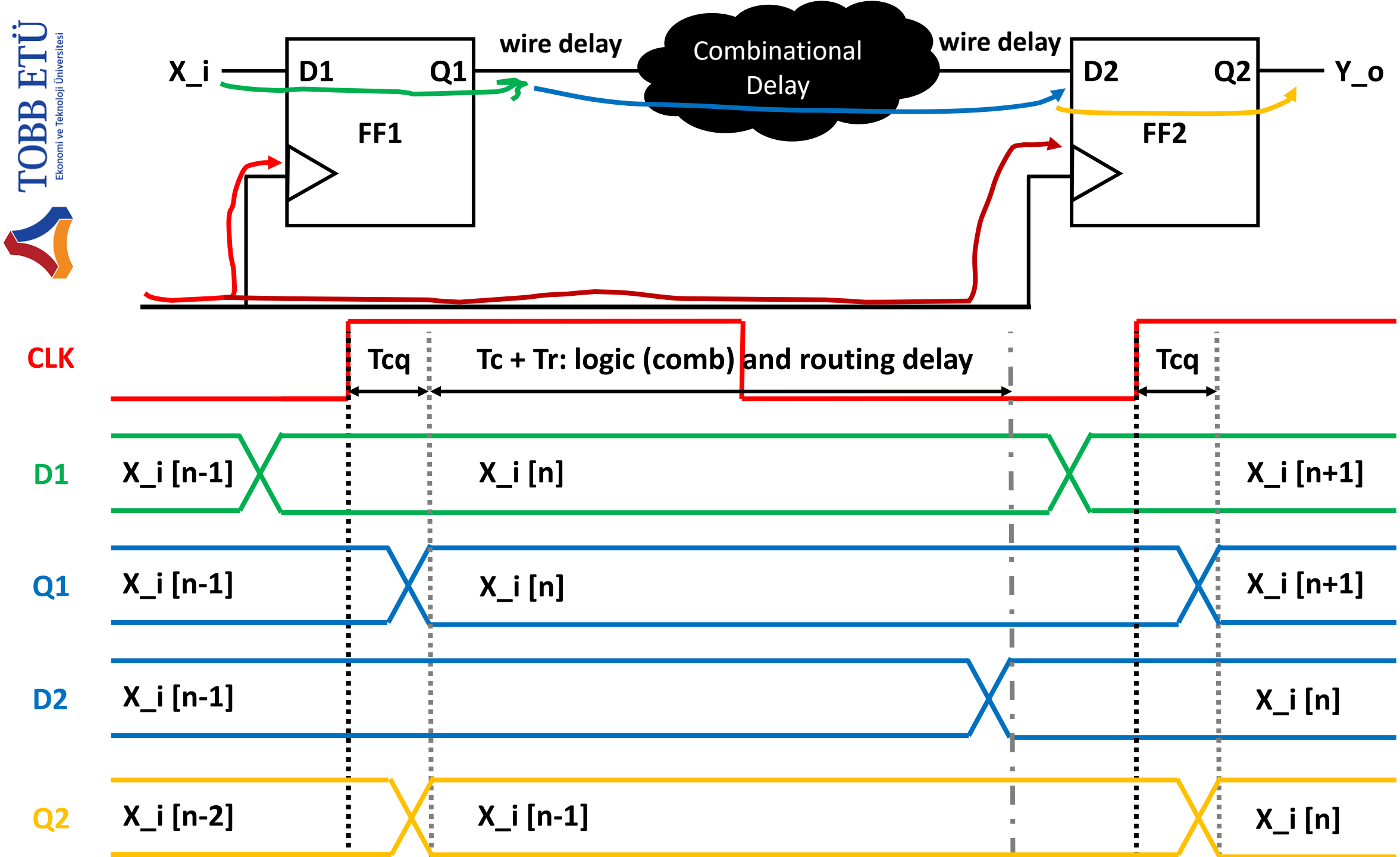
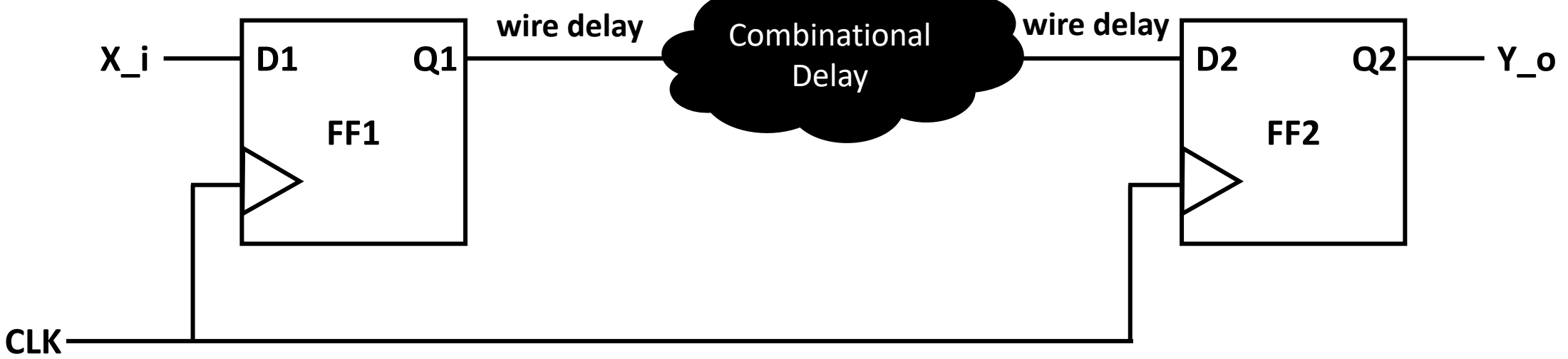
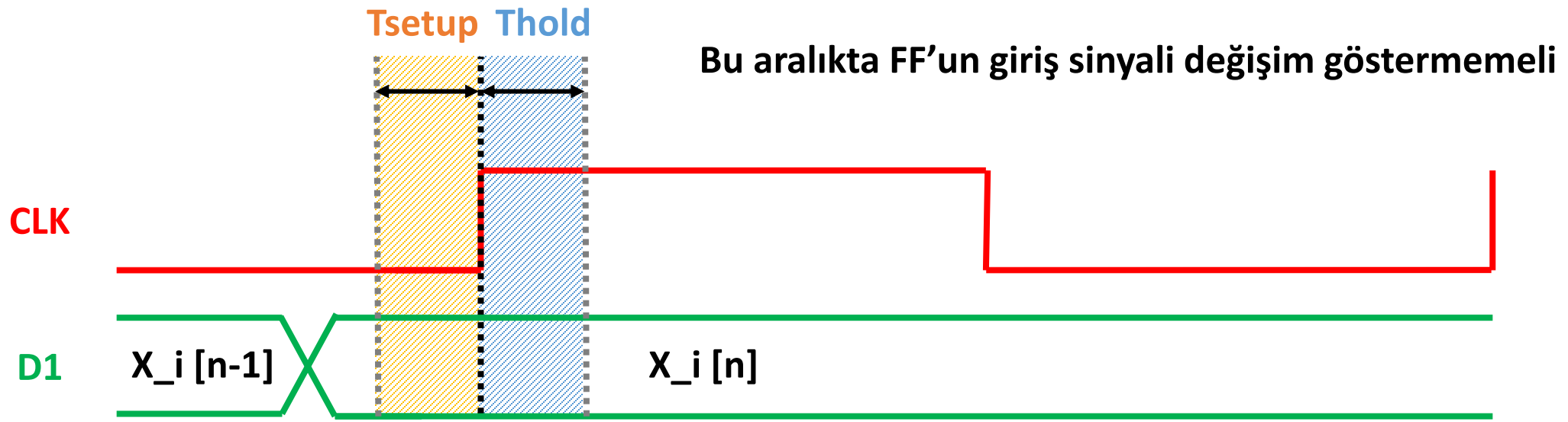


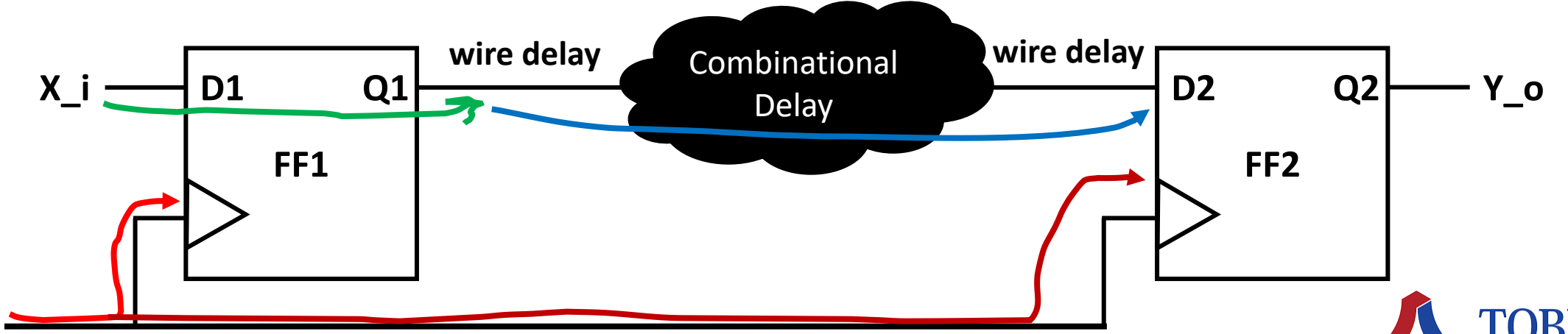

X_i
D1
Q1
FF1
wire delay
Combinational Delay
wire delay
D2
Q2
FF2
Y_o
CLK
Tcq
Tc + Tr: logic (comb) and routing delay
Tcq
D1
X_i [n-1]
X_i [n]
X_i [n+1]
Q1
X_i [n-1]
X_i [n]
X_i [n+1]
D2
X_i [n-1]
X_i [n]
Q2
X_i [n-2]
X_i [n-1]
X_i [n]



Setup Time (Tsetup): Flip-Flop çıkış sinyalinin tutarlı olması için, Flip-Flop giriş sinyalinin (D1) saat sinyalinin yükselen kenarından önce beklemesi gereken süre.

Hold Time (Thold): Flip-Flop çıkış sinyalinin tutarlı olması için, Flip-Flop giriş sinyalinin (D1) saat sinyalinin yükselen kenarından sonra beklemesi gereken süre.





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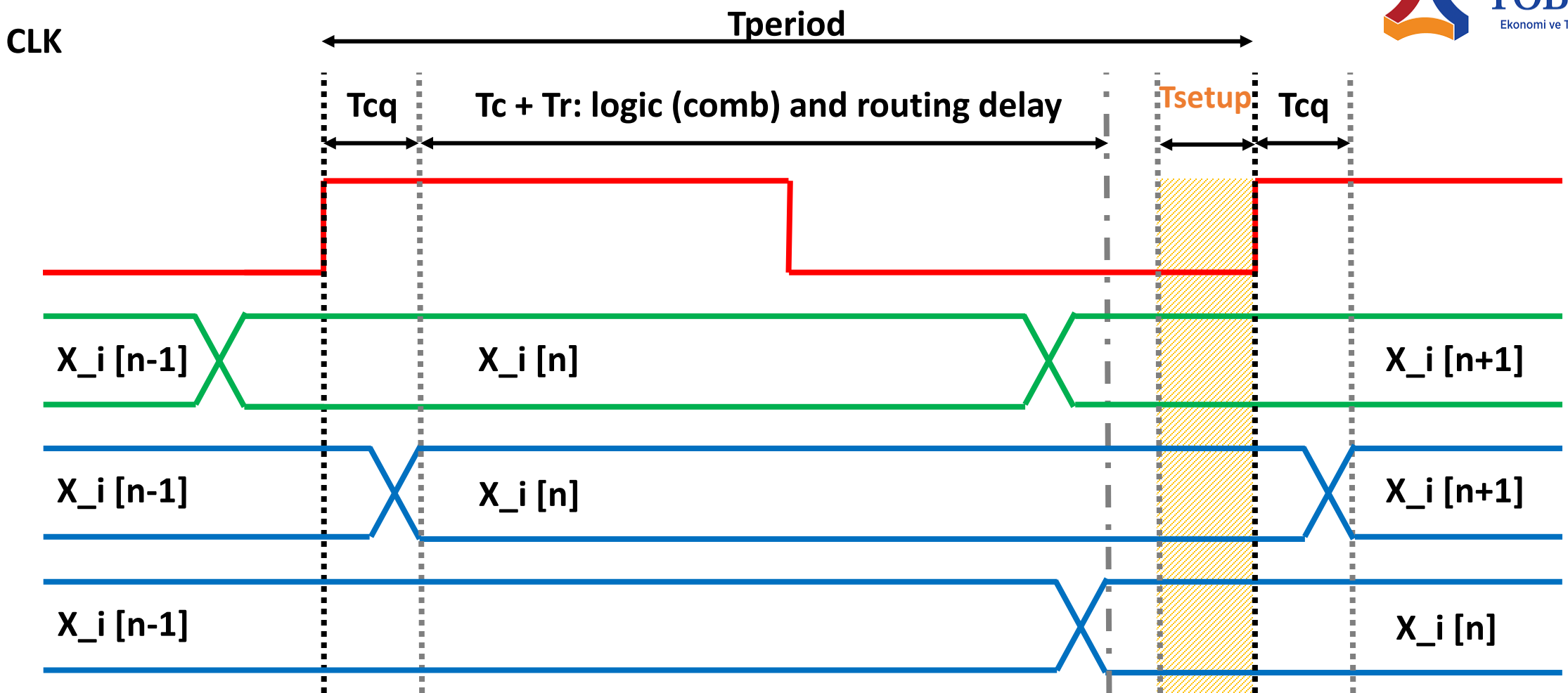

SETUP TIME ANALİZİ - MAX FREKANS FORMÜLÜ

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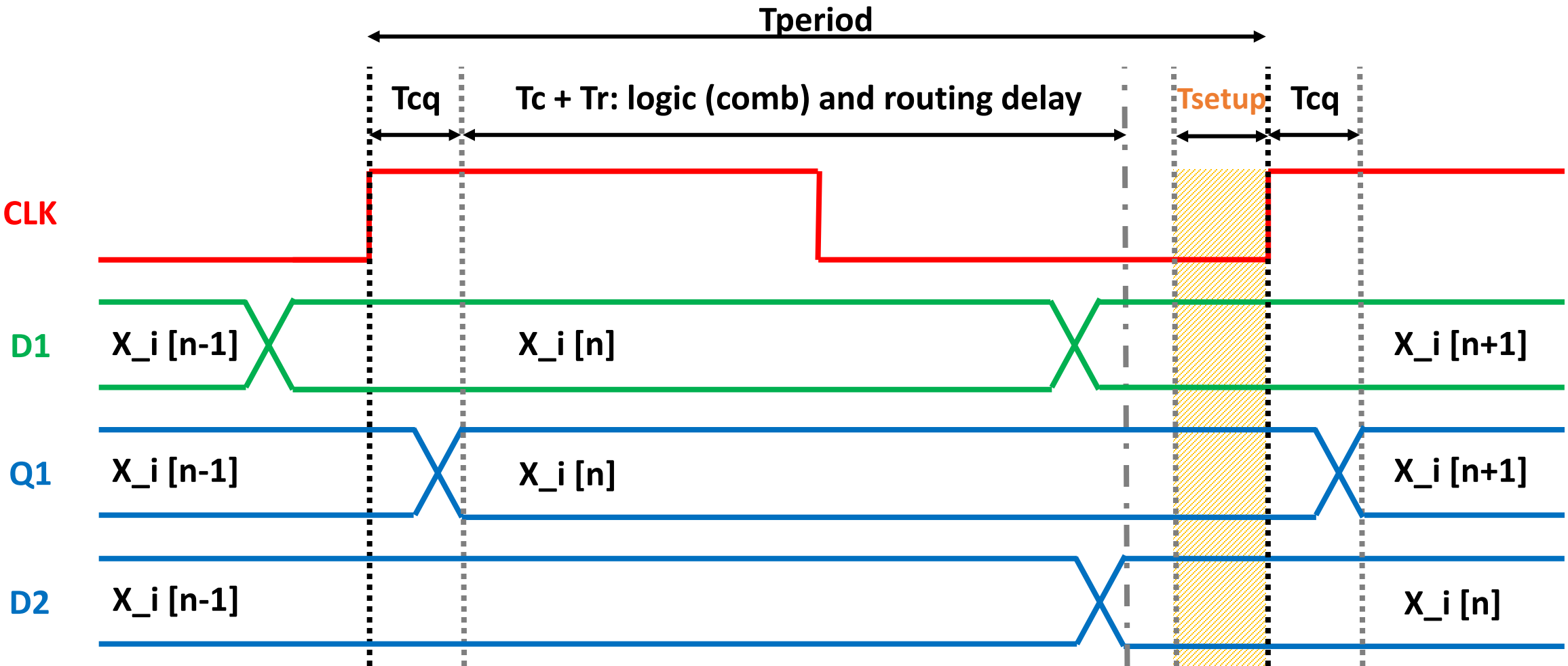
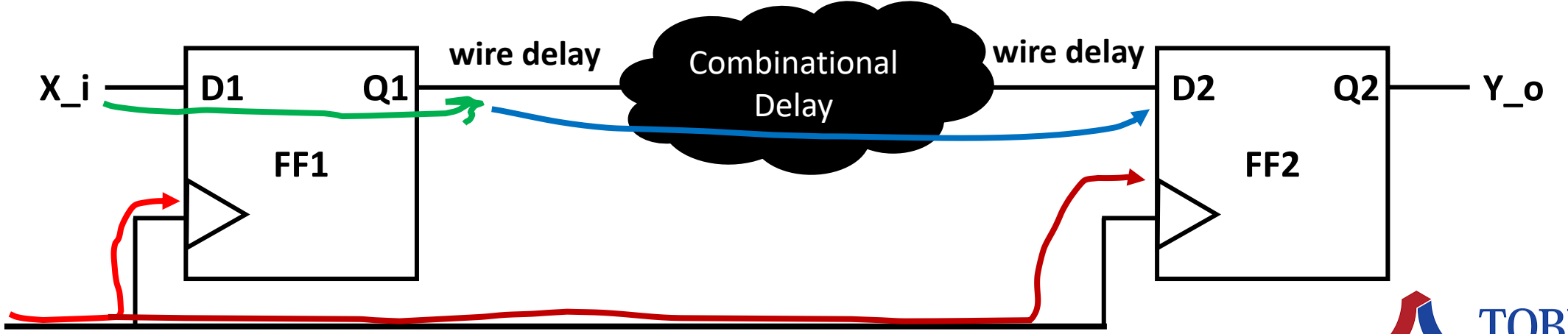
Tperiod – Tsetup > Tcq + Tcomb
Tperiod > Tcq + Tcomb + Tsetup
Period (min) = Tcq + Tcomb + Tsetup
Frequency (max) = 1 / (Tcq + Tcomb + Tsetup)

Slack = Tperiod – (Tcq + Tcomb + Tsetup)

Positive Slack

Negative Slack





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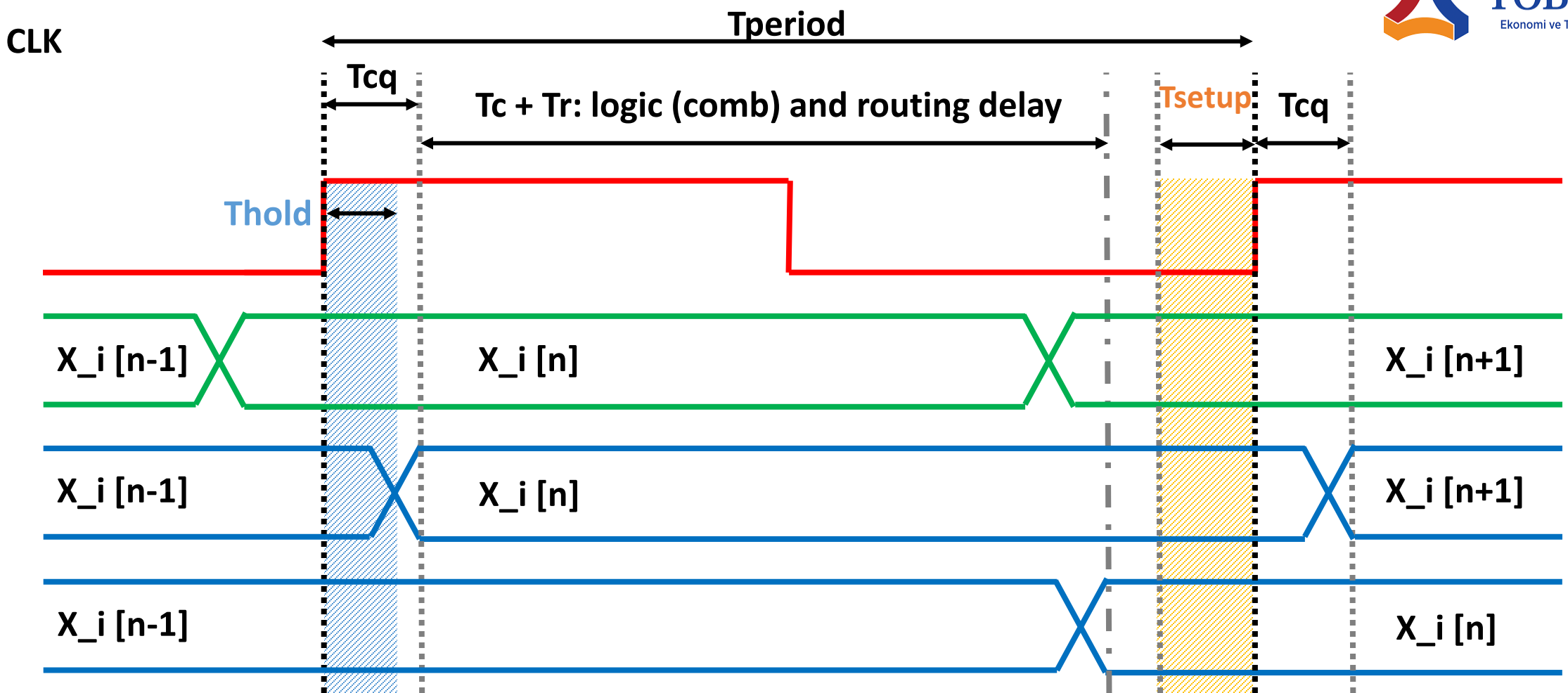

HOLD TIME ANALİZİ

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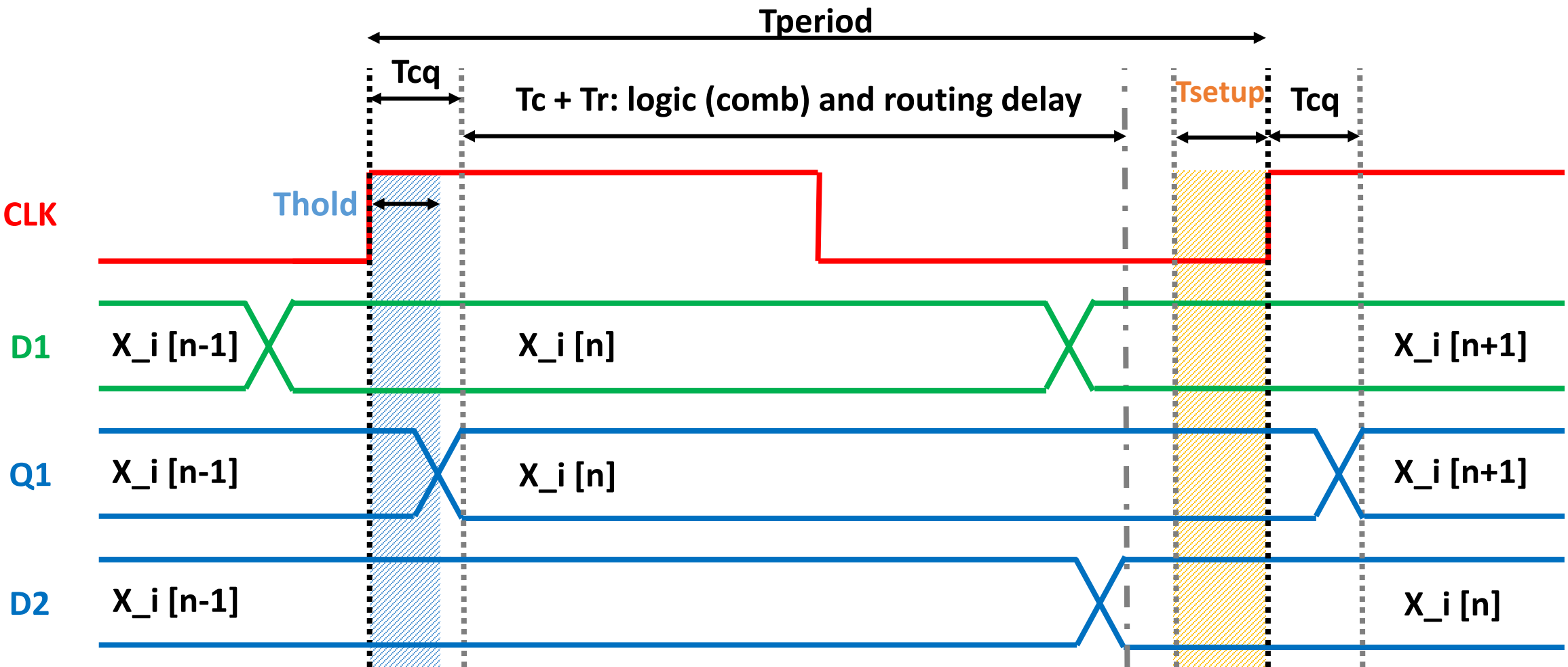
Tcq + Tcomb > Thold
if (Tcomb == 0) “Back to back 2 FF durumu”
Tcq > Thold

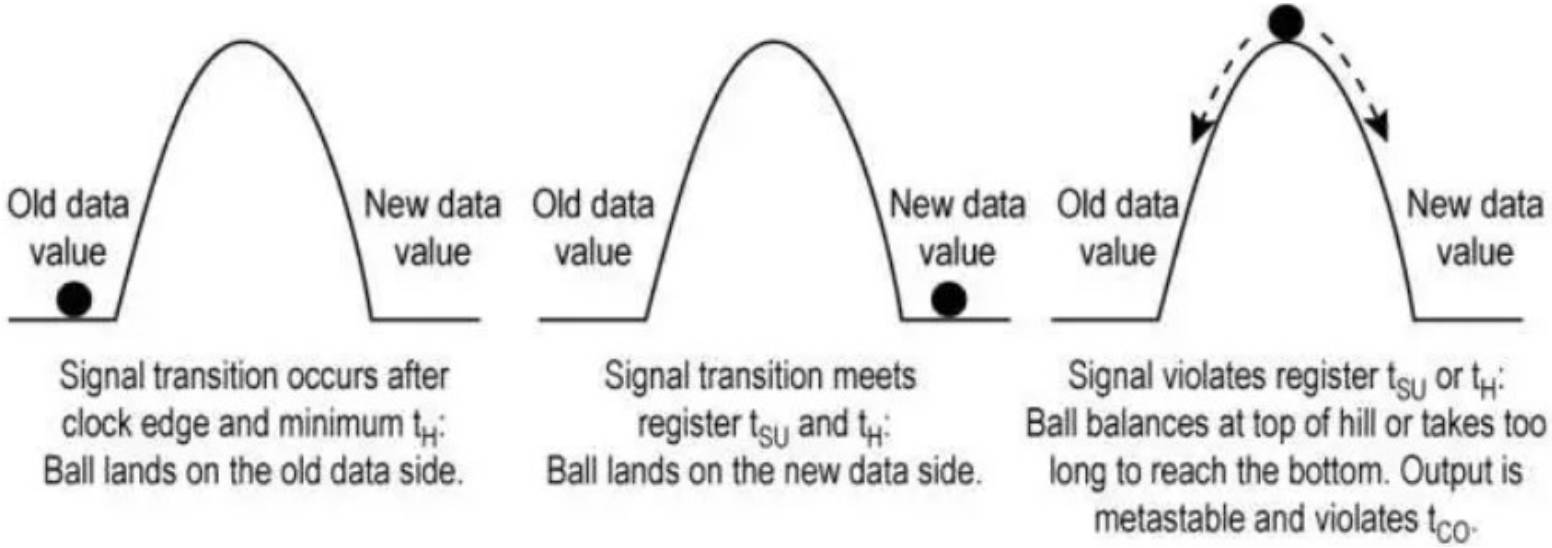
Slack = Tcq + Tcomb - Thold

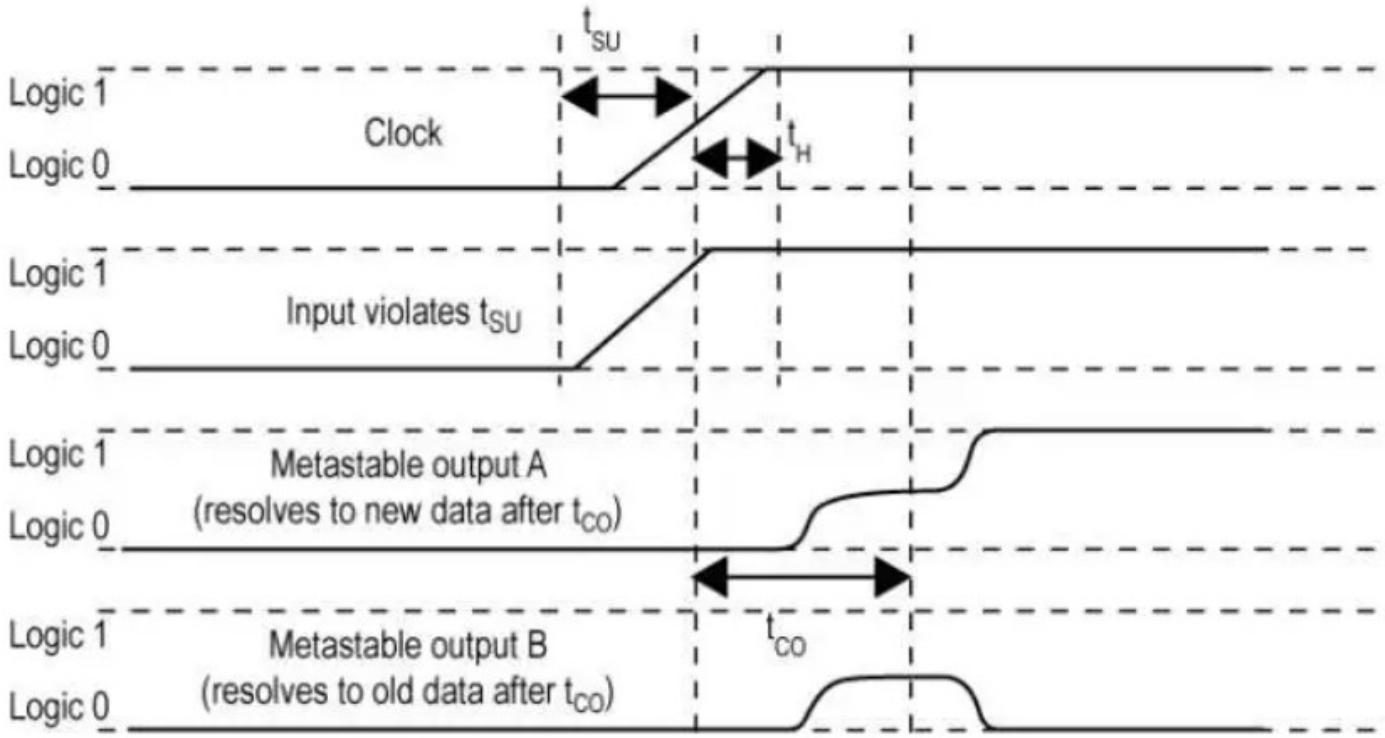
Positive Slack

Negative Slack



METASTABILITY





VIVADO PERIYOT KISITI

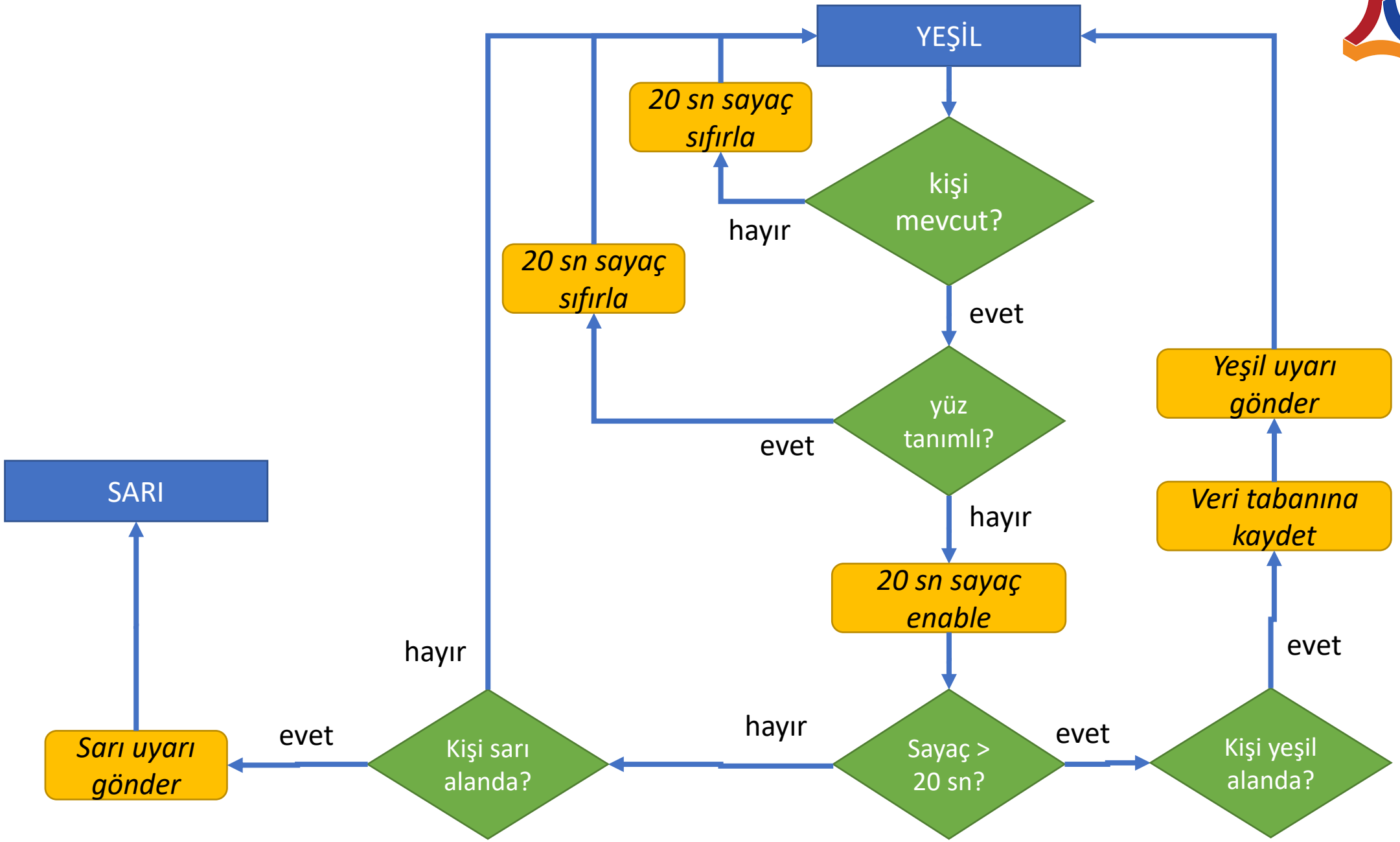
Tperiod – Tsetup > Tcq + Tcomb
Tperiod > Tcq + Tcomb + Tsetup
Period (min) = Tcq + Tcomb + Tsetup
Frequency (max) = 1 / (Tcq + Tcomb + Tsetup)

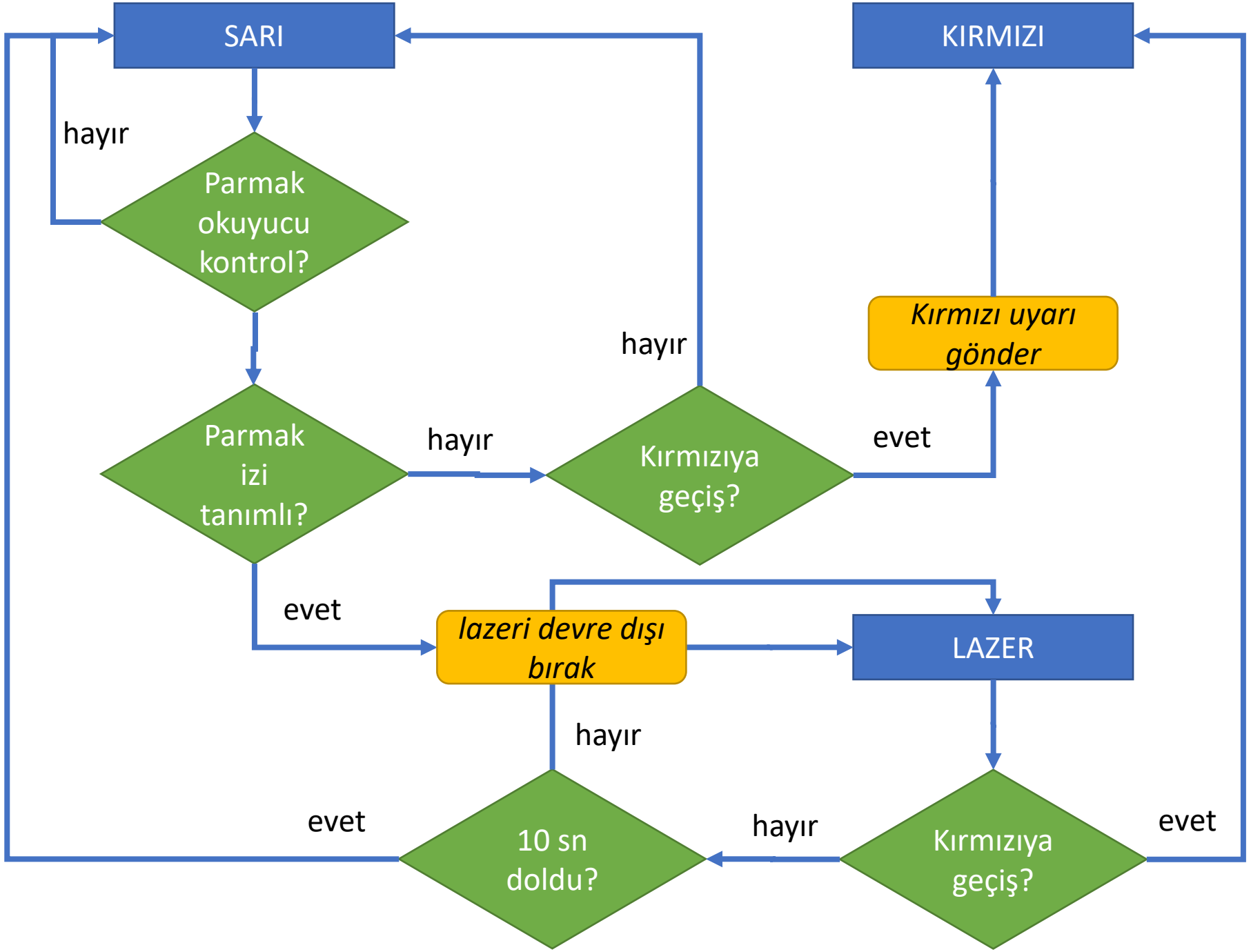
Slack = Tperiod – (Tcq + Tcomb + Tsetup)

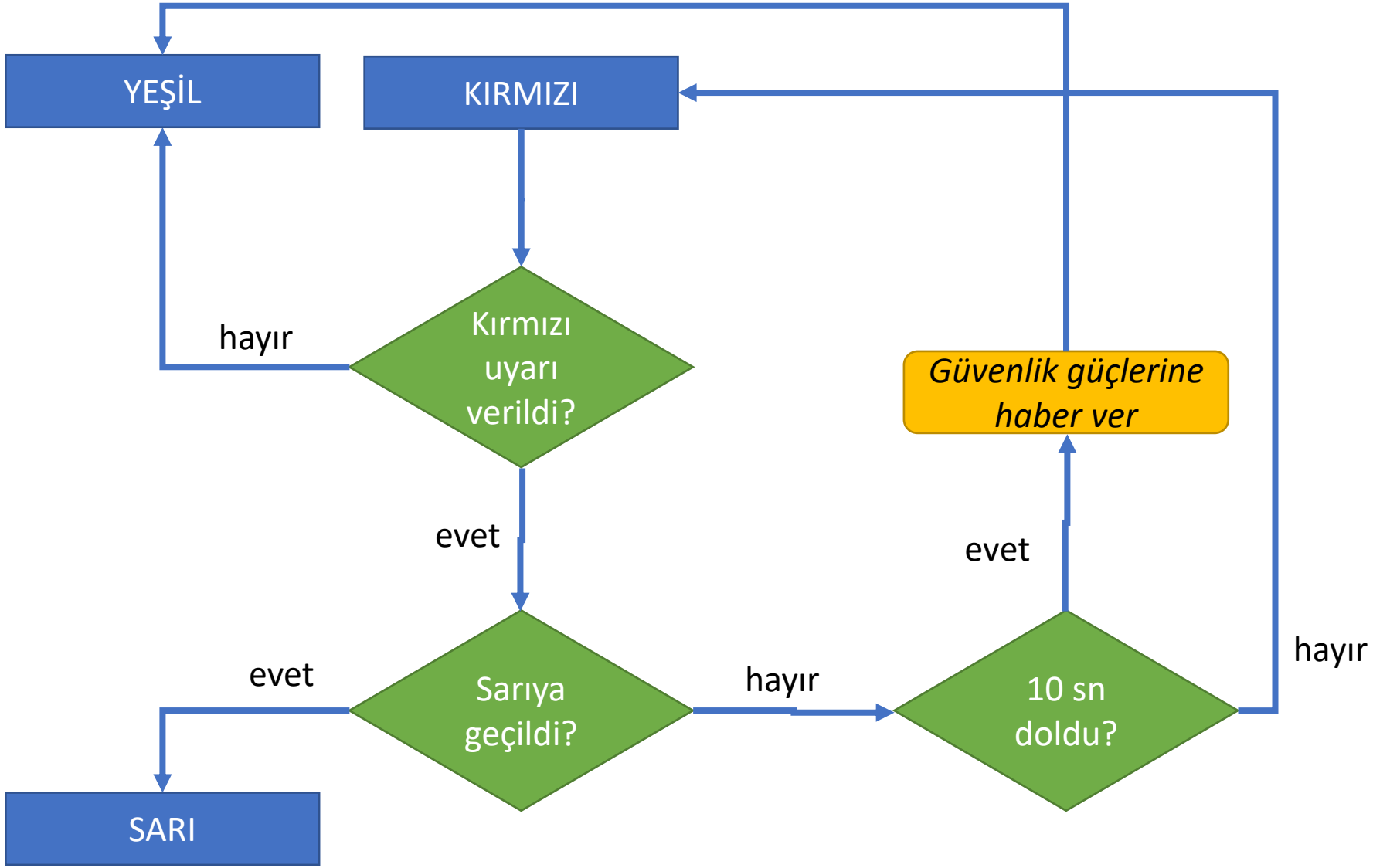
Positive Slack 

Negative Slack 

```
create_clock –name devclk –period 10 [get_ports clk]
```


YEŞİL
20 sn sayaç sıfırla
kişi mevcut?
hayır
20 sn sayaç sıfırla
evet
yüz tanımlı?
evet
Yeşil uyarı gönder
SARI
hayır
20 sn sayaç enable
Veri tabanına kaydet
hayır
evet
Sarı uyarı gönder
evet
Kişi sarı alanda?
hayır
Sayaç > 20 sn?
evet
Kişi yeşil alanda?


SARI
KIRMIZI
hayır
Parmak okuyucu kontrol?
hayır
Kırmızı uyarı gönder
Parmak izi tanımlı?
hayır
Kırmızıya geçiş?
evet
evet
lazeri devre dışı bırak
LAZER
hayır
evet
10 sn doldu?
hayır
Kırmızıya geçiş?
evet


YEŞİL
KIRMIZI
Kırmızı uyarı verildi?
hayır
evet
Sarıya geçildi?
evet
SARI
hayır
10 sn doldu?
hayır
evet
Güvenlik güçlerine haber ver

create_clock -period 10.000 -waveform {0.000 5.000} [get_ports clk]

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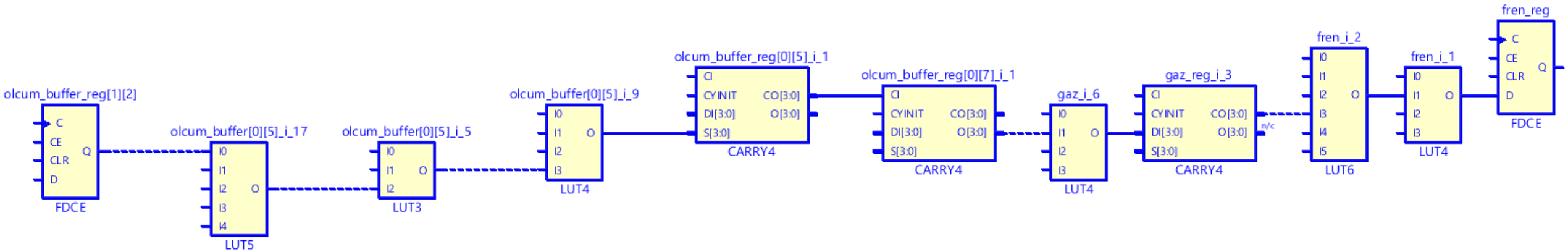
Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	3.075 ns	Worst Hold Slack (WHS):	0.146 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	50	Total Number of Endpoints:	50	Total Number of Endpoints:	48

All user specified timing constraints are met.



Summary

Name	Path 1
Slack	3.075ns
Source	olcum_buffer_reg[1][2]/C (rising edge-triggered cell FDCE clocked by clk {rise@0.000ns fall@5.000ns period=10.000ns})
Destination	fren_reg/D (rising edge-triggered cell FDCE clocked by clk {rise@0.000ns fall@5.000ns period=10.000ns})
Path Group	clk
Path Type	Setup (Max at Slow Process Corner)
Requirement	10.000ns (clk rise@10.000ns - clk rise@0.000ns)
Data Path Delay	6.774ns (logic 2.974ns (43.903%) route 3.800ns (56.097%))
Logic Levels	9 (CARRY4=3 LUT3=1 LUT4=3 LUT5=1 LUT6=1)
Clock Path Skew	-0.145ns
Clock U...tainty	0.035ns

Source Clock Path

Delay Type	Incr (ns)	Path (ns)	Location	Netlist Resource(s)
(clock clk rise edge)	(r) 0.000	0.000		
	(r) 0.000	0.000		clk
net (fo=0)	0.000	0.000		clk
				clk_IBUF_inst/I
IBUF (Prop_ibuf_I_O)	(r) 0.923	0.923		clk_IBUF_inst/O
net (fo=1, unplaced)	0.800	1.722		clk_IBUF
				clk_IBUF_BUFG_inst/I
BUFG (Prop_bufg_I_O)	(r) 0.096	1.818		clk_IBUF_BUFG_inst/O
net (fo=47, unplaced)	0.584	2.402		clk_IBUF_BUFG
FDCE				olcum_buffer_reg[1][2]/C

Data Path

Delay Type	Incr (ns)	Path ...	Loca...	Netlist Resource(s)
FDCE (Prop_fdce_C_Q)	(r) 0.456	2.858		olcum_buffer_reg[1][2]/Q
net (fo=3, unplaced)	0.824	3.682		olcum_buffer_reg[1][2]
				olcum_buffer[0][5]_i_17/I0
LUT5 (Prop_lut5_I0_O)	(r) 0.323	4.005		olcum_buffer[0][5]_i_17/O
net (fo=2, unplaced)	0.460	4.465		olcum_buffer[0][5]_i_17_n_0
				olcum_buffer[0][5]_i_5/I2
LUT3 (Prop_lut3_I2_O)	(r) 0.117	4.582		olcum_buffer[0][5]_i_5/O
net (fo=2, unplaced)	0.643	5.225		olcum_buffer[0][5]_i_5_n_0
				olcum_buffer[0][5]_i_9/I3
LUT4 (Prop_lut4_I3_O)	(r) 0.332	5.557		olcum_buffer[0][5]_i_9/O
net (fo=1, unplaced)	0.000	5.557		olcum_buffer[0][5]_i_9_n_0
				olcum_buffer_reg[0][5]_i_1/S[0]
CARRY4 (Prop_c...4_S[0]_CO[3])	(r) 0.532	6.089		olcum_buffer_reg[0][5]_i_1/CO[3]
net (fo=1, unplaced)	0.000	6.089		olcum_buffer_reg[0][5]_i_1_n_0
				olcum_buffer_reg[0][7]_i_1/CI
CARRY4 (Prop_carry4_CI_O[0])	(f) 0.235	6.324		olcum_buffer_reg[0][7]_i_1/O[0]
net (fo=3, unplaced)	0.488	6.812		gaz3[8]
				gaz_i_6/I1
LUT4 (Prop_lut4_I1_O)	(r) 0.320	7.132		gaz_i_6/O
net (fo=1, unplaced)	0.000	7.132		gaz_i_6_n_0
				gaz_reg_i_3/DI[3]
CARRY4 (Prop_c...4_DI[3]_CO[3])	(r) 0.411	7.543		gaz_reg_i_3/CO[3]
net (fo=3, unplaced)	0.936	8.479		gaz1
				fren_i_2/I3
LUT6 (Prop_lut6_I3_O)	(r) 0.124	8.603		fren_i_2/O
net (fo=1, unplaced)	0.449	9.052		fren_i_2_n_0
				fren_i_1/I1
LUT4 (Prop_lut4_I1_O)	(r) 0.124	9.176		fren_i_1/O
net (fo=1, unplaced)	0.000	9.176		fren1_out
FDCE				fren_reg/D
Arrival Time		9.176		

Destination Clock Path

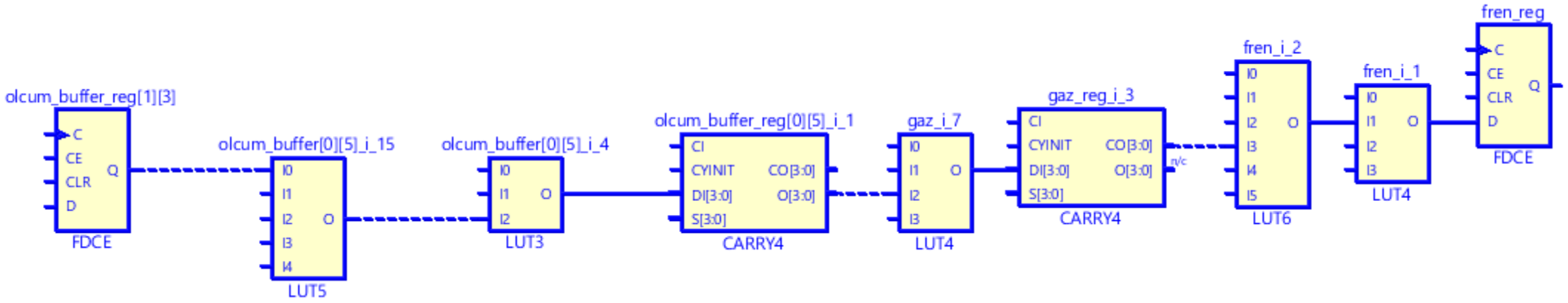
Delay Type	Incr (ns)	Path (...	Loca...	Netlist Resource(s)
(clock clk rise edge)	(r) 10.000	10.000		
	(r) 0.000	10.000		clk
net (fo=0)	0.000	10.000		clk
				clk_IBUF_inst/I
IBUF (Prop_ibuf_I_O)	(r) 0.789	10.789		clk_IBUF_inst/O
net (fo=1, unplaced)	0.760	11.549		clk_IBUF
				clk_IBUF_BUFG_inst/I
BUFG (Prop_bufg_I_O)	(r) 0.091	11.640		clk_IBUF_BUFG_inst/O
net (fo=47, unplaced)	0.439	12.079		clk_IBUF_BUFG
FDCE				fren_reg/C
clock pessimism	0.178	12.257		
clock uncertainty	-0.035	12.222		
FDCE (Setup_fdce_C_D)	0.029	12.251		fren_reg
Required Time		12.251		

create_clock -period 5.000 -waveform {0.000 2.500} [get_ports clk]

Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	-1.569 ns	Worst Hold Slack (WHS):	0.146 ns	Worst Pulse Width Slack (WPWS):	2.000 ns
Total Negative Slack (TNS):	-3.562 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	3	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	50	Total Number of Endpoints:	50	Total Number of Endpoints:	48

Timing constraints are not met.



Summary

Name	Path 1
Slack	-1.569ns
Source	olcum_buffer_reg[1][3]/C (rising edge-triggered cell FDCE clocked by clk {rise@0.000ns fall@2.500ns period=5.000ns})
Destination	fren_reg/D (rising edge-triggered cell FDCE clocked by clk {rise@0.000ns fall@2.500ns period=5.000ns})
Path Group	clk
Path Type	Setup (Max at Slow Process Corner)
Requirement	5.000ns (clk rise@5.000ns - clk rise@0.000ns)
Data Path Delay	6.418ns (logic 2.467ns (38.439%) route 3.951ns (61.561%))
Logic Levels	7 (CARRY4=2 LUT3=1 LUT4=2 LUT5=1 LUT6=1)
Clock Path Skew	-0.145ns
Clock U...tainty	0.035ns

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Source Clock Path

Delay Type	Incr (ns)	Path (ns)	Location	Netlist Resource(s)
(clock clk rise edge)	(r) 0.000	0.000		
	(r) 0.000	0.000		clk
net (fo=0)	0.000	0.000		clk
				clk_IBUF_inst/I
IBUF (Prop_ibuf_I_O)	(r) 0.923	0.923		clk_IBUF_inst/O
net (fo=1, unplaced)	0.800	1.722		clk_IBUF
				clk_IBUF_BUFG_inst/I
BUFG (Prop_bufg_I_O)	(r) 0.096	1.818		clk_IBUF_BUFG_inst/O
net (fo=47, unplaced)	0.584	2.402		clk_IBUF_BUFG
FDCE				olcum_buffer_reg[1][3]/C

Data Path

Delay Type	Incr (ns)	Path ...	Loca...	Netlist Resource(s)
FDCE (Prop_fdce_C_Q)	(r) 0.456	2.858		olcum_buffer_reg[1][3]/Q
net (fo=3, unplaced)	0.824	3.682		olcum_buffer_reg[1][3]
				olcum_buffer[0][5]_i_15/I0
LUT5 (Prop_lut5_I0_O)	(r) 0.295	3.977		olcum_buffer[0][5]_i_15/O
net (fo=3, unplaced)	0.467	4.444		olcum_buffer[0][5]_i_15_n_0
				olcum_buffer[0][5]_i_4/I2
LUT3 (Prop_lut3_I2_O)	(r) 0.124	4.568		olcum_buffer[0][5]_i_4/O
net (fo=1, unplaced)	0.639	5.207		olcum_buffer[0][5]_i_4_n_0
				olcum_buffer_reg[0][5]_i_1/DI[1]
CARRY4 (Prop_carry4_DI[1]_O[3])	(f) 0.614	5.821		olcum_buffer_reg[0][5]_i_1/O[3]
net (fo=3, unplaced)	0.636	6.457		gaz3[7]
				gaz_i_7/I2
LUT4 (Prop_lut4_I2_O)	(r) 0.303	6.760		gaz_i_7/O
net (fo=1, unplaced)	0.000	6.760		gaz_i_7_n_0
				gaz_reg_i_3/DI[2]
CARRY4 (Prop_c...4_DI[2]_CO[3])	(r) 0.427	7.187		gaz_reg_i_3/CO[3]
net (fo=3, unplaced)	0.936	8.123		gaz1
				fren_i_2/I3
LUT6 (Prop_lut6_I3_O)	(r) 0.124	8.247		fren_i_2/O
net (fo=1, unplaced)	0.449	8.696		fren_i_2_n_0
				fren_i_1/I1
LUT4 (Prop_lut4_I1_O)	(r) 0.124	8.820		fren_i_1/O
net (fo=1, unplaced)	0.000	8.820		fren1_out
FDCE				fren_reg/D
Arrival Time		8.820		

Destination Clock Path

Delay Type	Incr (ns)	Path ...	Loca...	Netlist Resource(s)
(clock clk rise edge)	(r) 5.000	5.000		
	(r) 0.000	5.000		clk
net (fo=0)	0.000	5.000		clk
				clk_IBUF_inst/I
IBUF (Prop_ibuf_I_O)	(r) 0.789	5.789		clk_IBUF_inst/O
net (fo=1, unplaced)	0.760	6.549		clk_IBUF
				clk_IBUF_BUFG_inst/I
BUFG (Prop_bufg_I_O)	(r) 0.091	6.640		clk_IBUF_BUFG_inst/O
net (fo=47, unplaced)	0.439	7.079		clk_IBUF_BUFG
FDCE				fren_reg/C
clock pessimism	0.178	7.257		
clock uncertainty	-0.035	7.222		
FDCE (Setup_fdce_C_D)	0.029	7.251		fren_reg
Required Time		7.251		