Title		
PlutoV2 Schematic		
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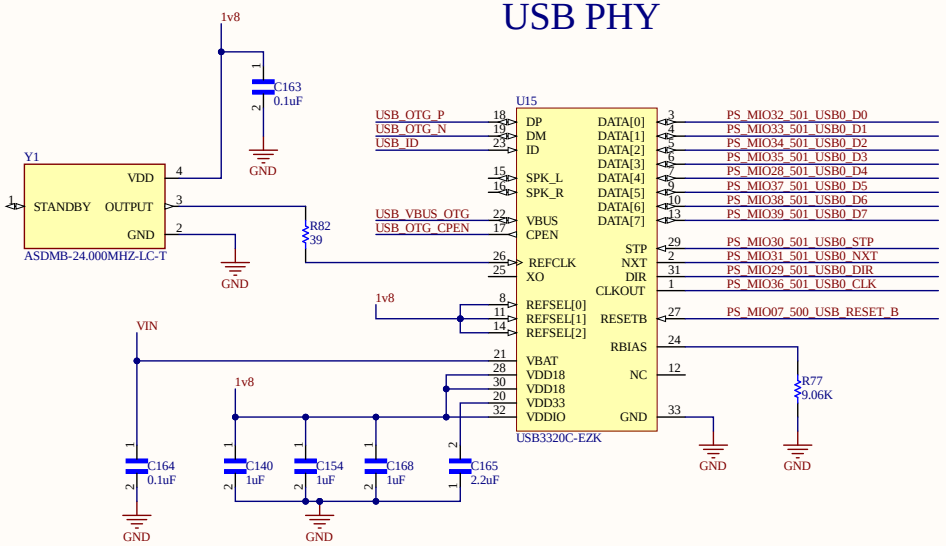
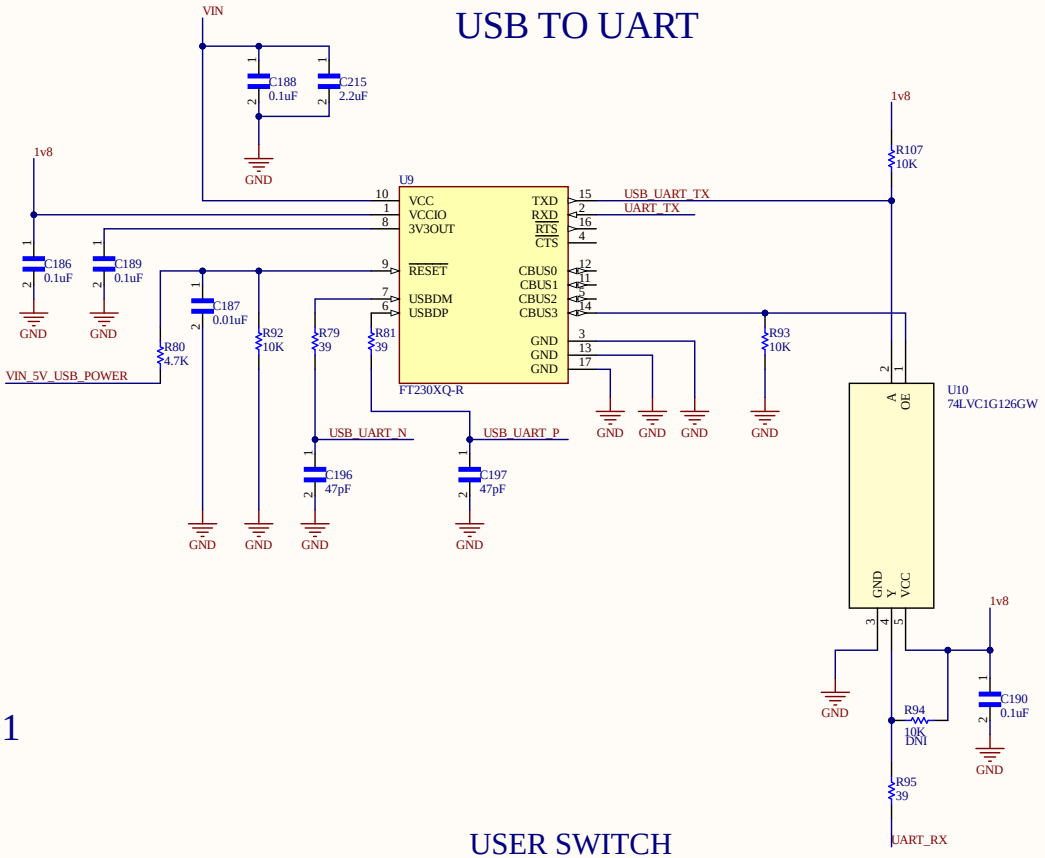
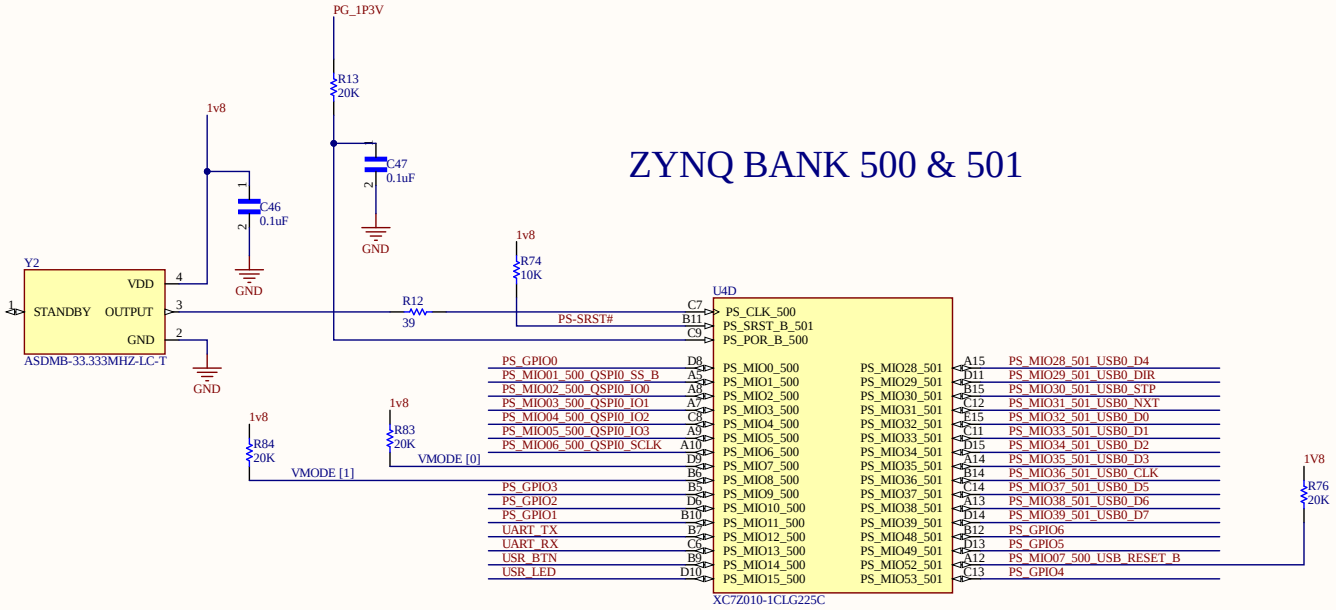
USB PHY



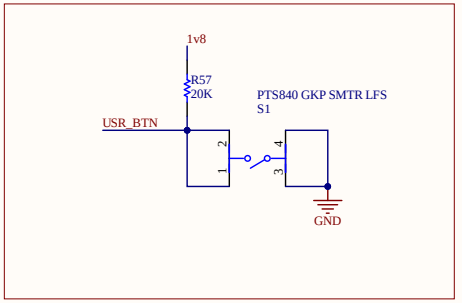
USB TO UART



ZYNQ BANK 500 & 501



USER SWITCH



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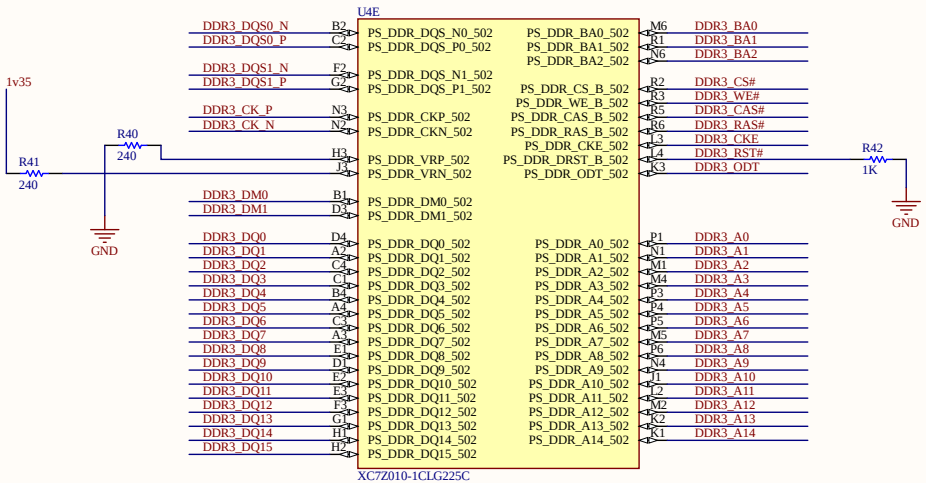
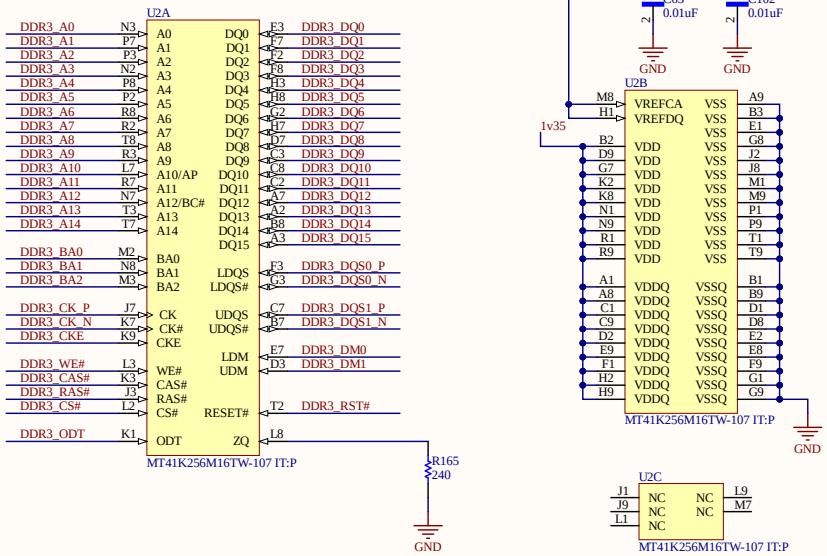
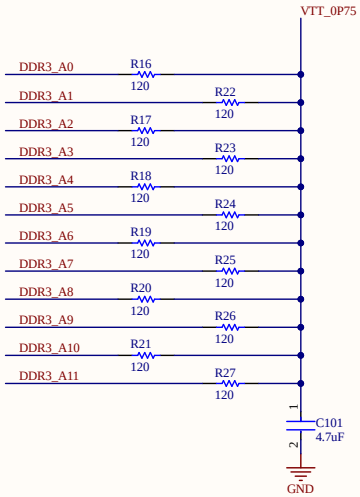
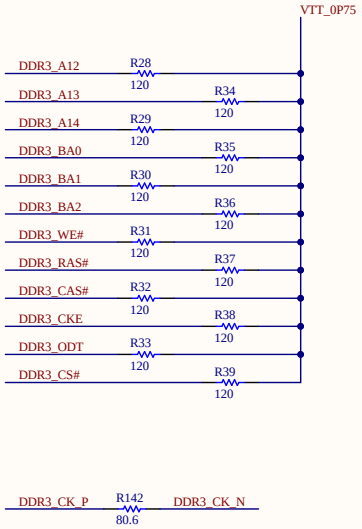
ZYNQ BANK 502 DDR3



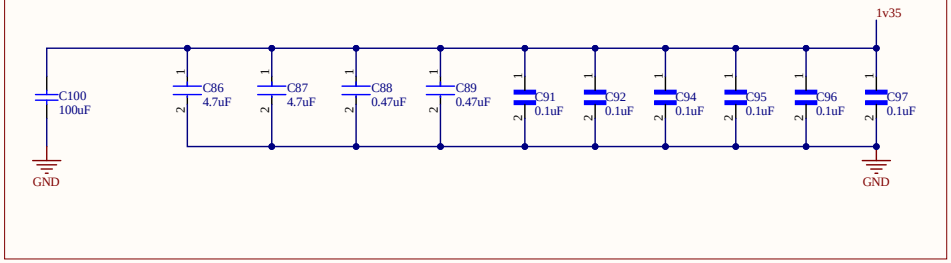
DDR3



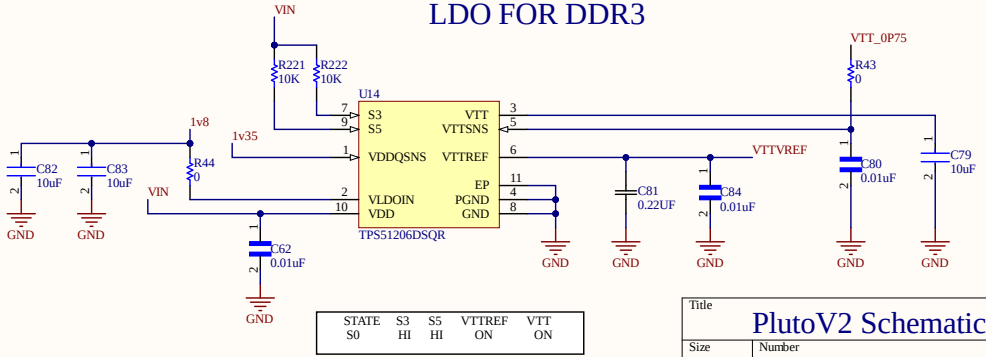




DDR3 DECOUPLING - PLACE NEAR DDR3



LDO FOR DDR3



STATE	S3	S5	VTTREF	VTT
S0	HI	HI	ON	ON

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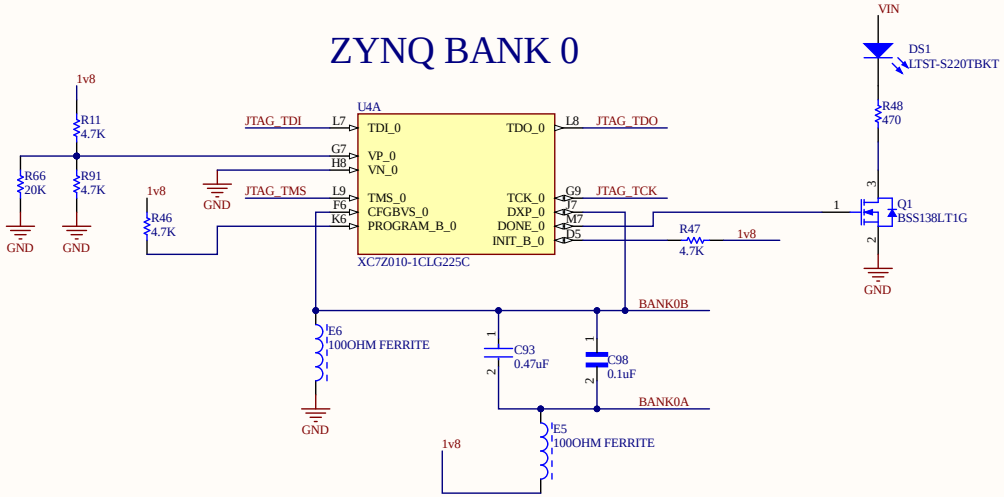
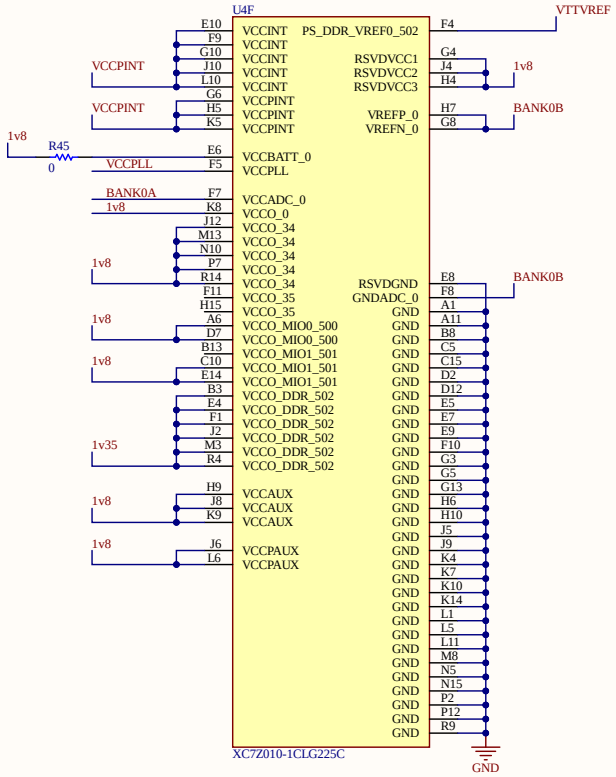
NOTE CHANGE LED PACKAGE

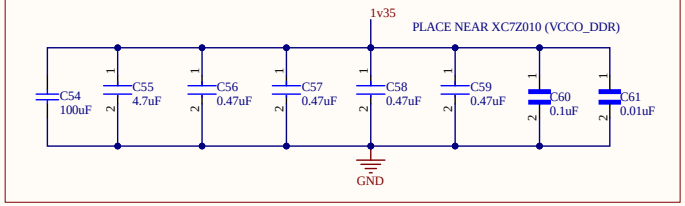
ZYNQ BANK 0



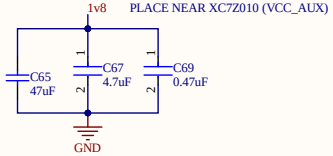
ZYNQ POWER



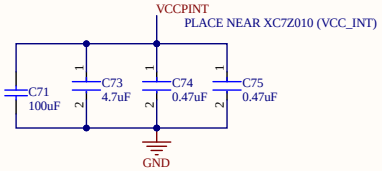
VCCO DDR DECOUPLING



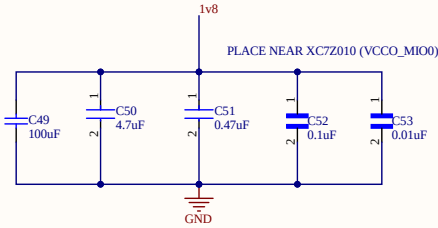
VCC AUX DECOUPLING



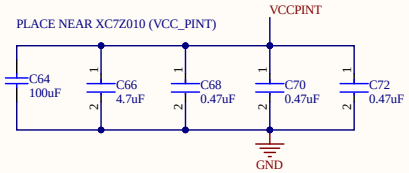
VCC INT DECOUPLING



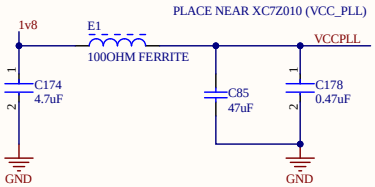
VCCO PAUX DECOUPLING



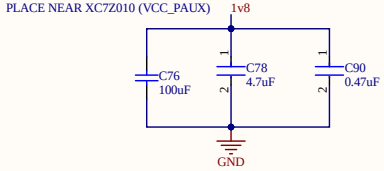
VCC PINT DECOUPLING



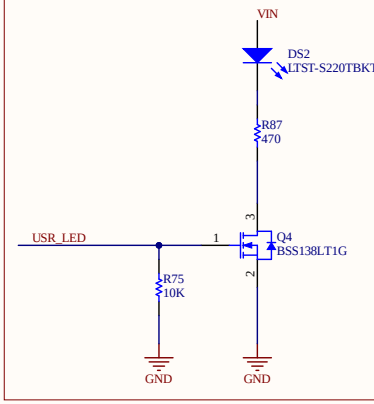
VCC PLL FILTERING



VCC PAUX DECOUPLING



NOTE CHANGE LED PACKAGE



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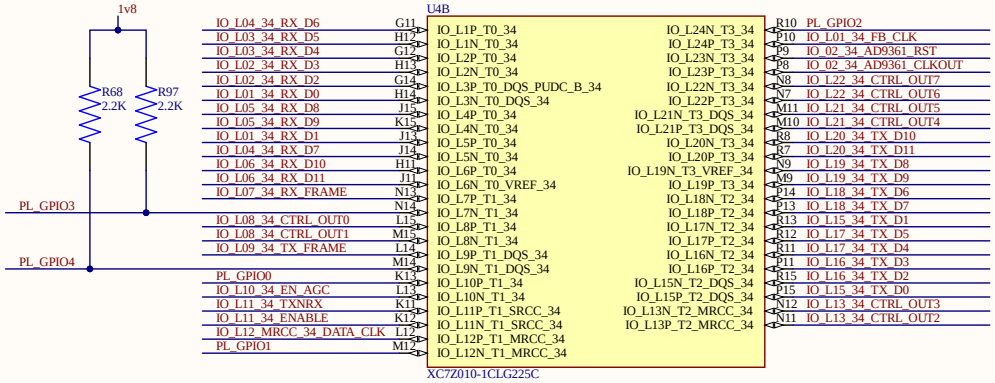
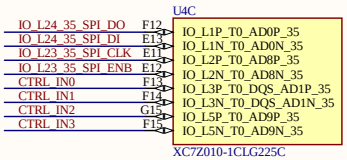
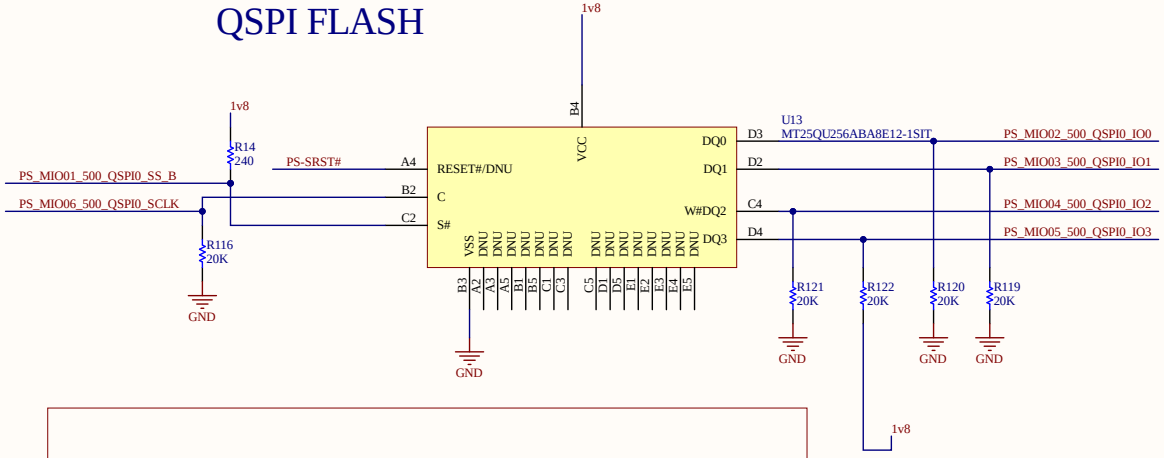
ZYNQ BANK 35



ZYNQ BANK 35



QSPI FLASH



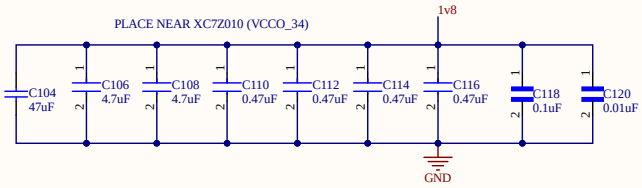
BOOT MODE	MIO5	MIO4
CASCADED JTAG	0	0
QSPI	1	0

MIO5 CAN BE SHORTED TO GND BY INSERTING A JUMPER ON THE JTAG ADAPTER

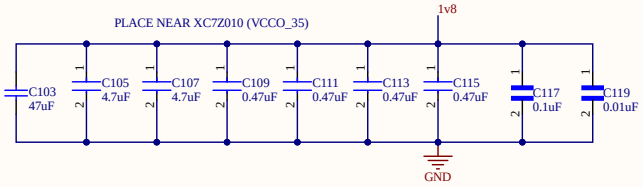
WHEN USING THE ADAPTER, AND WANTING TO HAVE JTAG BOOT (DEVICE DOESN'T BOOT U-BOOT, OR KERNEL):

- INSERT THE JUMPER ON THE ADAPTER (JTAG BOOT)ext
- POWER UP PLUTO
- REMOVE THE JUMPER ON THE ADAPTER, SO YOU CAN TALK TO THE SPI FLASH
- DEBUG AS NORMAL.

ZYNQ BANK 34 DECOUPLING



ZYNQ BANK 35 DECOUPLING



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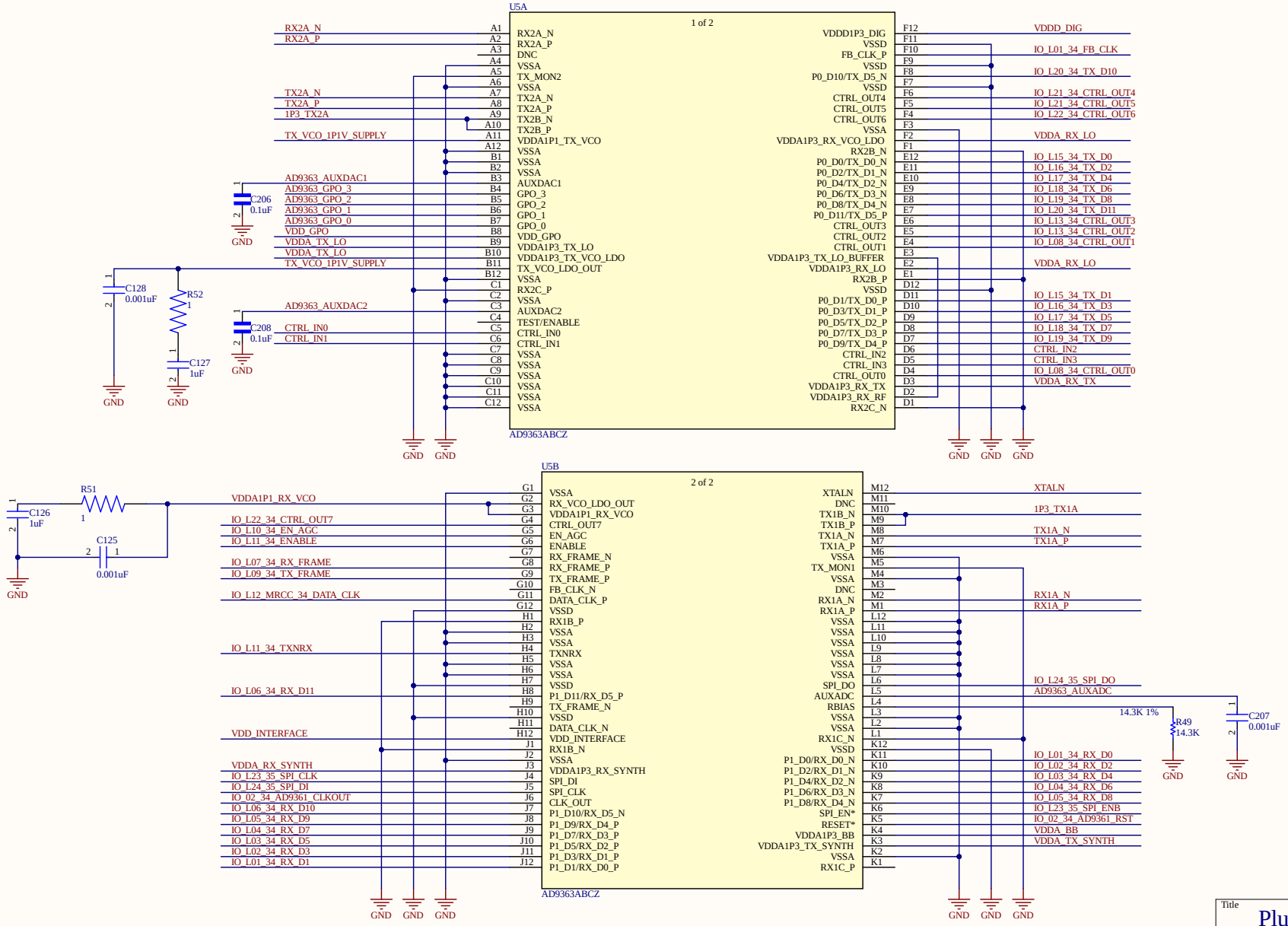
AD9363



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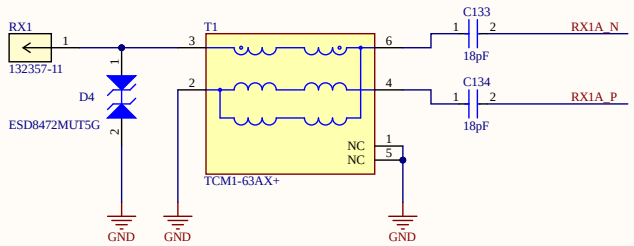
File: D:\EEET 2022\..\AD9363.SchDoc		Drawn By: R.Pender

RF FRONTEND

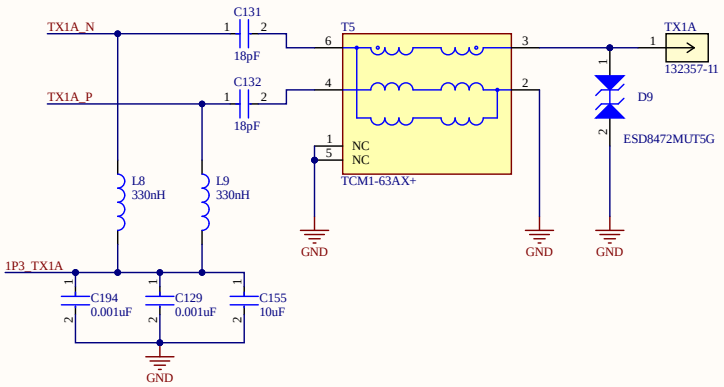
ADD RECEIVER LNA IF REQUIRED

RX SMA CONNECTOR

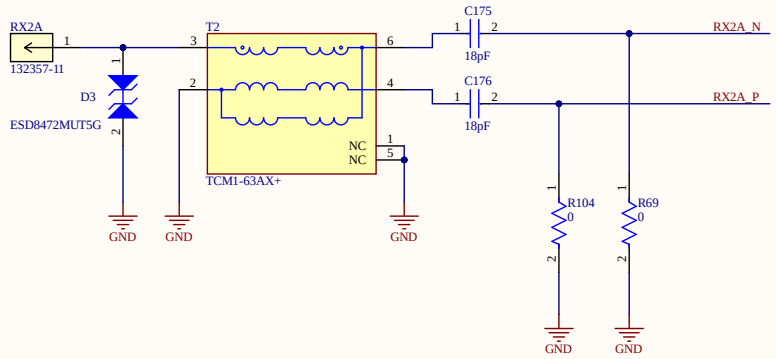


ADD TRANSMITTER PA IF REQUIRED

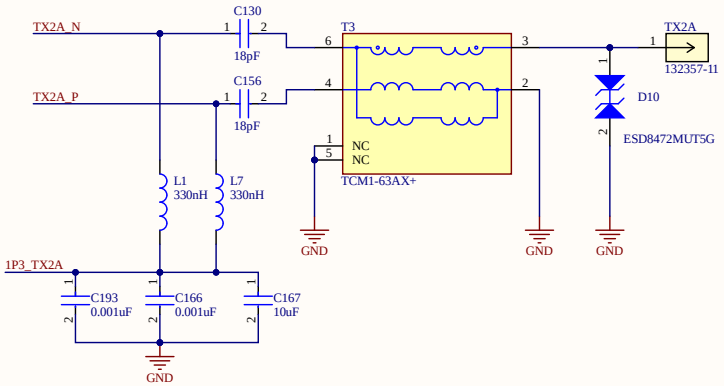
TX SMA CONNECTOR



RX U.FL CONNECTOR



TX U.FL CONNECTOR



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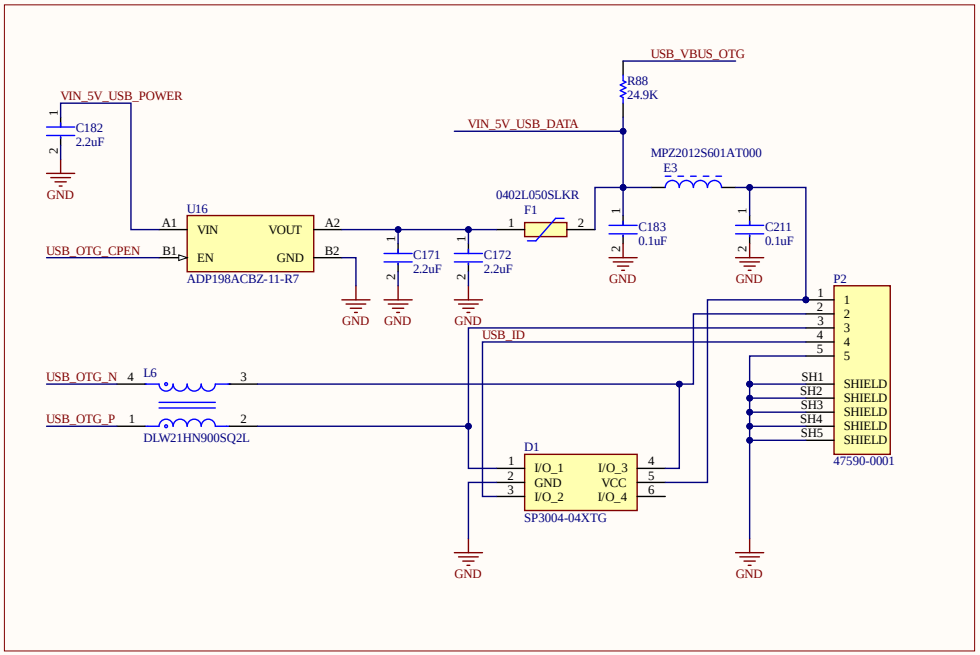
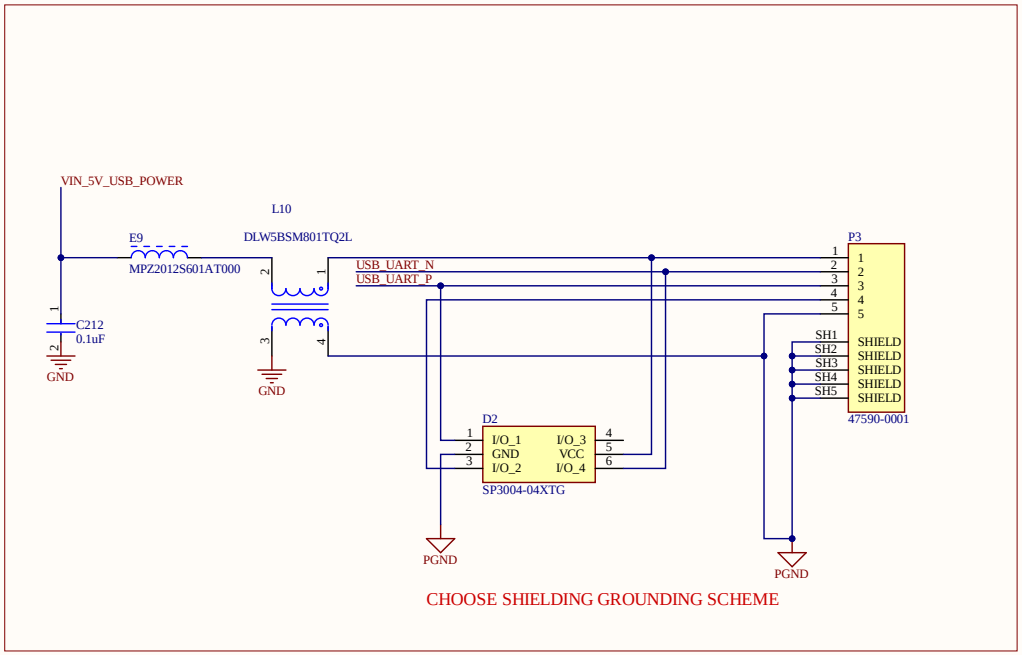
USB CONNECTORS

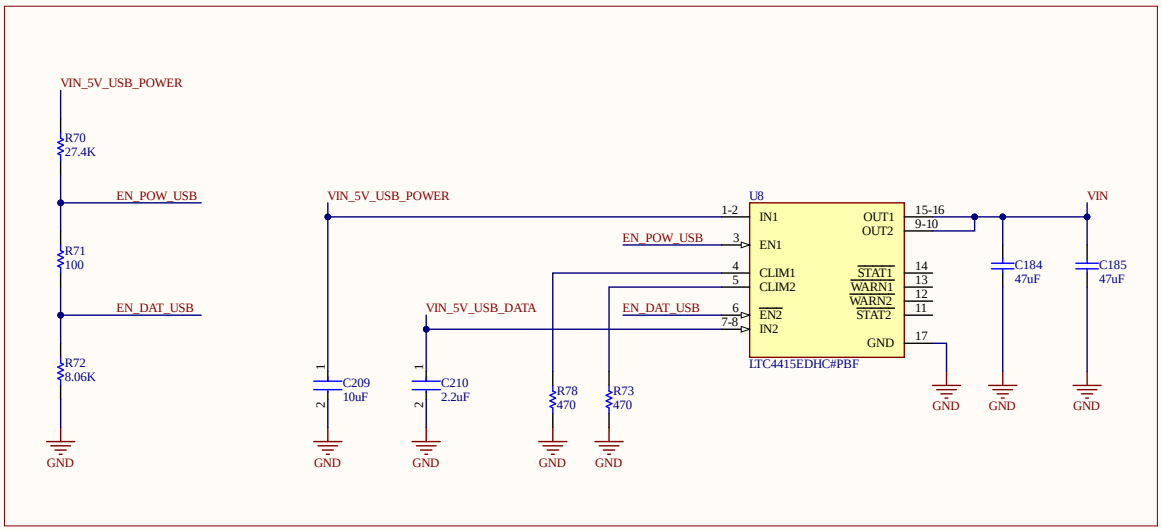
USB OTG



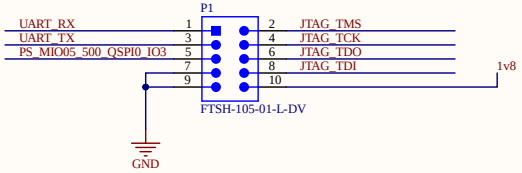
USB POWER ONLY



USB POWER SELECTOR



0.05 PITCH JTAG AND UART CONNECTOR



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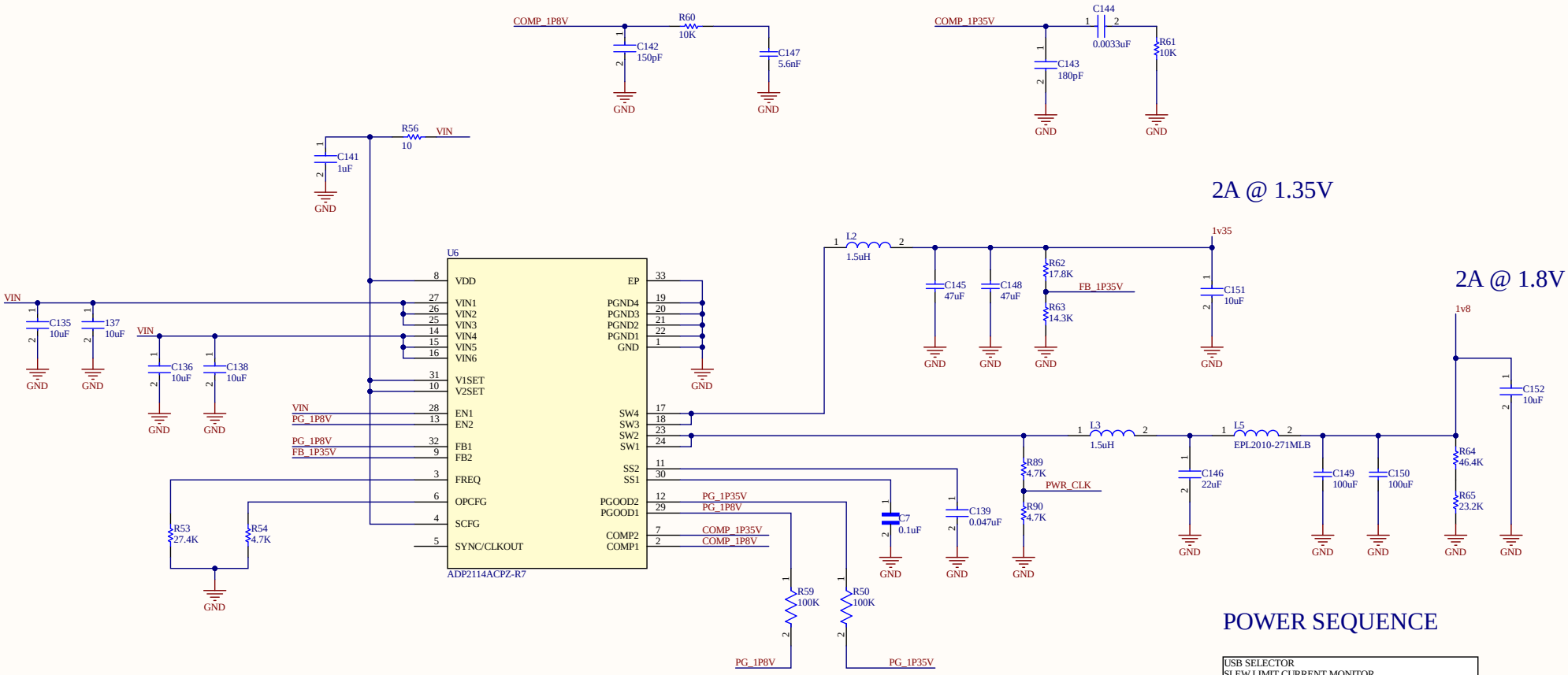
1.35V & 1.8V SUPPLY



POWER SEQUENCE

USB SELECTOR
SLEW LIMIT CURRENT MONITOR

1ST. 1V0
PS: VCCPINT
PL: VCCINT
AD9363: ---

2ND. 1V8 AND 1V3
PS: VCCPAUX, VCC_PLL, VCCO_MIO0, VCC_MIO1
PL: VCCAUX, VCCO_0, VCC0_34, VCCO_35
AD9363: VDD_INTERFACE (1V8), RF (1V3)

3RD. 1V35
PS: VCCO_DDR
PL: ---
AD9363: ---

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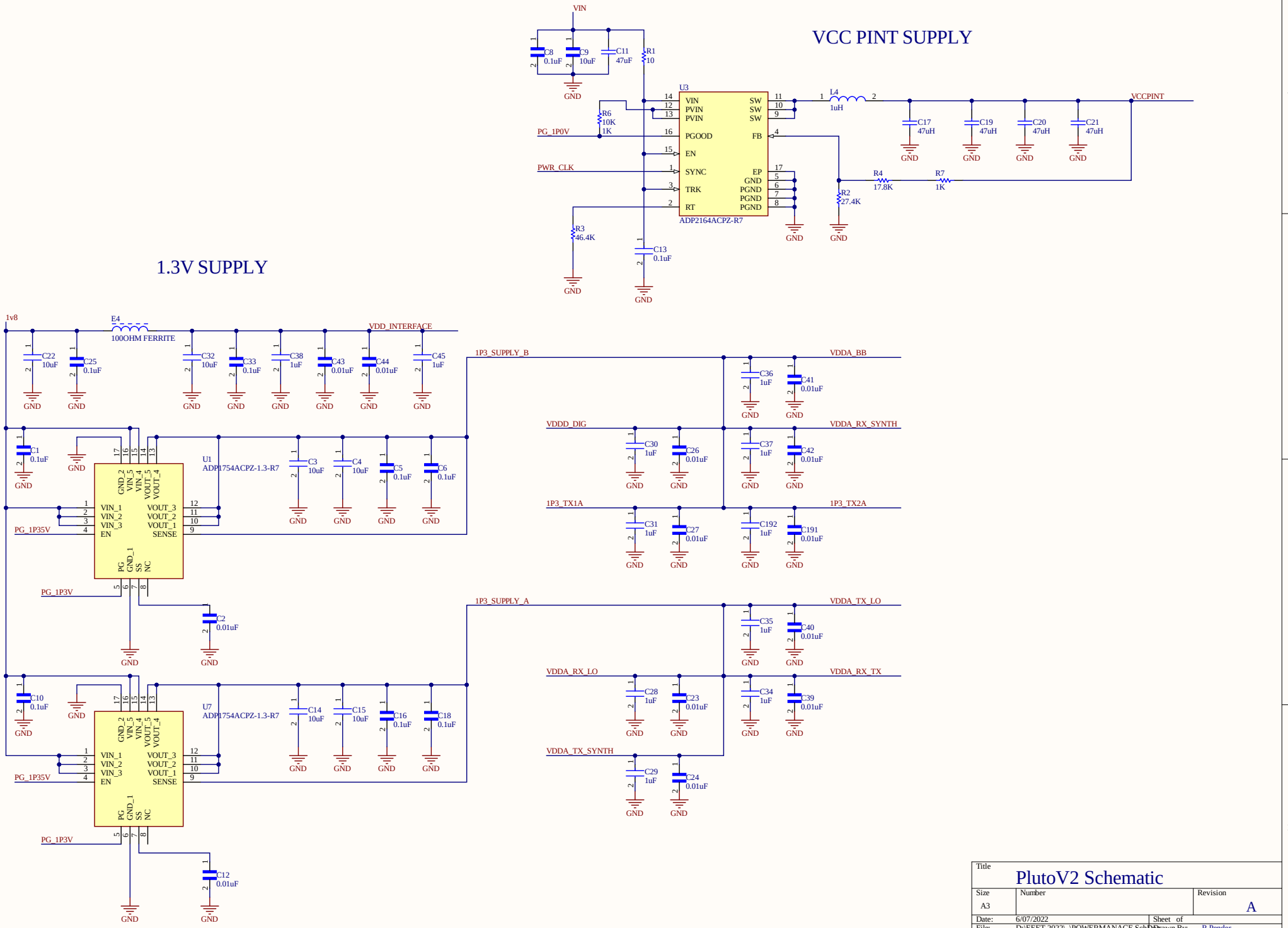

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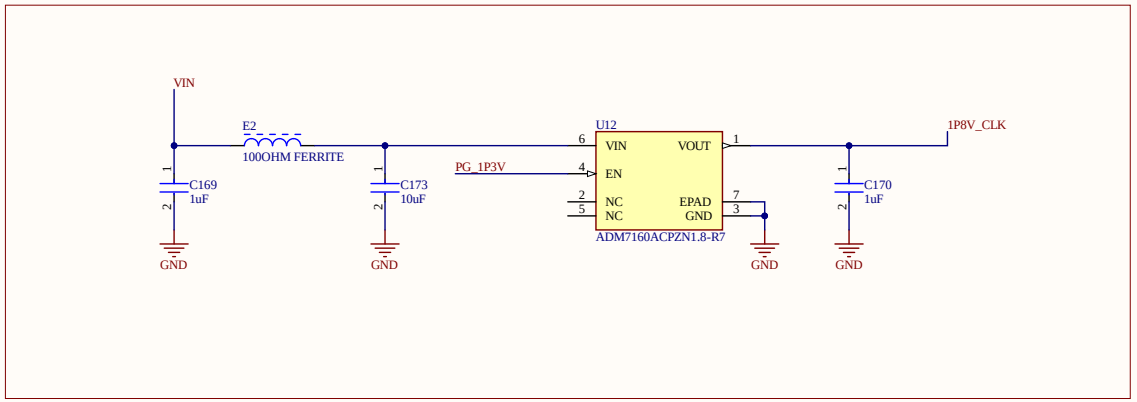
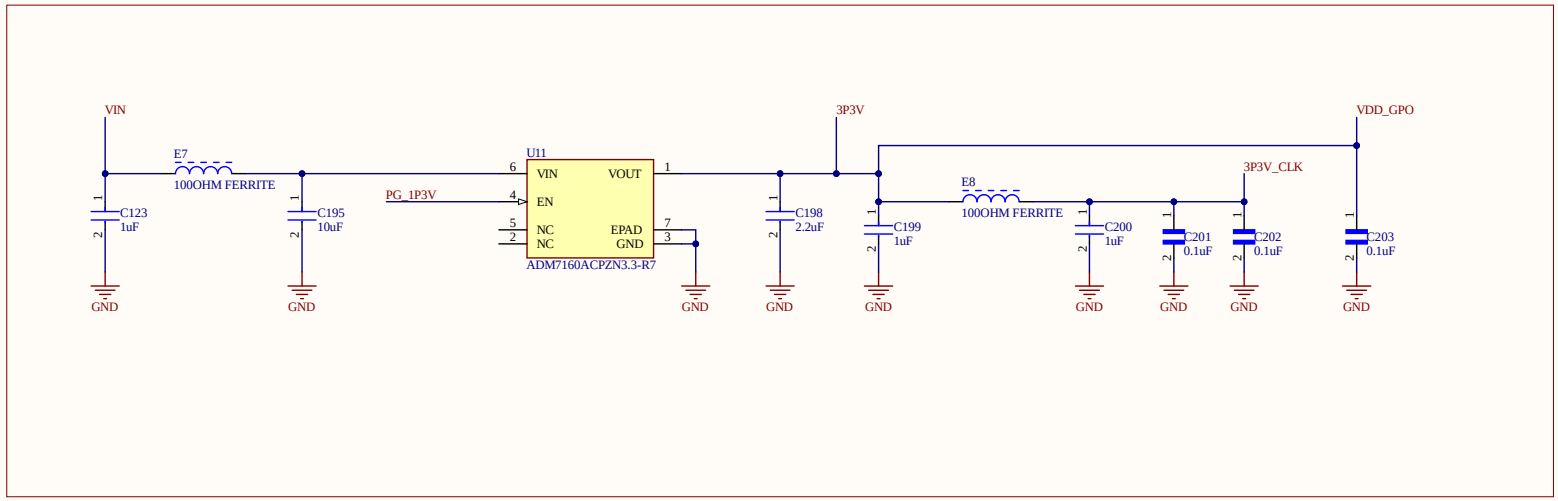
CLK 1.8V SUPPLY



3.3V SUPPLY



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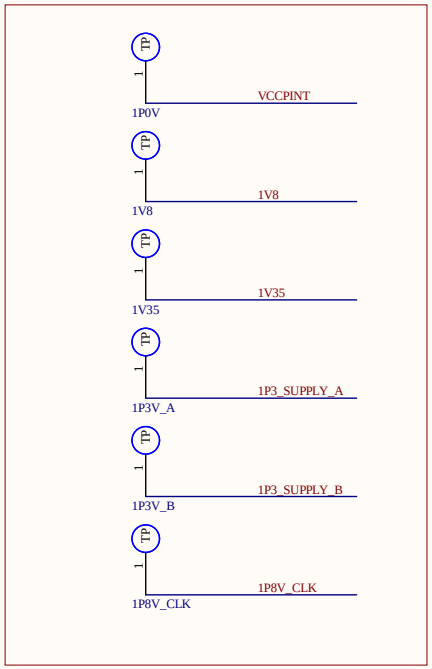
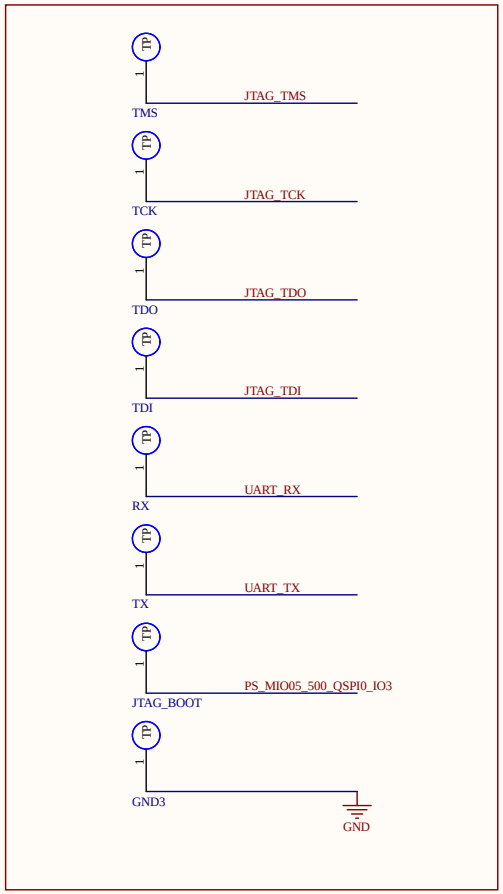
TEST POINTS

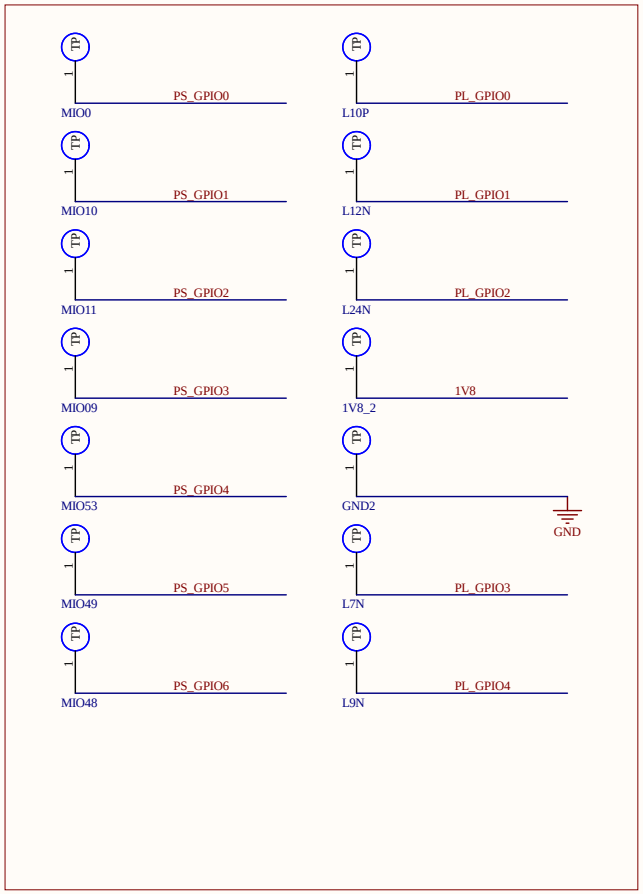
POWER TEST



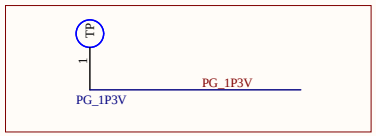
JTAG & UART



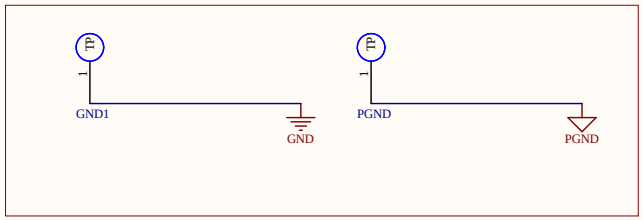
ZYNQ



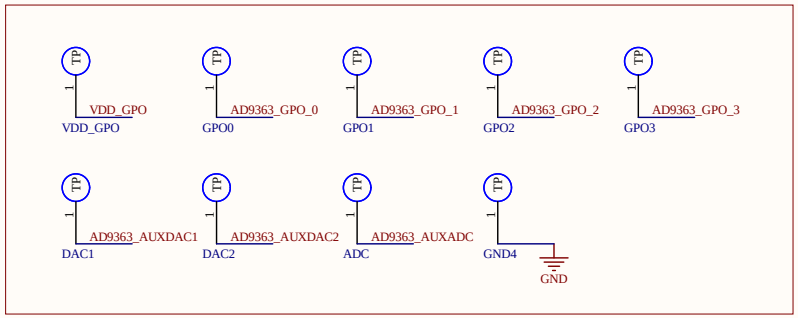
RESET ZYNQ



GROUND



AD9363



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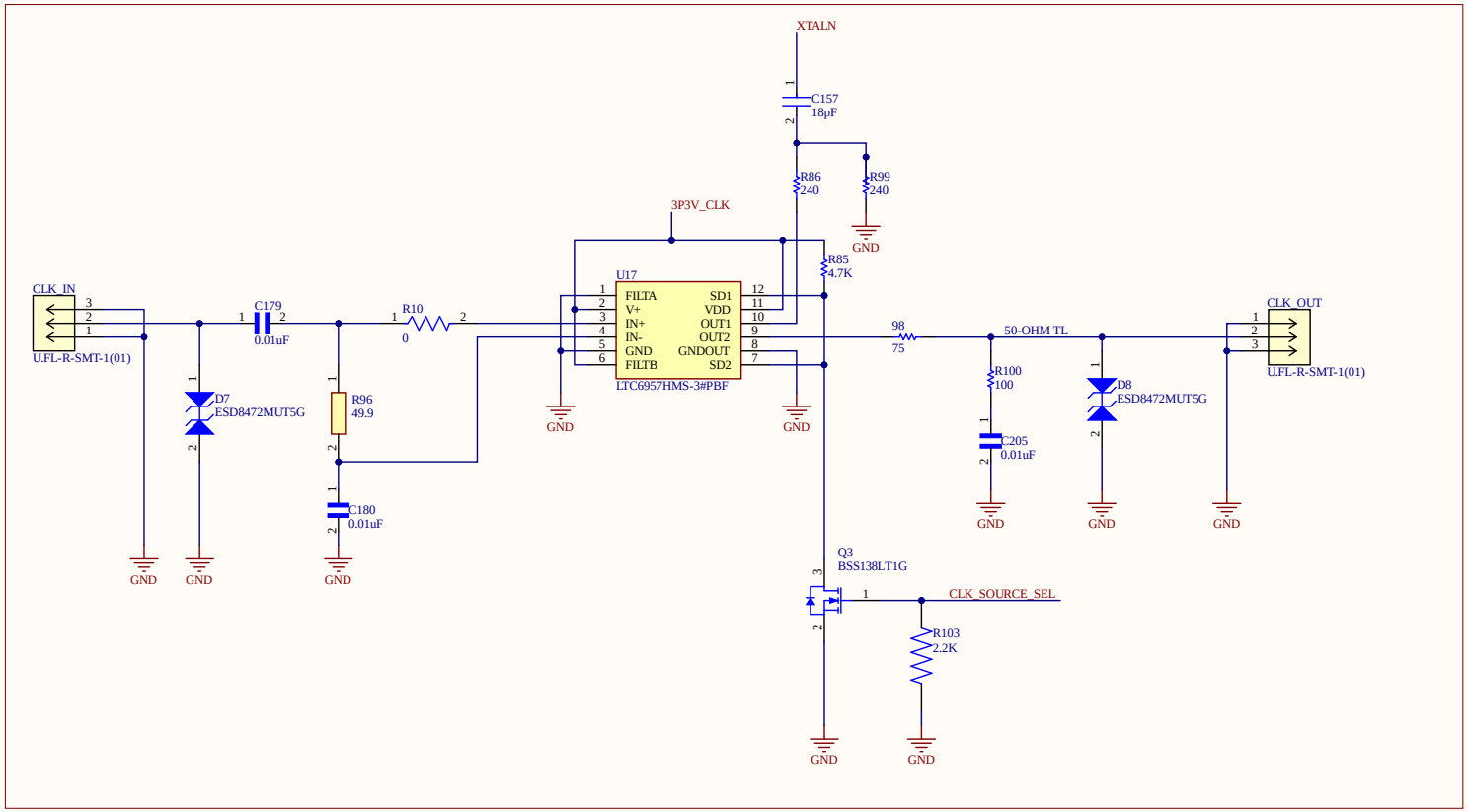
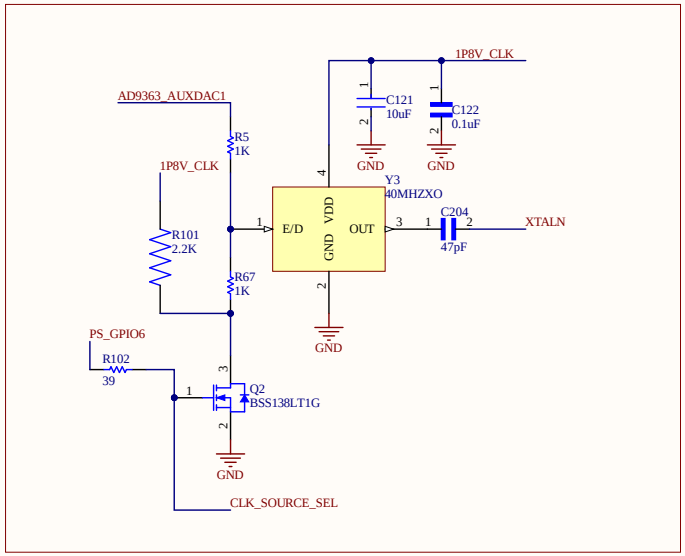
AD9363 EXTERNAL CLK



AD9363 XO



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Board Stack Report