Berk İhsan METİN

I'm a Junior Digital Design Engineer (Electronics Engineer). So far I worked mainly on military projects, and I'm getting experienced in the field of communication systems at my current employment in Turkey. I'm looking forward to a new opportunities worldwide.

Personal Information

Residence Address: Maltepe, Istanbul/Turkey
Date of Birth: 07 October 1998
Nationality: Turkish

Contact Information

Email: berkihsanmetin@outlook.com
Phone: +90 552 233 5864
Linkedin: linkedin.com/in/berkihsanmetin

Education

2016-2021

Sabanci University I Istanbul,Turkey

Bachelor of Science Electronics Engineering

Education Language: English

Work Experiences

CTech Information Technologies Inc. I Technopark Istanbul

Digital Design Engineer | Full Time | 18 May 2022 - Current

Company Description

CTech is subsidiary of Turkish Aerospace Industries (TAI) which develops and produce products for the industry for the fields like aerospace, military defense, security, information and communication.

Responsibilities

- Working as Digital Design Engineer which are developed on FPGA and SoC.
- Making RTL implementation of digital communication algorithms with VHDL which is developed by communication team or already existed in literature standards such as DVB-S2. I am currently working on a LOS modem project that is runing on Xilinx Ultrazed+ SOM board.

Pavelsis Avionics I Technopark Istanbul

Digital Design Engineer | Contracted | 10 Nov 2021 - 28 Feb 2022

Company Description

Pavelsis is the spinoff company of PAVOTEK, which has been designing and producing electronic products, mostly avionics for military defense industry such as ASELSAN, TAI, ROKETSAN.

Responsibilities

• Worked as Digital Design Engineer in avionics projects developed for the Turkish Defense Industry.
• Developed RTL designs by using VHDL on XILINX Vivado platform and tested them on XILINX's evaluation boards, then on PCB boards that are developed by the company.,
• Worked with AC701, VCU128, HTG930 and BASYS3 boards.

Internship Experiences

Yongatek Microelectronics I Technopark Istanbul

Digital Design | Intern | 15 Jun 2020 - 15 Sep 2020

Company Description

Yongatek Microelectronics provide a wide range of IC/ASIC/FPGA/SoC/Chip Design, 5G/6G and Satellite Communications,

Responsibilities

• Learning VHDL Syntax.
• Research on noise reduction filters and testing them on Matlab.
• RTL design of 3x3 median filter with high throughput by using VHDL on XILINX ISE platform.

Freelance Experience

QoreHub.com I Turkey

Founder | Freelance | 01 Apr 2022 - Current

QoreHub is a website that emerged by seeing the scarcity of Turkish resources in our country as a problem. People can easily access technical information in Turkish/English. They can take advantage of free resources at their workplace or university.

Skills & Expertise

Programming Languages
VHDL | Verilog HDL | Java
Design and Simulation Tools
Xilinx Vivado | Xilinx ISE | ModelSim | Cadence Virtuoso | Cadence Innovus | Synopsys DC
Software Tools
MATLAB | Git | Android Studio
Lab Equipments
Oscilloscope | Function Generator | Multimeter

Exams

TOEFL IBT | 89

Worldwide accepted English exam which is organized by ETS Global.

Volunteer Projects & Activities

- **AIESEC Global Volunteer Project** July 2018 - September 2018 | Timisoara, Romania

Participated in AIESEC Volunteer Project, and English education has given to children in weekdays with group of 4 in a kindergarten which is needy.

- **Civic Involvement Project** Fabruary 2017 - June 2017 | Sabanci University

Given some social education such as environmental consciousness to the about 9 years old primary school children one day per week. Worked as a group of 2 or 3 for every class. Plans and the evaluations are done at meetings every week.

- **University Clubs** September 2016 - June 2018 | Sabanci University

~ *Active Member*, Tea Talks with CEO's Club (2016, 2017)
~ *Member*, IEEE Engineering Society (2016, 2018)
~ *Member*, Industrial Engineers Club (2016, 2018)

Certificates

- **Advanced VHDL for Verification | Udemy**
- **Learning FPGA Development | LinkedIn Learning**
- **Android Mobile Application Development Course: Java | Udemy**

Other Information

Driving Licence
B

Compulsory Military Service
Postponed until September 2023, duration will be 28 days (paid military service)

Projects

CTech:

- Scrambler - Bit Interleaver - Bit Mapper for DVB-S2 Encoder.
- DVB-S2 FEC Encoder with Scrambler, BCH Encoder, LDPC Encoder, Bit Interleaver, Bit Mapper (BCH and LDPC Encoder modules are written by other teammates).
- DVB-S2 FEC Encoder and Decoder Loopback tests by creating block design and sending configuration information over ZYNQ processor by using Xilinx Vitis platform.
- Implementing OFDM algorithms with USRP B210 Device and MATLAB (Not finished).

Pavelsis:

- Converting finished Ethernet Layer 3 Switch project on FPGA to Ethernet Layer 2 Switch. (Project was Shelved).
- SPI, RS422-RS232-RS485 controllers and packet parsers designed with VHDL and tested on Artix-7.

Yongatek:

- Researching noise types, reduction algorithms and filters at digital image processing were researched.
- Filters were coded and implemented at MATLAB, such as median and gaussian filters, to found out the most appropriate filters for provided video by company.
- RTL design of “3x3 Median Filter” with high throughput, was finished by using VHDL and full match between MATLAB results and RTL results was provided.

Sabanci University

- Op-Amp Design: Designed both schematic and layout at Cadence Virtuoso with specifications: PSRR, CMRR, PM and Gain.
- Full Custom Inverter and NAND2 gates: Designed both schematic and layout at Cadence Virtuoso with specifications: propagation delay, rise time and fall times.
- Square Root Carry Select Adder and Kogge Stone Adder: Designed by using Verilog HDL and tested in ModelSim. Then synthesized with Synopsys Design Compiler. Physical Layout of these adders were done by using Cadence Innovus platform.
- Sobel Edge Detector: Coded by using Verilog HDL.
- Smoothening, Edge Detection, Sharpening, Line Detection, Corner Detection and Optical Flow Algorithms: Implemented by using MATLAB.
- Hodgkin-Huxley model is simulated and tested in MATLAB. R-wave detector circuit for ECG signal designed at LTSpice platform. 2-lead ECG wave circuit implemented on breadboard and tested on different volunteers.

Reference

Available upon request.