CS224
Section No.: 01
Spring 2021
Lab No.: 06
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1. (5 points: With 3 or more errors you get 0 points. Otherwise full point.) Fill in the empty cells of the following table. Assume that the main memory size is 0.5 GB. Index Size: No. of bits needed to express the set number in an address, Block Offset: No. of bits needed to indicate the word offset in a block, Byte Offset: No. of bits needed to indicate the byte offset in a word. Block Replacement Policy Needed: Indicate if a block replacement policy such as FIFO, LRU, LFU (Least Frequently Used) etc. is needed (yes) or not (no). If some combinations are not possible mark them.

Since memory is 0.5 gigabytes it is 2^{29}, address is 29 bits

No.	Cache Size KB	N way cache	Word Size in bits	Block size (no. of words)	No. of Sets	Tag Size in bits	Index Size (Set No.) in bits	Word Block Offset Size in bits	Byte Offset Size in bits	Block Replacement Policy Needed (Yes/No)
1	**8**	**1**	**8**	**8**	1024	16	10	3	0	No
2	**8**	**2**	**16**	**8**	256	17	8	3	1	Yes
3	**8**	**4**	**16**	**4**	256	18	8	2	1	Yes
4	**8**	**Full**	**16**	**4**	1	26	0	2	1	Yes
9	**32**	**1**	**16**	**2**	8192	14	13	1	1	No
10	**32**	**2**	**16**	**2**	4096	15	12	1	1	Yes
11	**32**	**4**	**8**	**8**	1024	16	10	3	0	Yes
12	**32**	**Full**	**8**	**8**	1	26	0	3	0	Yes

2. (5 points: With 3 or more errors you get 0 points. Otherwise full point.) Consider the following MIPS code segment. (Remember MIPS memory size is 4 GB.) Cache capacity is 8 words, Block size: 4 words, N= 1.

```
        addi $t0, $0, 5
loop:   beq $t0, $0, done
        lw $t1, 0xA4($0)
        lw $t2, 0xA8($0)
        lw $t3, 0xAC($0)
         addi $t0, $t0, -1
         j loop
 done:
```

a. In the following table indicate the type of miss, if any: Compulsory, Conflict, Capacity.

Instruction	Iteration No				
	1	2	3	4	5
lw $t1, 0xA4($0)	Compulsory	Hit	Hit	Hit	Hit
lw $t2, 0xA8($0)	Hit	Hit	Hit	Hit	Hit
lw $t3, 0xAC($0)	Hit	Hit	Hit	Hit	Hit

b. What is the memory size of one set in number of bits? What is the total cache memory (SRAM) size in number of bits? Note: Include the V bit in your calculations. Show the details of your calculation.

Each data 32 bits and address also 32 bits since memory size is 4 gb.

V bit = 1 bit,
Tag = (32 bits -2 bits byte offset -2 bits word block offset -1 bit index size) = 27 bits
4 data = 4*32 = 128 bits
For one set = 1 + 27 + 128 = 156 bits
Total 2 sets. Therefore 156 * 2 = 312 bits SRAM size.

c. State the number of AND and OR gates, EQUALITY COMPARATORs and MULTIPLEXERs needed to implement the cache memory. No drawing is needed.

One AND gate, one Equality Comparator and one 4-to-1 Multiplexer is needed.

3. (5 points: With 3 or more errors you get 0 points. Otherwise full point.) Consider the above MIPS code segment. The cache capacity is 2 words, block size is 1 word. N= 2. The block replacement policy is LRU.

a. In the following table indicate the type of miss, if any: Compulsory, Conflict, Capacity.

Instruction	Iteration No				
	1	2	3	4	5
lw $t1, 0xA4($0)	Compulsory	Capacity	Capacity	Capacity	Capacity
lw $t2, 0xA8($0)	Compulsory	Capacity	Capacity	Capacity	Capacity
lw $t3, 0xAC($0)	Capacity	Capacity	Capacity	Capacity	Capacity

b. How many bits are needed for the implementation of LRU policy: for a set, for the entire cache memory? What is the total cache memory size in number of bits? Include the V bit and the bit(s) used for LRU in your calculations. Show the details of your calculation.

Again each data 32 bits and address also 32 bits since memory size is 4 gb.

V bit = 1 bit
Tag = (32 bits -2 bits byte offset -0 bits word block offset -0 bit index size) = 30 bits
1 data = 1*32 = 32 bits
Used bit = 1 bit
For way 0 = 1 + 30 + 32 = 63 bits
For way 1 = 1 + 1 + 30 + 32 = 64
Total 127 bits SRAM size.

c. State the number of AND and OR gates, EQUALITY COMPARATORs and MULTIPLEXERs needed to implement the cache memory. No drawing is needed.

Since there are two Tags, two Equality Comparators are needed.
Since there are two comparators, 2 AND gates are needed to compare the result of the comparator and V bit.
One OR gate is needed for the result of AND gates.
One 2-to-1 Multiplexer is needed to choose among two data.