**BILKENT UNIVERSITY**

**COMPUTER ENGINEERING**

**CS 224**

**COMPUTER ORGANIZATION**

**LAB REPORT**

**LAB 06**

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**SECTION 4**

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* Throughout the testing I was not able to choose number of blocks bigger than 256 because of the size of my computer screen. First I tried to use larger block sizes for testing higher cache sizes however continuously I was getting very good hit rates and I thought it was not a healthy way of testing to observe different scenarios. So I decided to use smaller block sizes and smaller cache sizes.

1. **Matrix Size: 100**

**a)**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Cache Size ->**  **Block Size** | **2KB** | **4KB** | **8KB** | **16KB** | **32KB** |
| **32** | 48% | 48% | 52% | 53% | 85% |
| **64** | 49% | 49% | 49% | 51% | 83% |
| **128** | 61% | 61% | 61% | 61% | 85% |
| **256** | 80% | 80% | 80% | 80% | 93% |
| **512** | 90% | 90% | 90% | 90% | 96% |

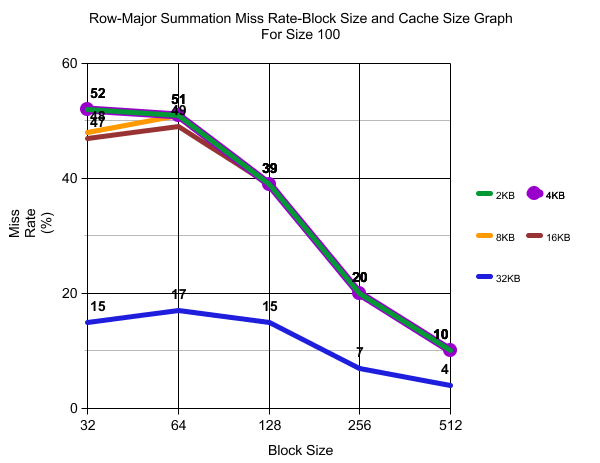
**Table 1.1 Direct Mapped Row-Major Summation Hit Rates**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Cache Size ->**  **Block Size** | **2KB** | **4KB** | **8KB** | **16KB** | **32KB** |
| **32** | 52% | 52% | 48% | 47% | 15% |
| **64** | 51% | 51% | 51% | 49% | 17% |
| **128** | 39% | 39% | 39% | 39% | 15% |
| **256** | 20% | 20% | 20% | 20% | 7% |
| **512** | 10% | 10% | 10% | 10% | 4% |

**Table 1.2 Direct Mapped Row-Major Summation Miss Rates**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Cache Size ->**  **Block Size** | **2KB** | **4KB** | **8KB** | **16KB** | **32KB** |
| **32** | 10314 | 10314 | 9537 | 9461 | 3098 |
| **64** | 10158 | 10158 | 10158 | 9752 | 3360 |
| **128** | 7896 | 7896 | 7896 | 7896 | 2912 |
| **256** | 3957 | 3957 | 3957 | 3957 | 1473 |
| **512** | 2021 | 2021 | 2021 | 2021 | 821 |

**Table 1.3 Direct Mapped Row-Major Summation Miss Counts**

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**Figure 1.1**

* For the direct mapped row-major summation of matrix size 100, I collected similar data for 2KB, 4KB, 8KB and 16KB caches. In these sizes, miss rates drop as block size increase which is an expected result. Also it is possible to get better hit rates by increasing the cache size. So 32KB cache has better hit rates than the smaller sizes. The reason for the similarities between 2KB, 4KB, 8KB and 16KB caches can be capacity misses which is meaning that the functionality of 2KB and16KB caches are same because already they are not enough large to deal with this big of data. However 32KB cache is appropriate to deal with this big of data. Even though 32KB cache has less miss rates, the trend of its line is same with the other sizes. So we can have an idea about the other types of misses(compulsory, conflict) according to change of block size.

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Cache Size ->**  **Block Size** | **2KB** | **4KB** | **8KB** | **16KB** | **32KB** |
| **32** | 97% | 97% | 97% | 97% | 98% |
| **64** | 98% | 98% | 98% | 98% | 99% |
| **128** | 99% | 99% | 99% | 99% | 99% |
| **256** | 100% | 100% | 100% | 100% | 100% |
| **512** | 100% | 100% | 100% | 100% | 100% |

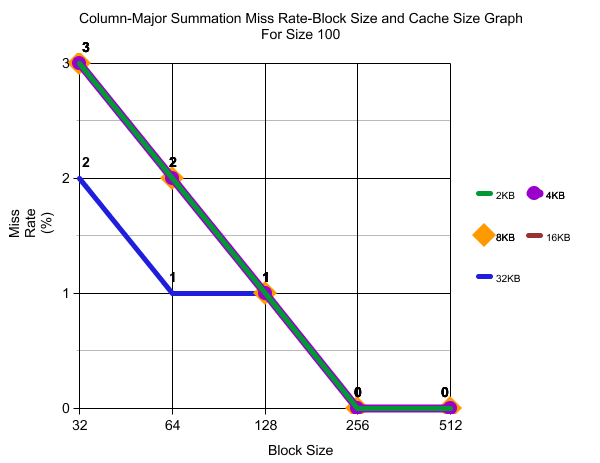
**Table 1.4 Direct Mapped Column-Major Summation Hit Rates**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Cache Size ->**  **Block Size** | **2KB** | **4KB** | **8KB** | **16KB** | **32KB** |
| **32** | 3% | 3% | 3% | 3% | 2% |
| **64** | 2% | 2% | 2% | 2% | 1% |
| **128** | 1% | 1% | 1% | 1% | 1% |
| **256** | 0% | 0% | 0% | 0% | 0% |
| **512** | 0% | 0% | 0% | 0% | 0% |

**Table 1.5 Direct Mapped Column-Major Summation Miss Rates**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Cache Size ->**  **Block Size** | **2KB** | **4KB** | **8KB** | **16KB** | **32KB** |
| **32** | 627 | 627 | 627 | 627 | 428 |
| **64** | 315 | 315 | 315 | 315 | 216 |
| **128** | 159 | 159 | 159 | 159 | 110 |
| **256** | 81 | 81 | 81 | 81 | 57 |
| **512** | 41 | 41 | 41 | 41 | 29 |

**Table 1.6 Direct Mapped Column-Major Summation Miss Counts**

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**Figure 1.2**

* Column-major summation is a basic array summation which is an easy computation for computer because while computing the sum the address increases regularly without jumping unexpected addresses. So I could collect very low miss rates for all types of cache sizes and block sizes.

**b)**

|  |  |  |  |
| --- | --- | --- | --- |
|  | **Cache 4KB, BS 32** | **Cache 16KB, BS 128** | **Cache 32KB, BS 512** |
| **Poor Hit Rate** | **Medium Hit Rate** | **Good Hit Rate** |
| **Direct Mapped** | 48% | 61% | 96% |
| **Fully Associative-LRU** | 48% | 61% | 90% |
| **Fully Associative-Random** | 51% | 65% | 96% |

**Table 1.7 Hit Rate Values of Row-Major Summation for Matrix Size 100**

* In a general look it’s seen that Fully Associative-LRU does not have some much difference with direct mapped however, fully associative-random increases the hit rates. The reason for this, because of the spatial locality in fully associative, LRU policy can’t make better guesses because the address jumping to a long distance while summing the elements. Random policy could give better results because it is able to use advantages of spatial locality by eliminating the disadvantages of LRU policy.

**c)**

|  |  |  |  |
| --- | --- | --- | --- |
| **Medium Hit Rate (Cache 16KB, BS 128)** | **Hit Rate** | **Miss Rate** | **Miss Count** |
| **Set Size 4** | 61% | 39% | 10314 |
| **Set Size 8** | 61% | 39% | 10314 |
| **Set Size 16** | 61% | 39% | 10314 |
| **Set Size 32** | 61% | 39% | 10314 |

**Table 1.8 Hit-Miss Rates and Miss Counts for N-Way Associative (Medium Hit Rate)**

|  |  |  |  |
| --- | --- | --- | --- |
| **Good Hit Rate (Cache 32KB, BS 512)** | **Hit Rate** | **Miss Rate** | **Miss Count** |
| **Set Size 4** | 90% | 10% | 2021 |
| **Set Size 8** | 90% | 10% | 2021 |
| **Set Size 16** | 90% | 10% | 2021 |
| **Set Size 32** | - | - | - |

**Table 1.9 Hit-Miss Rates and Miss Counts for N-Way Associative (Good Hit Rate)**

|  |  |  |  |
| --- | --- | --- | --- |
| **Poor Hit Rate (Cache 4KB, BS 32)** | **Hit Rate** | **Miss Rate** | **Miss Count** |
| **Set Size 4** | 48% | 52% | 10314 |
| **Set Size 8** | 48% | 52% | 10314 |
| **Set Size 16** | 48% | 52% | 10314 |
| **Set Size 32** | 48% | 52% | 10314 |

**Table 1.10 Hit-Miss Rates and Miss Counts for N-Way Associative (Poor Hit Rate)**

* N-way associative does not change anything for any different value in terms of hit rates and miss rates. N-way associative is a good method for reducing the conflict misses however according to my results in (a), usually there are capacity misses. Because of the lack conflict misses, we could not observe the positive affects of N-way associative in these results.

1. **Matrix Size: 250**

**a)**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Cache Size ->**  **Block Size** | **2KB** | **4KB** | **8KB** | **16KB** | **32KB** |
| **32** | 48% | 48% | 48% | 55% | 77% |
| **64** | 49% | 49% | 49% | 49% | 54% |
| **128** | 50% | 50% | 50% | 50% | 50% |
| **256** | 51% | 51% | 51% | 51% | 51% |
| **512** | 75% | 75% | 75% | 75% | 75% |

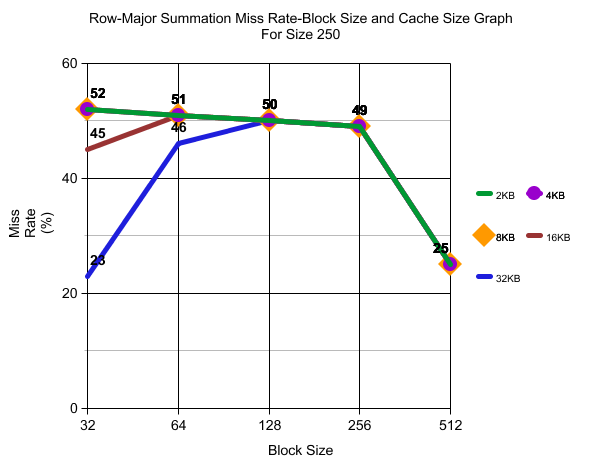
**Table 2.1 Direct Mapped Row-Major Summation Hit Rates**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Cache Size ->**  **Block Size** | **2KB** | **4KB** | **8KB** | **16KB** | **32KB** |
| **32** | 52% | 52% | 52% | 45% | 23% |
| **64** | 51% | 51% | 51% | 51% | 46% |
| **128** | 50% | 50% | 50% | 50% | 50% |
| **256** | 49% | 49% | 49% | 49% | 49% |
| **512** | 25% | 25% | 25% | 25% | 25% |

**Table 2.2 Direct Mapped Row-Major Summation Miss Rates**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Cache Size ->**  **Block Size** | **2KB** | **4KB** | **8KB** | **16KB** | **32KB** |
| **32** | 64455 | 64455 | 64455 | 56144 | 28195 |
| **64** | 63478 | 63478 | 63478 | 63478 | 58015 |
| **128** | 62990 | 62990 | 62990 | 62990 | 62990 |
| **256** | 61282 | 61282 | 61282 | 61282 | 61282 |
| **512** | 30660 | 30660 | 30660 | 30660 | 30660 |

**Table 2.3 Direct Mapped Row-Major Summation Miss Counts**

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**Figure 2.1**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Cache Size ->**  **Block Size** | **2KB** | **4KB** | **8KB** | **16KB** | **32KB** |
| **32** | 97% | 97% | 97% | 97% | 97% |
| **64** | 98% | 98% | 98% | 98% | 98% |
| **128** | 99% | 99% | 99% | 99% | 99% |
| **256** | 100% | 100% | 100% | 100% | 100% |
| **512** | 100% | 100% | 100% | 100% | 100% |

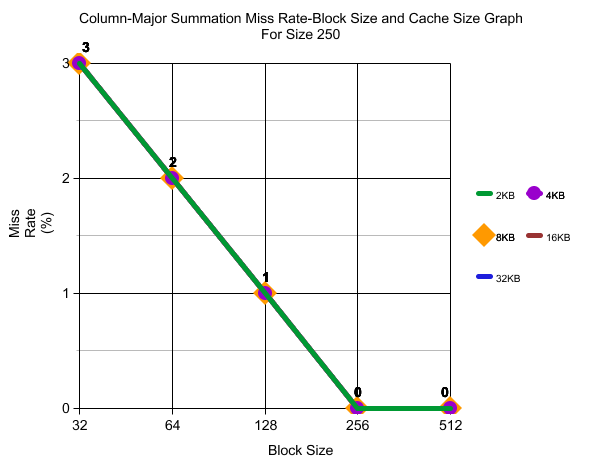
**Table 2.4 Direct Mapped Column-Major Summation Hit Rates**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Cache Size ->**  **Block Size** | **2KB** | **4KB** | **8KB** | **16KB** | **32KB** |
| **32** | 3% | 3% | 3% | 3% | 3% |
| **64** | 2% | 2% | 2% | 2% | 2% |
| **128** | 1% | 1% | 1% | 1% | 1% |
| **256** | 0% | 0% | 0% | 0% | 0% |
| **512** | 0% | 0% | 0% | 0% | 0% |

**Table 2.5 Direct Mapped Column-Major Summation Miss Rates**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Cache Size ->**  **Block Size** | **2KB** | **4KB** | **8KB** | **16KB** | **32KB** |
| **32** | 3909 | 3909 | 3909 | 3909 | 3909 |
| **64** | 1955 | 1955 | 1955 | 1955 | 1955 |
| **128** | 979 | 979 | 979 | 979 | 979 |
| **256** | 491 | 491 | 491 | 491 | 491 |
| **512** | 247 | 247 | 247 | 247 | 247 |

**Table 2.6 Direct Mapped Column-Major Summation Miss Counts**

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**Figure 2.2**

**b)**

|  |  |  |  |
| --- | --- | --- | --- |
|  | **Cache 8KB, BS 32** | **Cache 16KB, BS 32** | **Cache 32KB, BS 32** |
| **Poor Hit Rate** | **Medium Hit Rate** | **Good Hit Rate** |
| **Direct Mapped** | 48% | 55% | 77% |
| **Fully Associative-LRU** | 48% | 48% | 97% |
| **Fully Associative-Random** | 49% | 59% | 88% |

**Table 2.7 Hit Rate Values of Row-Major Summation for Matrix Size 100**

**c)**

|  |  |  |  |
| --- | --- | --- | --- |
| **Medium Hit Rate (Cache 16KB, BS 32)** | **Hit Rate** | **Miss Rate** | **Miss Count** |
| **Set Size 4** | 48% | 52% | 64455 |
| **Set Size 8** | 48% | 52% | 64455 |
| **Set Size 16** | 48% | 52% | 64455 |
| **Set Size 32** | 48% | 52% | 64455 |

**Table 2.8 Hit-Miss Rates and Miss Counts for N-Way Associative (Medium Hit Rate)**

|  |  |  |  |
| --- | --- | --- | --- |
| **Good Hit Rate (Cache 32KB, BS 32)** | **Hit Rate** | **Miss Rate** | **Miss Count** |
| **Set Size 4** | 83% | 17% | 21417 |
| **Set Size 8** | 88% | 12% | 14390 |
| **Set Size 16** | 95% | 5% | 6181 |
| **Set Size 32** | 95% | 5% | 6619 |

**Table 2.9 Hit-Miss Rates and Miss Counts for N-Way Associative (Good Hit Rate)**

|  |  |  |  |
| --- | --- | --- | --- |
| **Poor Hit Rate (Cache 16KB, BS 128)** | **Hit Rate** | **Miss Rate** | **Miss Count** |
| **Set Size 4** | 48% | 52% | 64455 |
| **Set Size 8** | 48% | 52% | 64455 |
| **Set Size 16** | 48% | 52% | 64455 |
| **Set Size 32** | 48% | 52% | 64455 |

**Table 2.10 Hit-Miss Rates and Miss Counts for N-Way Associative (Poor Hit Rate)**