**Digital Design**

**CS223**

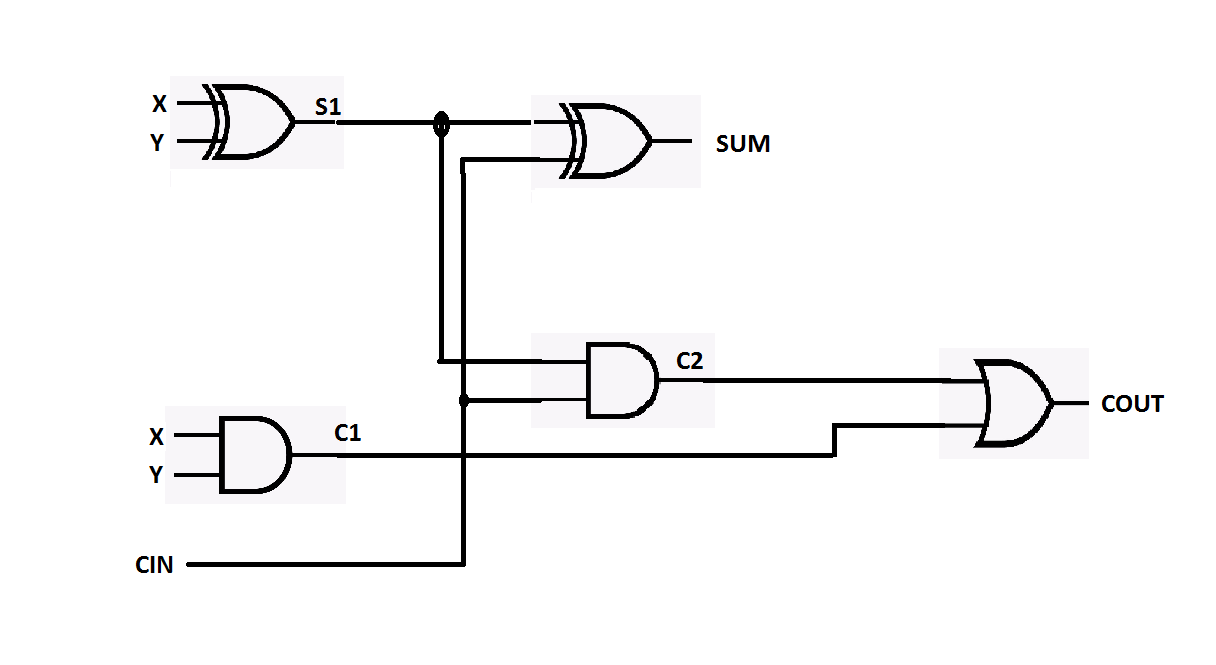
**Lab 02**

**Berk Yıldız**

**21502040**

**10.10.2017**

**Trainer Pack 31**

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**Dataflow Systemverilog**

module fullAdder(

input logic X,Y,CIN,

output logic SUM,COUT);

assign SUM = X^Y^CIN;

assign COUT = (X&Y)|((X^Y)&CIN);

endmodule

**Testbench**

module testfullAdder();

logic X,Y,CIN,SUM,COUT;

fullAdder uut (X,Y,CIN,SUM,COUT);

initial begin

#100;

X=0; Y=0; CIN=0; #10;

X=0; Y=0; CIN=1; #10;

X=0; Y=1; CIN=0; #10;

X=0; Y=1; CIN=1; #10;

X=1; Y=0; CIN=0; #10;

X=1; Y=0; CIN=1; #10;

X=1; Y=1; CIN=0; #10;

X=1; Y=1; CIN=1; #10;

end

Endmodule

**Structural Systemverilog**

Module fullAdder(

input logic X,Y,CIN,

output logic SUM, COUT);

logic S1,C1,C2;

xor(S1,X,Y);

xor(SUM,CIN,S1);

and(C1,X,Y);

and(C2,S1,CIN);

or(COUT,C1,C2);

endmodule;

**Testbench**

module testfullAdder();

logic X,Y,CIN,SUM,COUT;

fullAdder uut (X,Y,CIN,SUM,COUT);

initial begin

#100;

X=0; Y=0; CIN=0; #10;

X=0; Y=0; CIN=1; #10;

X=0; Y=1; CIN=0; #10;

X=0; Y=1; CIN=1; #10;

X=1; Y=0; CIN=0; #10;

X=1; Y=0; CIN=1; #10;

X=1; Y=1; CIN=0; #10;

X=1; Y=1; CIN=1; #10;

end

Endmodule