**CS223**

**DIGITAL DESIGN**

**LAB 03**

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**21502040**

**PACK NUMBER 31**

**SystemVerilog module for Part A-a.**

module D2to4\_decoder ( input logic i1,i0,

output logic y3,y2,y1,y0) ;

assign y3 = i1 & i0 ;

assign y2 = i1 & ~i0 ;

assign y1 = ~i1 & i0 ;

assign y0 = ~i1 & ~i0 ;

endmodule

**Testbench for Part A-a**

module testD2to4\_decoder();

logic i1,i0,y3,y2,y1,y0;

D2to4\_decoder uut(i1,i0);

initial begin

#100;

i1=0; i0=0; #10;

i1=0; i0=1; #10;

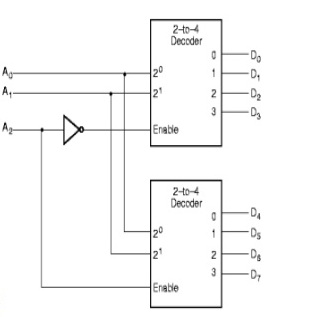
i1=1; i0=0; #10;

i1=1; i0=1; #10;

end

endmodule

**Schematic for Part A-e**

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**SystemVerilog module for Part A-e**

module D3to8\_decoder(output logic [7:0]o,input logic [2:0]i);

wire x;

inv d1(x,i[2]);

D2to4\_decoder d2(o[3:0],i[1],i[0],x);

D2to4\_decoder d3(o[7:4],i[1],i[0],i[2]);

endmodule

**Testbench**

module test\_d3to8();

logic i[0],i[1],i[2],o[0],o[1],o[2],o[3],o[4],o[5],o[6],o[7];

D3to8\_decoder uut (i[0],i[1],i[2],o[0],o[1],o[2],o[3],o[4],o[5],o[6],o[7]);

initial begin

#100; // wait

i[0]=0; i[1]=0; i[2]=0; #10 ;

i[0]=0; i[1]=0; i[2]=1; #10 ;

i[0]=0; i[1]=1; i[2]=0; #10 ;

i[0]=0; i[1]=1; i[2]=1; #10 ;

i[0]=1; i[1]=0; i[2]=0; #10 ;

i[0]=1; i[1]=0; i[2]=1; #10 ;

i[0]=1; i[1]=1; i[2]=0; #10 ;

i[0]=1; i[1]=1; i[2]=1; #10 ;

end

endmodule

**SystemVerilog module for Part C-a.**

module mux4( input logic i3,i2,i1,i0,s1,s0,

output logic z );

logic d1,d0;

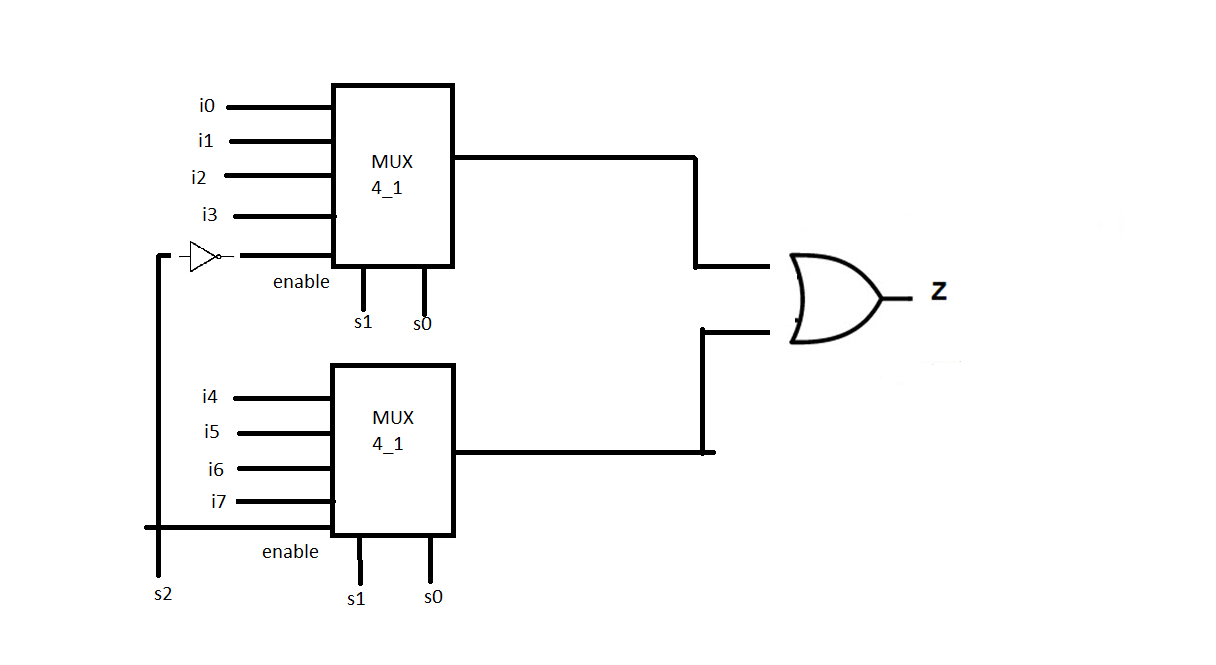
assign d1 = ~s0 & i2|s0 & i3;

assign d0 = ~s0 & i0|s0 & i1;

assign z = ~s1 & d0|s1 & d1;

endmodule

**Schematic for Part C-b.**

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**System Verilog module for Part C-b.**

module mux2\_8(input logic [7:0] d0, d1,

input logic s,

output logic [7:0] y);

mux4 lsbmux(d0[3:0], d1[3:0], s, y[3:0]);

mux4 msbmux(d0[7:4], d1[7:4], s, y[7:4]);

endmodule